A New Fault-Tolerant Topology and Operation Scheme for the High Voltage Stage in a Three-Phase Solid-State Transformer

By

Ali Mohamed Alshawish

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Doctor of Philosophy

Dr. Prasad Kulkarni

Dr. Alessandro Salandrino

Dr. Taejoon Kim

Dr. Morteza Hashemi

Dr. Elaina Sutley

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The dissertation committee for Ali Mohamed Alshawish certifies that this is the approved version of the following dissertation:

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A New Fault-Tolerant Topology and Operation Scheme for the High Voltage Stage in a Three-Phase Solid-State Transformer

Dr. Prasad Kulkarni, Chairperson

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Abstract

Solid-state transformers (SSTs) are comprised of several cascaded power stages with different voltage levels. This leads to more challenges for operation and maintenance of the SSTs not only under critical conditions, but also during normal operation. However, one of the most important reliability concerns for the SSTs is related to high voltage side switch and grid faults. High voltage stress on the switches, together with the fact that most modern SST topologies incorporate large number of power switches in the high voltage side, contribute to a higher probability of a switch fault occurrence. The power electronic switches in the high voltage stage are under very high voltage stress, significantly higher than other SST stages. Therefore, the probability of the switch failures becomes more substantial in this stage. In this research, a new technique is proposed to improve the overall reliability of the SSTs by enhancing the reliability of the high voltage stage.

The proposed method restores the normal operation of the SST from the point of view of the load even though the input stage voltages are unbalanced due to the switch faults. On the other hand, high voltage grid faults that result in unbalanced operating conditions in the SST can also lead to dire consequences in regards to safety and reliability. The proposed method can also revamp the faulty operation to the pre-fault conditions in the case of grid faults. The proposed method integrates the quasi-z-source inverter topology into the SST topology for rebalancing the transformer voltages. Therefore, this work develops a new SST topology in conjunction with a fault-tolerant operation strategy that can fully restore operation of the proposed SST in the case of the two aforementioned fault scenarios. The proposed fault-tolerant operation strategy rebalances the line-to-line voltages after a fault occurrence by modifying the phase angles between the phase voltages generated by the high voltage stage of the proposed SST. The boosting property of the

quasi-z-source inverter topology circuitry is then used to increase the amplitude of the rebalanced line-to-line voltages to their pre-fault values. A modified modulation technique is proposed for modifying the phase angles and controlling the quasi-z-source inverter topology shoot-through duty ratio.

The specific contributions of this work are as follows:

- The proposed method enables the SST to operate normally in case of switch fault occurrences due to high voltage stress. The function of faulty cells is compensated for without adding any extra legs or backup power cells. The remaining healthy cells are used to modify and balance the output voltage.
- Using the proposed method, the delivered power by the SST after fault occurrence will be the same as the pre-fault conditions. Modifying the angles of phase voltages and using the feature of the proposed SST to boost the voltages lead to deliver the same power as in the pre-fault conditions.
- Using the quasi-z-source inverter topology in the proposed method increases the reliability of the proposed SST topology since the transformer will have the ability to generate balanced three phase voltages using only two phase voltages.
- The proposed method increases the lifetime of the SST after fault occurrence by distributing the voltage stress symmetrically between all cells of the high voltage stage in the three phases.
- The proposed method guarantees the regulation of the output voltage of the SST, since the proposed SST topology can isolate the load from any disturbances in the grid. Also, the obtained output voltage of the proposed SST is balanced. As a result of this, there is no

difference between the pre-fault voltage and post-fault voltage. Therefore, the obtained voltages will be synchronized well with the grid.

Dedication

To my mother, my father, my brothers, and my sisters.

Acknowledgements

I would like to thank all members of the advisory committee for their comments and suggestions. Also, I would like to thank Dr. Ahmad for his great advice, guidance, and invaluable feedback on my research.

I deeply thank my mother and my father for their everlasting support. I am really appreciative of their excellent encouragement, and I am privileged that I have been raised in such a fabulous family. Also, thanks go to my friends for their companionship related to my PhD research.

Special thanks to Allah (God) who has given me the power to acquire new skills and knowledge to obtain this level of education to complete my PhD program.

Table of Contents

List of Figures

List of Tables

Chapter 1

1.1 Introduction

Electric energy is conventionally generated in massive power plants which are distributed over the power grid. These conventional power plants can be gas turbine power plants, nuclear power plants, steam power plants, coal power plants, or combined-cycle gas and steam turbine power plants. The main source of energy for these power plants therefore is non-renewable, e.g. coal, crude oil, natural gas, uranium, and etc [1, 2]. The generated power by conventional power plants is dispatchable. Also, conventionally the power flow has only one direction from the power plants to consumers on the grid. Power systems in general are comprised of three main stages. The three stages are generation units (plants), transmission systems (transmission lines), and distribution systems [2-5].

Transformers are employed in all three stages to transfer various voltage levels. The electric energy is generated in power plants and transformed to a very high voltage level for transmission by huge transformers [4, 5]. Then it is transmitted by high voltage transmission lines for long distances. Finally, the delivered electric energy to the consumer loads is transformed to a lower voltage in several steps using smaller transformers [4, 5]. This process demands hundreds of traditional power transformations in each stage of the grid. Step-up transformers are connected in

the transmission stage of the grid and close to the power plants, while step-down transformers are connected in the distribution stage of the grid and close to the consumers.

However, it is anticipated that in the smart grid of the future, integration of renewable energy sources makes the operation and control of power grid more complicated. The renewable energy sources can be installed on various levels on the grid [4, 6]. Therefore:

- The consumers can support the grid by selling the energy back to the grid.
- The generated renewable power is not unidirectional anymore.
- The total power in the grid is not predictable.

This makes the use of traditional power transformers over the grid problematic. Even though the traditional power transformers have high reliability and high efficiency, they pose several issues to the grid of the future [5, 7, 8]:

- Big size and heavy weight due to requirements of big steel pieces.
- Voltage drop due to heavy loads.
- Poor capability of dynamic control due to use of renewable energy sources.
- Inability to limit and isolate the propagation of voltage sag or fault occurrence from one side to another side.
- Sensitivity to harmonics since they are designed to work at low frequency (60 Hz).
- Inability to work with multi-input (AC/DC) sources.

1.2 Definition of the Solid-State Transformer

Solving the previous issues requires new technologies. One of these technologies is the solid-state transformer (SST). The SST is basically a power electronic converter operating partially at high frequency [2, 8]. It is considered as a key component and the main part of the smart grid. It is known as a power electronic transformer (PET), electronic power transformer (EPT), or an

intelligent universal transformer (IUT) [3, 7-11]. It is a new technology, and its behavior is unclear especially under critical conditions of the electrical grid. In order to investigate the working of the SSTs in the power grid, this research will study this device under two fault conditions. Then it proposes a fault-tolerant operation method to enable a multilevel cascaded h-bridge based high stage SST to continue normal operation in the faulty conditions. The SST mainly consists of a high frequency transformer and at least one of three power electronic stages. These stages are an AC/DC converter stage, a DC/DC converter stage, and a DC/AC converter stage [3, 6, 9-15]. However, the traditional power transformer is used only to step the voltage up or down. The SSTs not only can provide this capability but they can also offer more features in comparison to traditional power transformers, along with smaller size and reduced weight due to high frequency operation, which is inversely proportional to the size [3, 4, 6-13, 16]. Therefore, there is no need for large magnetic core materials. Figure 1.1 and Figure 1.2 show the general schematic of a traditional power transformer and a solid-sate transformer.

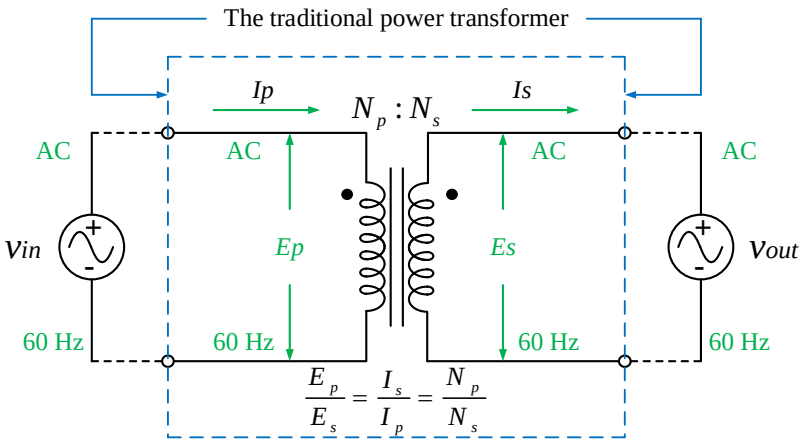


Figure 1.1. The general schematic of a traditional power transformer.

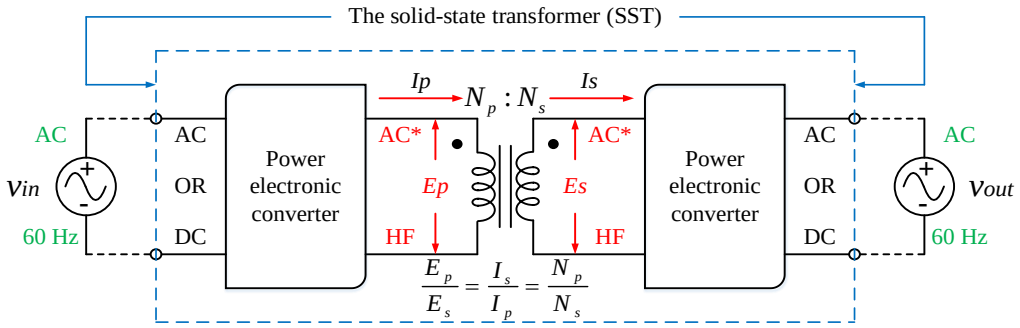


Figure 1.2. The general schematic of a solid-state transformer.

1.3 Advantages of the Solid-State Transformer

- Excellent capabilities not only to generate a three-phase output from a single-phase input, but also to make the output voltage with a different frequency from the input.
- Extremely short time for regulating the bus voltages.
- Great capabilities for compensating the voltage and to correct the voltage sag.
- Possibility of a DC input and an output (DC or AC).
- Management and isolation of the current fault on both transformer sides.
- Active power flow control in both directions.
- Correction of the power factor.
- Excellent device to compensate for reactive power on both transformer sides.
- Eliminating the voltage sag due to existing the DC link.

In addition to the mentioned features [2-4, 6-13, 15-19] most SSTs have isolated voltage source converters, but conversion stages of most SSTs require complex controllers. This leads to some disadvantages compared to the traditional power transformer [7, 9, 20].

1.4 Disadvantages of the Solid-State Transformer

- High cost due to expensive high frequency, high-voltage, and high-power semiconductors.
- Low efficiency because of semiconductor losses, which is a big challenge of the SST.

- Poor reliability since the SST requires many components for the modern designs.

However, due to important development in power electronics, the required power semiconductor devices for the SSTs have become available with superior characteristics as well as an acceptable price (e.g. SiC switches) [3, 7, 9, 12]. Therefore, SSTs are becoming economically feasible to be used in the grid instead of using the traditional power transformer. The general working idea of the SST is the input frequency is changed to a higher frequency by using the power semiconductors [3, 9]. Then the input is increased or decreased through the high frequency transformer. Finally, the output of the transformer is reshaped again to be low frequency (60 Hz). It is clear to see that the high frequency operation is the key enabling advantage of the SSTs since the frequency is inversely proportional with the size [3, 9].

1.5 Classification of the Solid-State Transformers

Using the SSTs in different applications requires appropriate design for each application. Numerous SST topologies have been proposed in recent years to achieve different goals, but the majority of them have some common building blocks. They employ a high frequency transformer to step voltage down or up and several stages of power electronic converters [3, 9].

The SSTs can have multiple different inputs and multiple different outputs. In the same circuit, the input and output can be AC voltage or DC voltage. These characteristics require different power converters connected in different ways. Therefore, both of the power converters connected to the high frequency transformer have to be built appropriately to generate the correct output [3, 9, 13]. Also, the controller for each converter has to be designed well to achieve and guarantee the desired output. The first designed SST was a single-phase AC/AC isolated converter. However, SST topologies have been advancing a lot in past few years. These topologies have different

converters connected in multi-stage structures to support DC/DC isolation such as a dual active bridge (DAB) converter [3, 6].

The SSTs can be classified based on existence of the DC link in either side of the high-frequency transformers. These classifications are according to SST applications and features that required the DC link and the level of the DC voltage (HVDC, MVDC, or LVDC). Accordingly, SSTs can be categorized into four categories [3, 6, 7, 12-15].

- A single-stage SST.
- A two-stage SST with a low voltage DC link on the secondary side (the low voltage side).
- A two-stage SST with a high voltage DC link on the primary side (the high voltage side).
- A three-stage SST with a high voltage DC link on the primary side and a low voltage DC link on the secondary side (the high voltage side and the low voltage side).

The main topology configuration for these categories are shown in Figure 1.3.

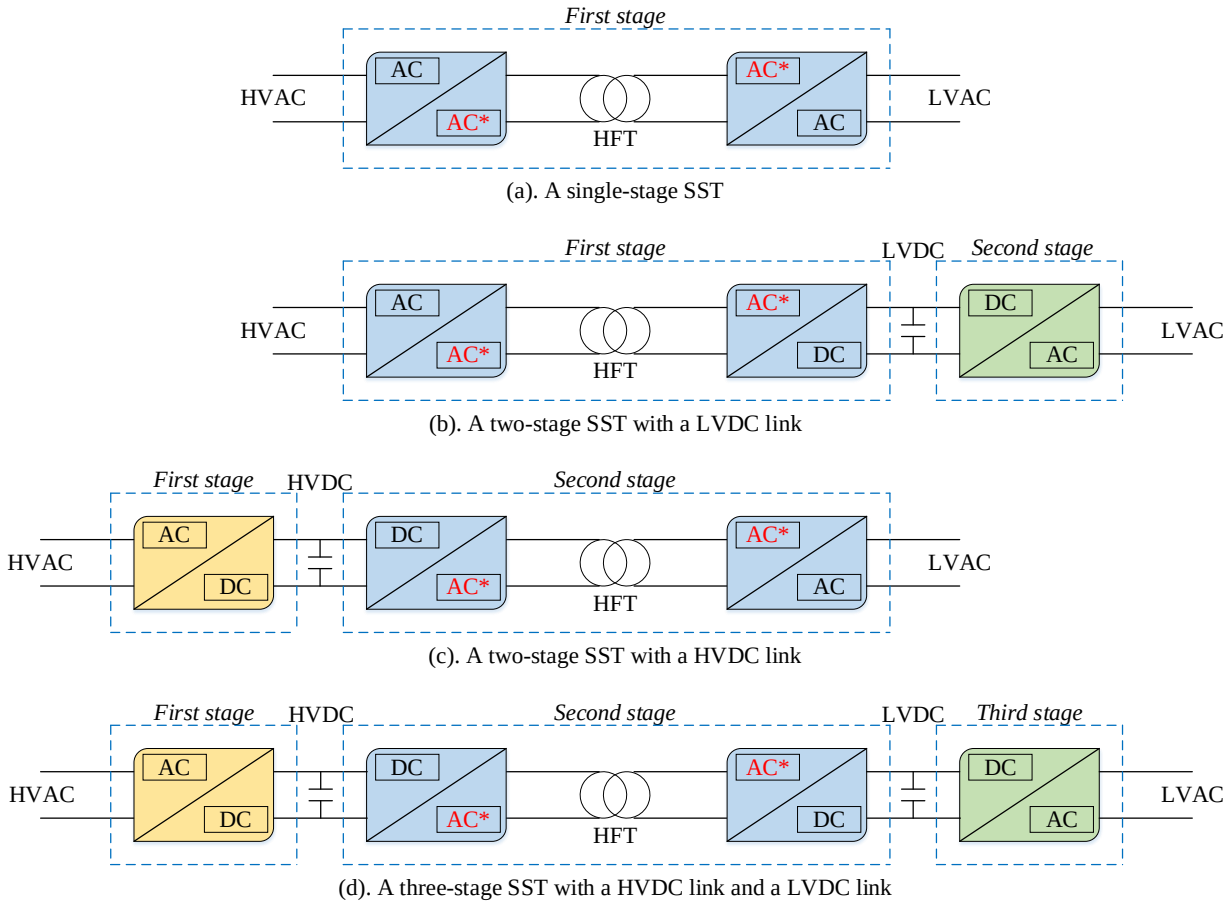


Figure 1.3. SST categories (AC with 60Hz and AC* with a high frequency).

1.5.1 A Single-Stage SST

There is no DC link because this solid-state transformer has only one stage for power conversion. Therefore, it directly converts high voltage AC to low voltage AC without needing a DC voltage stage [3, 6, 7, 19]. This can be done by chopping the high voltage AC into a high frequency waveform. The high-frequency transformer works to step down the voltage as well as to provide galvanic isolation. Then the output voltage (the high frequency waveform) will be reshaped again into low voltage AC with 60 Hz. This topology does not require a complex control system [14]. Also, it does not offer any extra features such as power factor correction or reactive power compensation in the grid since there is no DC link [3, 6, 13-15]. This is considered as drawback to use it in the smart grid. The single-stage SST can be divided to two groups. The first

group has four-quadrant switches on both sides of the high-frequency transformer. The second group has two-quadrant switches on both sides of the high-frequency transformer [3, 6]. There are several converter topologies that can be used in this kind of SSTs, such as a cycloconverter, and a dual active bridge converter. Figure 1.4 and Figure 1.5 show a single-stage SST based on an AC/AC cycloconverter [21-23] and an AC/AC dual active bridge (DAB) converter [24-26].

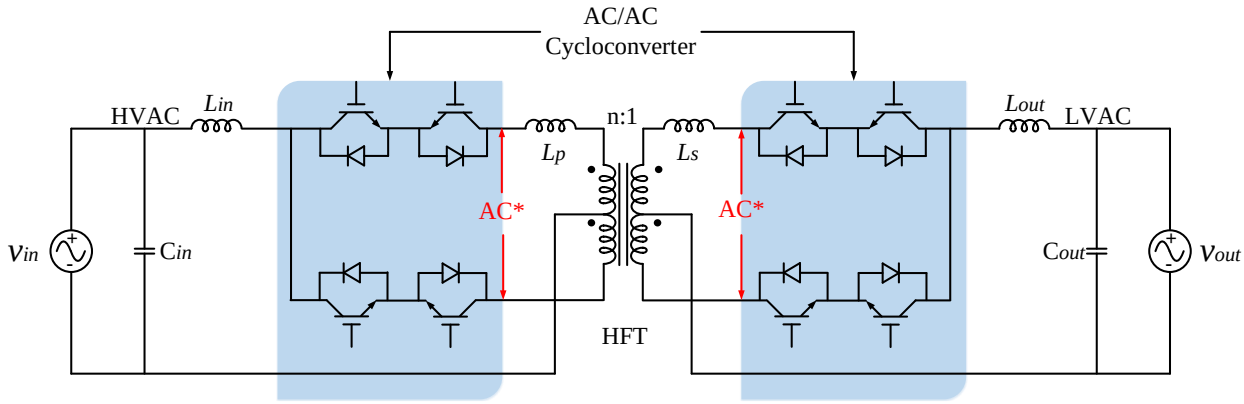


Figure 1.4. A single-stage SST based on an AC/AC cycloconverter.

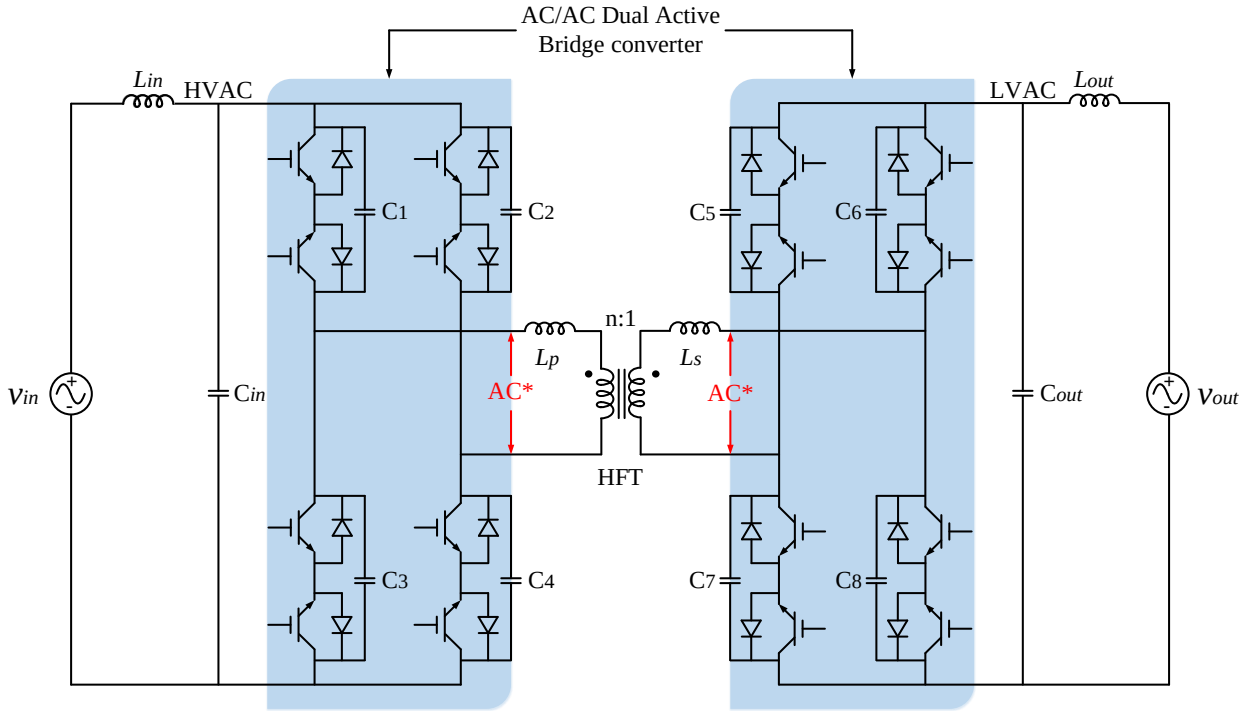


Figure 1.5. A single-stage SST based on an AC/AC dual active bridge (DAB) converter.

1.5.2 A Two-Stage SST with a Low Voltage DC Link on the Secondary Side

This kind of SSTs can be implemented by connecting one more stage on the secondary side of the high-frequency transformer of the single-stage SST. The output of the first stage is designed to be low voltage DC. Therefore, the added stage is implemented by using a DC/AC converter (an inverter) to convert the low voltage DC to low voltage AC with 60 Hz [7]. The high-frequency transformer works to step down the voltage as well as to provide galvanic isolation, which is the same as in the single-stage SST [3]. The DC link provides more flexibility to the two-stage SST. This topology simplifies connecting DC sources or DC loads to the grid, since there is a DC link in the low voltage side of the transformer. It provides an important feature to correct the power factor [3, 12, 13]. Also, it supports the isolation of storage devices and supplying power back to the grid [9, 13, 15]. However, large capacitors are required to filter a large ripple (120 Hz). This ripple is generated on both sides of the transformer since there is no high voltage DC link in the primary side [13, 14]. The two-stage SST with a low voltage DC link can be implemented by different converters such as a flyback converter, a cycloconverter, and a dual active bridge converter. Figure 1.6 and Figure 1.7 show a two-stage SST based on an AC/DC cycloconverter [27-29] and an AC/DC dual active bridge (DAB) converter [30-32] respectively.

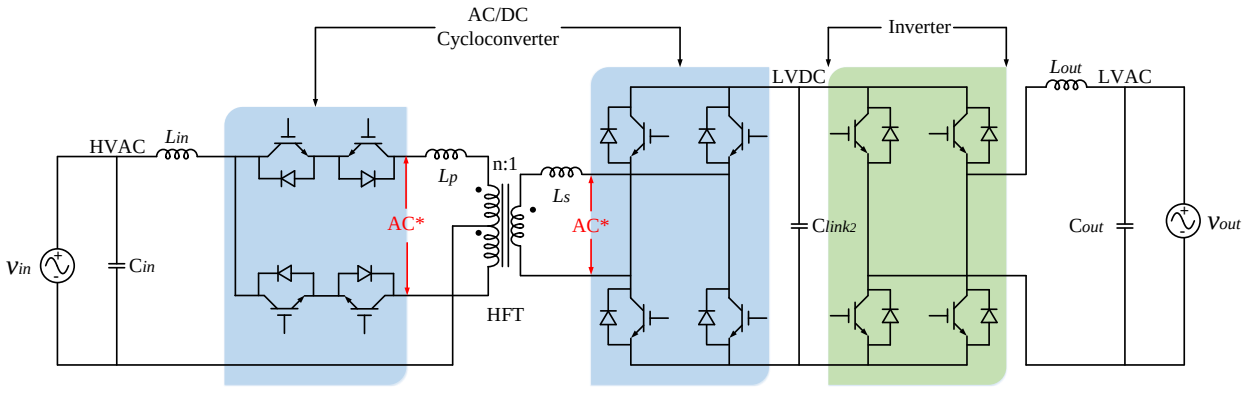


Figure 1.6. A two-stage SST based on an AC/DC cycloconverter.

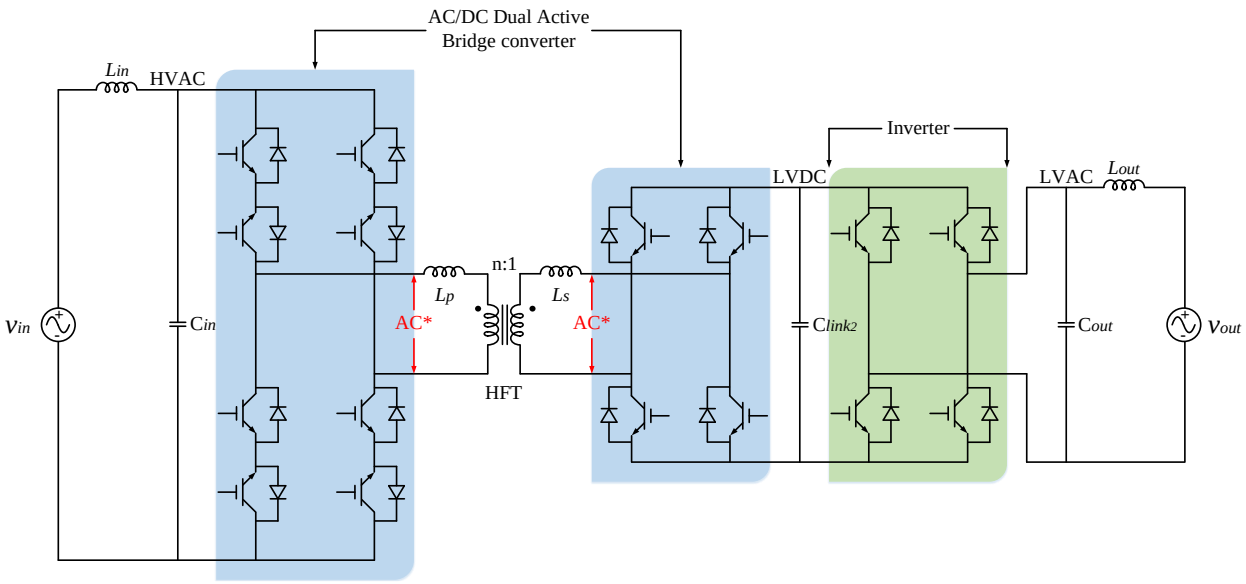


Figure 1.7. A two-stage SST based on an AC/DC dual (DAB) active bridge converter.

1.5.3 A Two-Stage SST with a High Voltage DC Link on the Primary Side

It is similar to the topology with a low voltage DC link, but the added stage is an AC/DC converter (a rectifier). This stage is connected to the grid to create a high voltage DC link. The high voltage grid is converted to high voltage DC by an AC/DC converter (a rectifier) in the first stage [3, 6, 7]. The rectifier output requires bulky capacitors because of the high voltage DC. Therefore, to minimize the capacitor size, it is necessary to divide this stage to multilevel converters [3, 9]. The multilevel converters have attractive features such as near sinusoidal voltage and currents, higher efficiency, reduced harmonic contents, and ability to employ fault tolerant operation [3]. In the second stage, the high voltage DC is converted to high voltage AC with high-frequency, and the transformer steps down this voltage with the same high-frequency. Eventually, the voltage at the secondary side of the transformer is converted to low voltage AC with 60 Hz. This kind of SSTs does not support the injection of the power to the grid because of the lack of low voltage DC link [3]. However, the DC link is in the high voltage side of the transformer, therefore, there is no isolation from the grid. As a result, this topology is unsuitable for distributed

energy resources integration as well as energy storage [14]. Hence, to make it workable for SST implementations, an AC/DC converter (a rectifier) has to be connected to the grid to get a three-stage SST topology. This type of SSTs can be implemented using various converters such as a flyback converter [33-35] and a dual active bridge (DAB) converter [36-38]. The two-stage SST based on these converters are shown in Figure 1.8 and Figure 1.9 respectively.

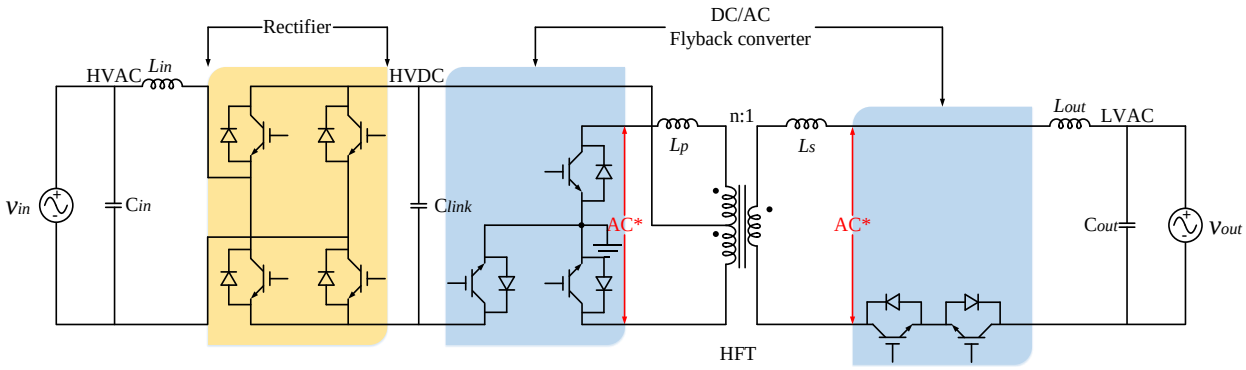


Figure 1.8. A two-stage SST based on a DC/AC flyback converter.

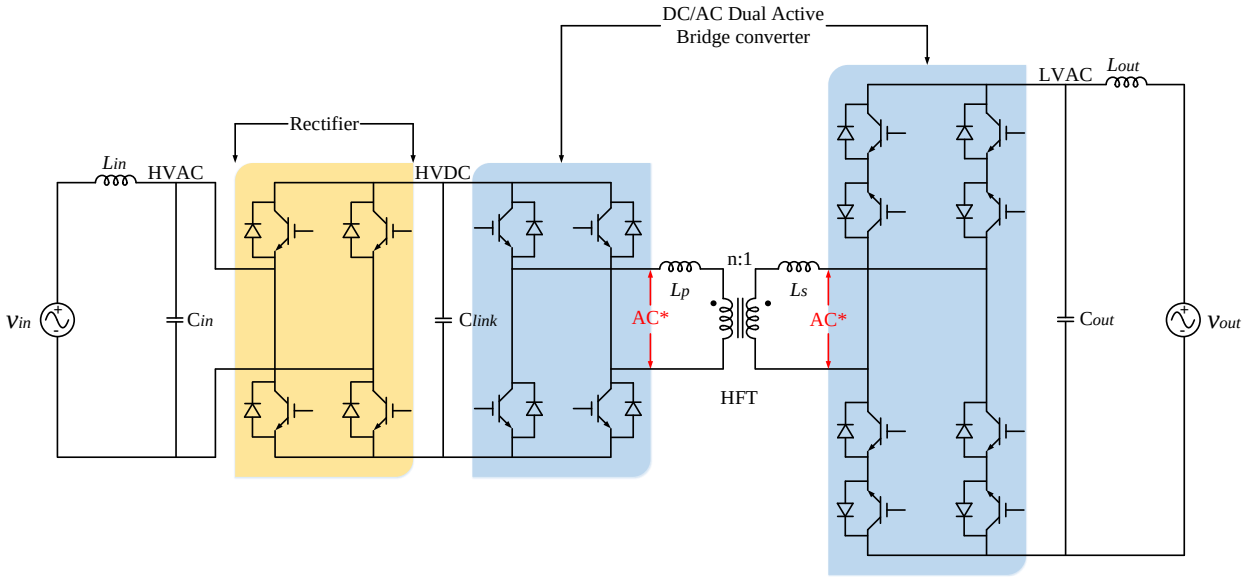


Figure 1.9. A two-stage SST based on a DC/AC dual active bridge (DAB) converter.

1.5.4 A Three-Stage SST with a High Voltage DC Link on the Primary Side and a Low Voltage DC Link on the Secondary Side

This topology consists of all other SST topologies. It consists of an AC/DC converter (a rectifier), an isolated DC/DC converter, and a DC/AC converter (an inverter). The three different stages are integrated together to enable this kind of SSTs to offer more features in different places of the grid. This SST has a high voltage DC link and a low voltage DC link [3, 6, 13-15]. In the first stage, the high voltage grid is converted to high voltage DC by using an AC/DC converter (a rectifier). In the second stage, called a DC/DC conversion stage, the high voltage DC is converted to high voltage AC with high-frequency. Then it is stepped down by the transformer, and it is converted to low voltage DC. Finally, the low voltage DC is converted to low voltage AC with 60 Hz by a DC/AC converter (an inverter) [7]. This type of SSTs is widely used in different applications more than other SST types because of its capability to provide all SST functions. Both DC links support controlling the active and reactive power independently to have unity power factor. Also, this type of SSTs provides better control of the voltage regulation and voltage sag [3, 12]. However, it is not easy to design a controller for this topology since each stage has independent control states from the other stages. Figure 1.10 shows a three-stage SST based on a DC/DC dual active bridge (DAB) converter [39-41], which is most a preferred converter to be used in the three-stage SST.

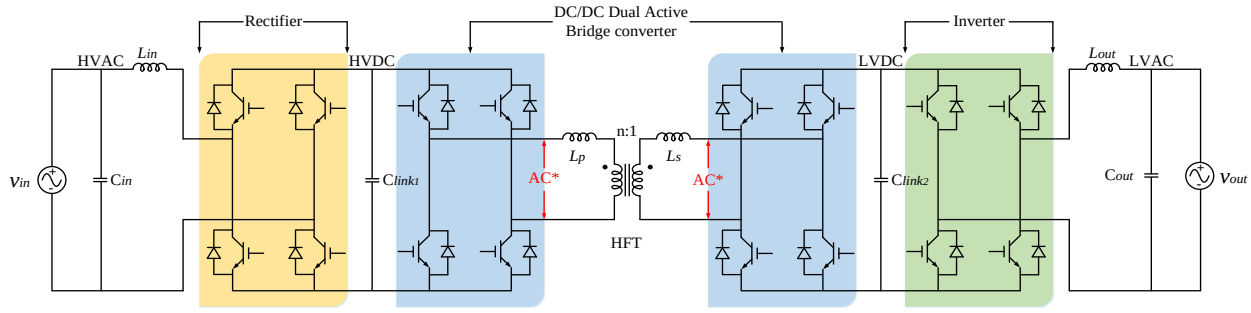


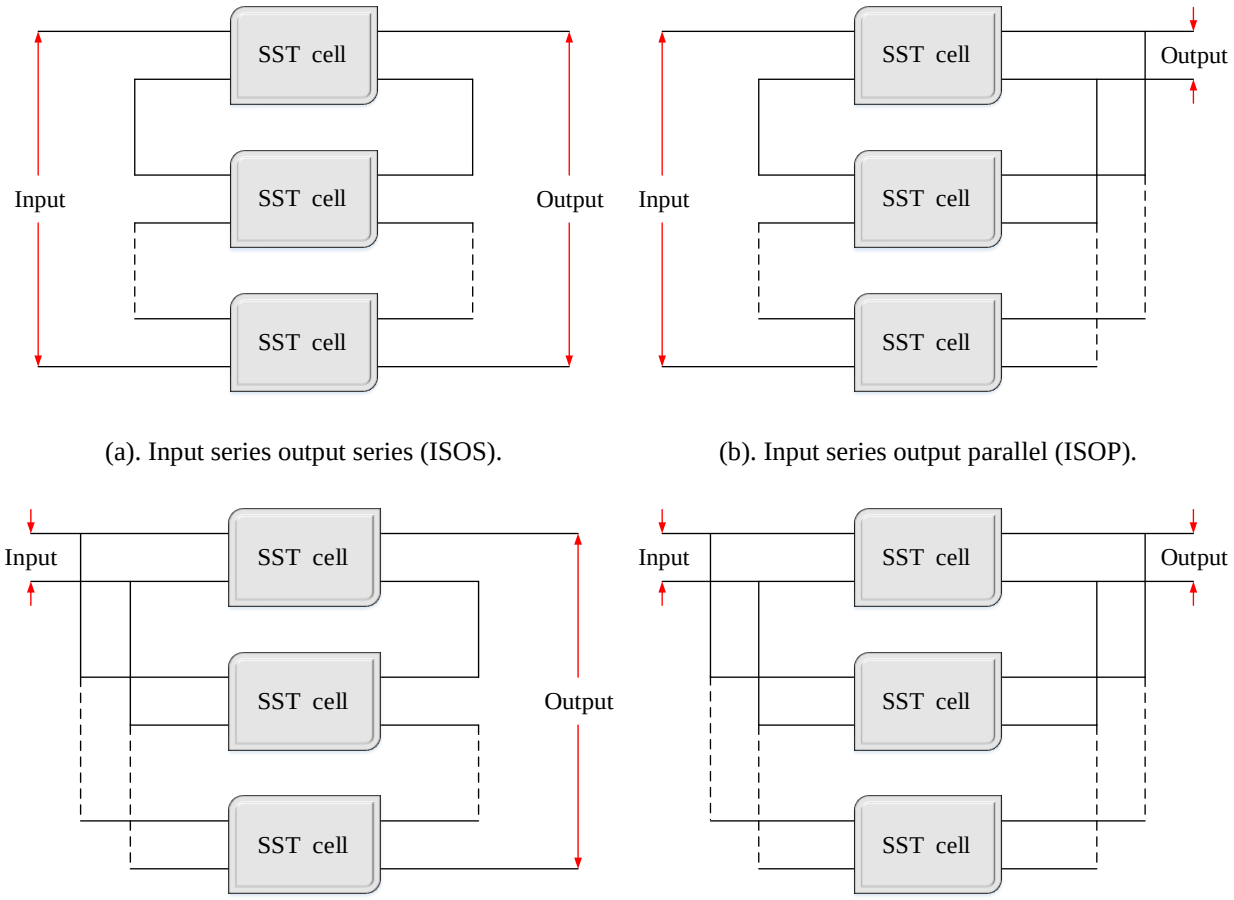
Figure 1.10. A three-stage SST based on a DC/DC dual active bridge (DAB) converter.

1.6 Connection of the Solid-State Transformers

The previous figures for solid-state transformers are for single-phase type with a single cell for each stage. However, a three-phase transformer is widely used in different stages of the power system distribution. A three-phase solid-state transformer can be implemented similar to a traditional power transformer.

The first option is a three-phase solid-state transformer based on three single-phase solid-state transformers with a single-cell for each stage. The three single-phase solid-state transformers are connected together in star connection or delta connection. In this topology, there is no direct contribution between the three phases as the power is transferred individually by each phase. This is considered a drawback of this topology because any electrical fault in any switch may lead to outage of whole phase [42]. Solving this issue requires using multilevel converters instated of using single-cell for each stage.

The second option is a three-phase solid-state transformer based on three single-phase solid-state transformers with a multilevel-cell for each stage. It is similar to the first option, but each stage in each phase consists of multilevel converters [17]. These stages can be connected by different ways, which are input series output series (ISOS), input series output parallel (ISOP), input parallel output series (IPOS), and input parallel output parallel (IPOP) [3, 43]. Figure 1.11 shows these different categories of the connections.



(a). Input series output series (ISOS).

(b). Input series output parallel (ISOP).

(c). Input parallel output series (IPOS).

(d). Input parallel output parallel (IPOP).

Figure 1.11. Connection of the solid-state transformers.

The third option is a three-phase solid-state transformer based on three single-phase solid-state transformers with a single/multi-cell for each stage. In this option, the first stage and the second one consist of multi-cell converters. They can be connected the same way as in the previous options. However, the DC/AC converter in the last stage consists of only one cell. It is extended to be a three-phase DC/AC converter (a three-phase inverter) because the input voltage of the last stage is always low voltage [44].

1.7 Objective of Dissertation

The SSTs have been evolving quickly for the past few decades from an abstract concept to a reliable contender for replacing conventional transformers in a wide range of applications that

demand less weight and volume, e.g. traction applications, or a higher level of controllability, e.g. renewable energy integration into smart grid. Several new topologies, control systems, and applications for SSTs have been proposed recently [3, 45]. Nevertheless, many key research challenges pertaining to the protection, isolation, reliability, and fault-tolerant operation of SSTs remain unanswered.

The purpose of this work is to propose a new solid-state transformer topology in conjunction with a fault-tolerant operation method that can be used to fully restore the transformer operation in the case of two types of common faults in SST applications, i.e. high voltage side switch faults and high voltage grid faults. The proposed SST topology is derived by introducing z-source circuitry into a well-known three-stage multilevel cascaded SST topology [17, 46-48]. This SST topology has a stiff low voltage DC bus that can be used for renewable energy integration and for a fully modular structure.

1.8 Problem Statement

This work proposes a fault-tolerant operation strategy for the proposed solid-state transformer that can revamp the faulty operation to the pre-fault conditions in the case of two distinct types of fault.

- The first fault type covered is a fault occurrence on one of the switches of the multilevel cascaded quasi-z-source inverter stage, which is termed a QZSI switch fault hereinafter [47].
- The second fault type covers the unbalanced voltage conditions on the high voltage AC grid side due to faults on the grid, which is termed a HVAC grid fault hereinafter [48].

The two types of faults studied in this work are illustrated in Figure 1.12 and Figure 1.13.

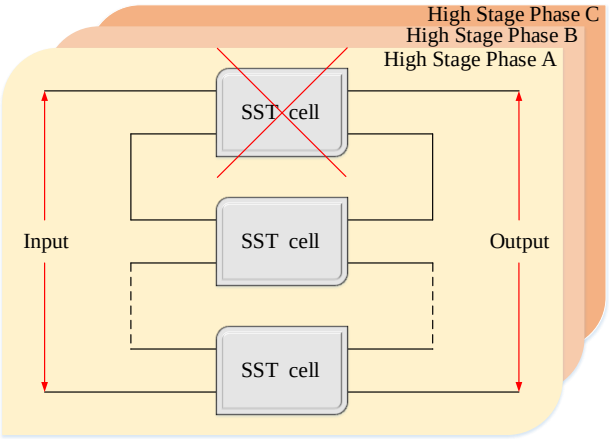


Figure 1.12. A quasi-z-source inverter switch fault (A QZSI switch fault).

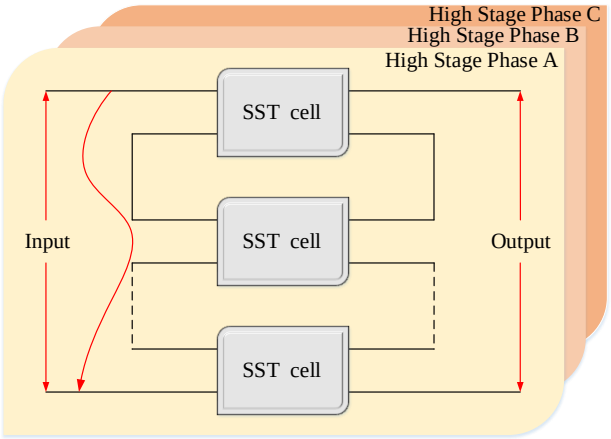


Figure 1.13. A high voltage AC grid fault (A HVAC grid fault).

1.9 Overview of Dissertation

As previously mentioned, in this research the new proposed SST topology will be designed to fully restore operation of the SST in the case of two types of common faults in SST applications. The rest of the dissertation is organized as follows.

In chapter 2, a brief introduction of quasi-z-source inverter topology, which will be used in a high voltage stage of the proposed SST, is provided. This part of the dissertation also presents the modulation method for the quasi-z-source inverter topology that will be used in the proposed SST. The analysis of the proposed fault-tolerant method is presented to provide the solution for the two types of faults. The difference between traditional methods and the proposed method is provided to prove the efficacy of the proposed modulation method.

In chapter 3, the proposed solid-state transformer topology is provided with detailed explanation of using quasi-z-source inverter topology in the high voltage stage of the proposed transformer. The analysis of the proposed fault-tolerant method to provide the solution for the two types of faults is presented and explained with its equations. Additionally, the controller design for

the output stage of the proposed solid-state transformer is carried out for synchronizing the output voltage to the grid and controlling the output power.

In chapter 4, simulation results using PLECS are presented to verify the effectiveness of the proposed solid-state transformer fault tolerant strategy.

In chapter 5, the conclusion of the dissertation and the future work are presented.

Chapter 2

2.1 Introduction

One of the most important solid-state transformers reliability issues is related to the high voltage stage. Different multi-level topologies are implemented for the primary side of the SSTs, since the input voltage is high. The high voltage in this stage is divided to low levels [13, 49]. Therefore, voltage the stress on all components will be lower as well. However, the high voltage stage is still suffering because of the stress in the divided voltage [49, 50]. The stress also may lead to different fault scenarios in this stage. In this research, a multilevel cascaded quasi-z-source inverter stage will be used in the high voltage stage.

2.2 Quasi-Z-Source Inverter Topology

The quasi-z-source inverter (QZSI) topology is a derived topology from the traditional voltage-source inverter (VSI). It is created by adding an impedance source network to the input of the traditional voltage-source inverter [51]. The impedance source network is comprised of two capacitors, two inductors, and one diode. It is a two-port network, which is added to prevent damaging the input source and inverter itself when the short circuit occurs. The time of short circuit is called shoot-through duty ratio [51-53]. The impedance source network provides an impedance source for the converter, and it is coupling the converter to the load [54]. It will also make the control of the output voltage more flexible by adding a new voltage boosting factor of the inverter

gain. This factor is used to boost the DC link voltage [51, 55-57], where this feature is important to the proposed solid-state transformer operation. Figure 2.1 shows a simple circuit of the single phase of the quasi-z-source inverter topology.

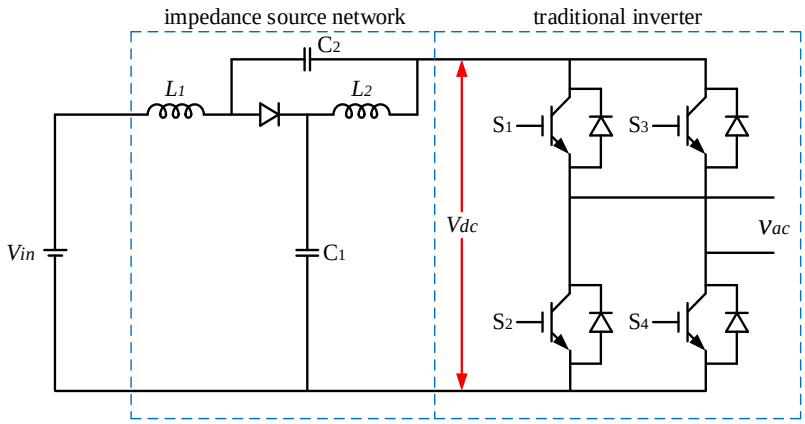


Figure 2.1. The quasi-z-source inverter (QZSI) topology.

The quasi-z-source inverter topology not only has all features of voltage-source inverter but also has unique advantages. The obtained AC output voltage can surpass the dc input voltage by implementing the new voltage boosting factor [51, 55, 57-60]. The input voltage and output voltage also have the same ground. The quasi-z-source inverter topology has simple control strategies, and it draws a constant current from the input. This advantage is very important and makes the quasi-z-source inverter topology more suitable to be implemented in the SST applications. It supports the proposed solid-state transformer with following features [51, 53, 55, 59, 61],

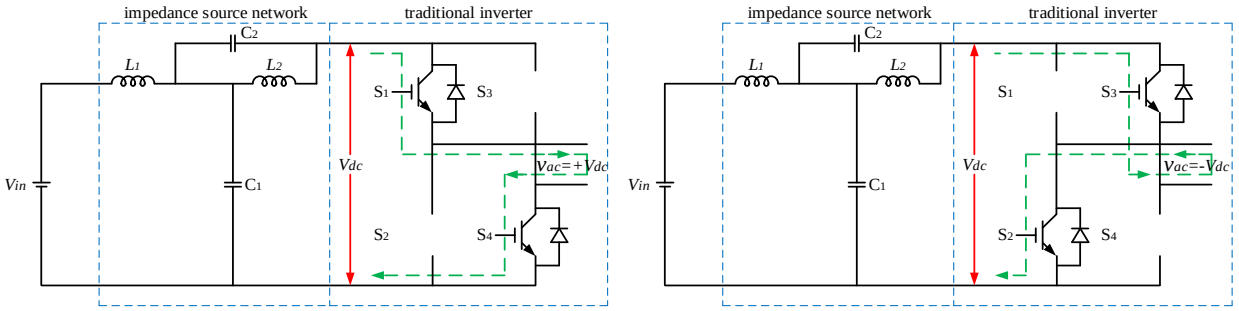
- Reducing the passive component rating.
- Decreasing the input-current THD.
- Reducing source stress as well as no need for extra filters.
- Making the proposed solid-state transformer more suitable for applications in PV systems.

2.3 Operation of Quasi-Z-Source Inverter Topology

The operation of quasi-z-source inverter topology is divided to two modes, which are an active mode and a shoot-through mode.

2.3.1 Active Mode (Non-Shoot-Through Mode)

In this mode, the quasi-z-source inverter topology operates the same as other voltage-source inverters, and it is controlled in the same manner. There is no more than one and only one switch in each leg turned on as an active switch, and these active switches are on different levels of each other. [52, 53]. Therefore, the input dc voltage source is available as a DC link voltage input to the inverter. The output voltage is either positive or negative [51-53, 58, 62, 63]. The circuits of the active mode are shown in Figure 2.2.

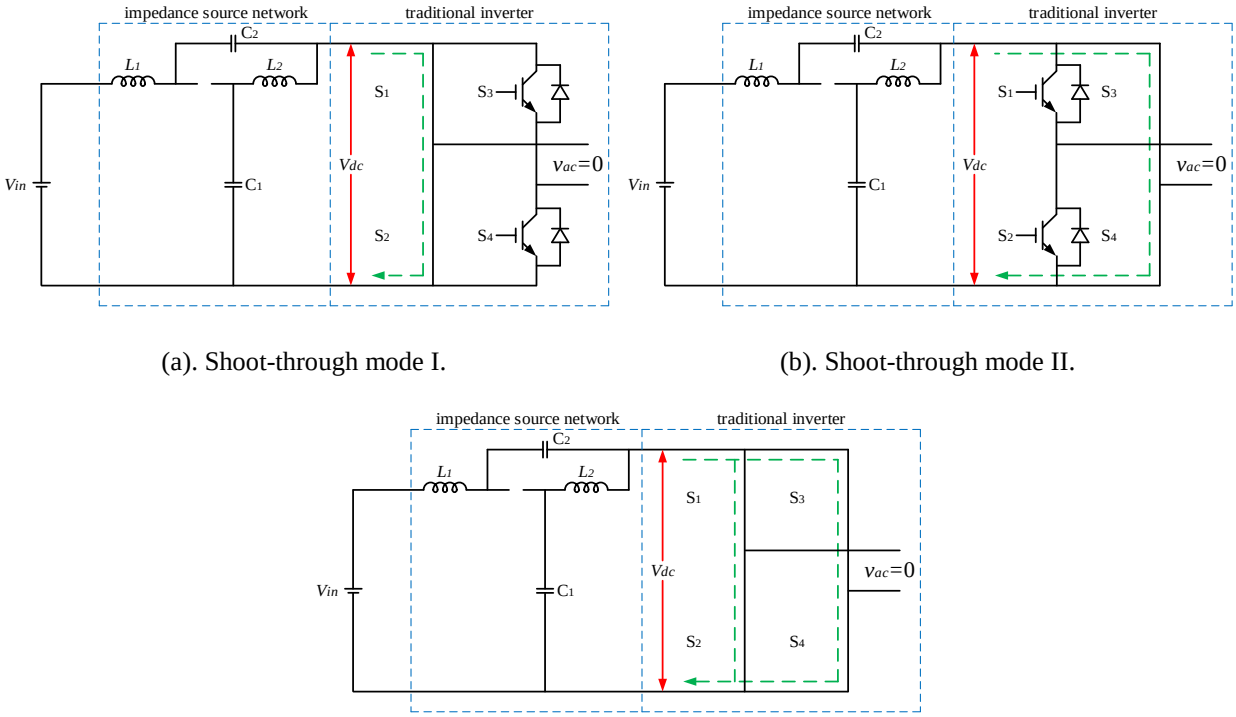


(a). Active mode I (positive output). (b). Active mode II (negative output).

Figure 2.2. Active mode of the quasi-z-source inverter circuit.

2.3.2 Shoot-Through Mode

In this mode, two switches in at least one leg are turned on for a short duration, and the diode is reverse biased. The DC link voltage is boosted by the voltage boosting factor. The value of the voltage boosting factor is a function of the shoot through. The voltage output of the inverter is always zero [51-53, 58, 62, 63]. The circuits of the shoot-through mode are shown in Figure 2.3 for the three different cases.



(a). Shoot-through mode I.

(b). Shoot-through mode II.

(c). Shoot-through mode III.

Figure 2.3. Shoot-through mode of the quasi-z-source inverter circuit.

The voltage through the impedance source network can be described in term of the input voltage and the DC link voltage (the internal input voltage). Hence, the voltage of two capacitors (V_{C_1} and V_{C_2}) and the input voltage to the quasi-z-source inverter topology (V_{in}) are expressed in [56, 63-65] as,

$$V_{C_1} = \frac{1-D}{1-2D} V_{in} \tag{2.1}$$

$$V_{C_2} = \frac{D}{1-D} V_{in} \tag{2.2}$$

where ($D = t_{sh}/T$) is the duty ratio of the shoot-through, t_{sh} is the duration time of the shoot-through, and T is the time period. As a result, the relationship between the DC link voltage (V_{dc}) and the input voltage to the quasi-z-source inverter topology (V_{in}) is formulated in [56, 63, 64] as,

$$V_{dc} = V_{C_1} + V_{C_2} = \frac{1}{1-2D} V_{in} \tag{2.3}$$

Therefore, the gain of the quasi-z-source inverter topology is obtained with multiplying (2.3) by $(1-D)/2$ and following next steps as,

$$\frac{(1-D)}{2} \times V_{dc} = \frac{(1-D)}{2} \times \frac{1}{1-2D} V_{in} \tag{2.4}$$

Reorganizing (2.4) as,

$$(1-D) \times \frac{V_{dc}}{2} = (1-D) \times \frac{1}{1-2D} \times \frac{V_{in}}{2} \tag{2.5}$$

Defining modulation index (*M*) as,

$$M = (1-D) \tag{2.6}$$

Also, by defining the voltage boosting factor (*B*) in [63, 64] as,

$$B = \frac{1}{1-2D} \tag{2.7}$$

Therefore, (2.4) can be formulated again as,

$$M \times (V_{dc}/2) = M \times B \times (V_{in}/2) \tag{2.8}$$

Finally, the gain of the quasi-z-source inverter topology (*G*) can be expressed as,

$$G = \frac{M \times (V_{dc}/2)}{(V_{in}/2)} = \frac{v_{ac}}{(V_{in}/2)} = M \times B \tag{2.9}$$

Also, by careful inspection of (2.9), it can be realized the shoot-through duty ratio (*D*) can be formulated as a function of the gain of the quasi-z-source inverter topology (*G*) as,

$$D = \frac{(G-1)}{(2G-1)} \tag{2.10}$$

Based on the voltage boosting factor (*B*) formula in (2.7), the factor becomes bigger and bigger as soon as the shoot-through duty ratio (*D*) approaches 0.5. This is an ideal operation of the quasi-

z-source inverter topology. In reality, the voltage boosting factor cannot be infinity because of the limitation of the modulation index (*M*). The higher voltage boosting factor has to be implemented, the smaller modulation index has to be designed as in (2.6) *D*=1-*M*.

2.4 Control of Quasi-Z-Source Inverter Topology

Different modulation methods have been used to generate the required states to control multilevel cascaded quasi-z-source inverter stage. One of the common methods is traditional pulse width modulation (PWM) [66, 67]. As it was explained earlier, the quasi-z-source inverter topology has a new different state operation which is a shoot-through state. However, the shoot-through state cannot be generated by using the traditional PWM. The pluses for each of the two switches in the same phase leg cannot have the same state. They must be always opposite each other. Therefore, including the shoot-through state in traditional PWM is necessary to make it suitable to control the quasi-z-source inverter topology. According to [68], the adjustment can be archived by adding a new switching signal in three different forms to implement the shoot-through. They are a simple boost control, a maximum boost control, and a maximum constant boost control [64]. However, these methods are suitable for the three-phase quasi-z-source inverter topologies with three legs more than the single-phase inverters with two legs. The boost control and the maximum constant boost control were modified properly to be suitable to control the single-phase quasi-z-source inverter [69]. However, the maximum boost control will be modified in this part of the research. Also, a new proposed method will be introduced and explained to improve the reliability and the dynamic response of the proposed solid-state transformer response.

2.4.1 Simple Boost Control (SBC)

In this method, two reference signals are implemented by using two sinusoidal waves. The phase shift between the reference signals is 180^{o}. The carrier signal is implemented by using a high

frequency triangle wave same as the traditional PWM technique. Also, the shoot-thought is implemented by using two signals in the form of straight lines. One is used to employ the positive value, and the other one is for the negative value [68, 69]. The details of this technique are shown in Figure 2.4.

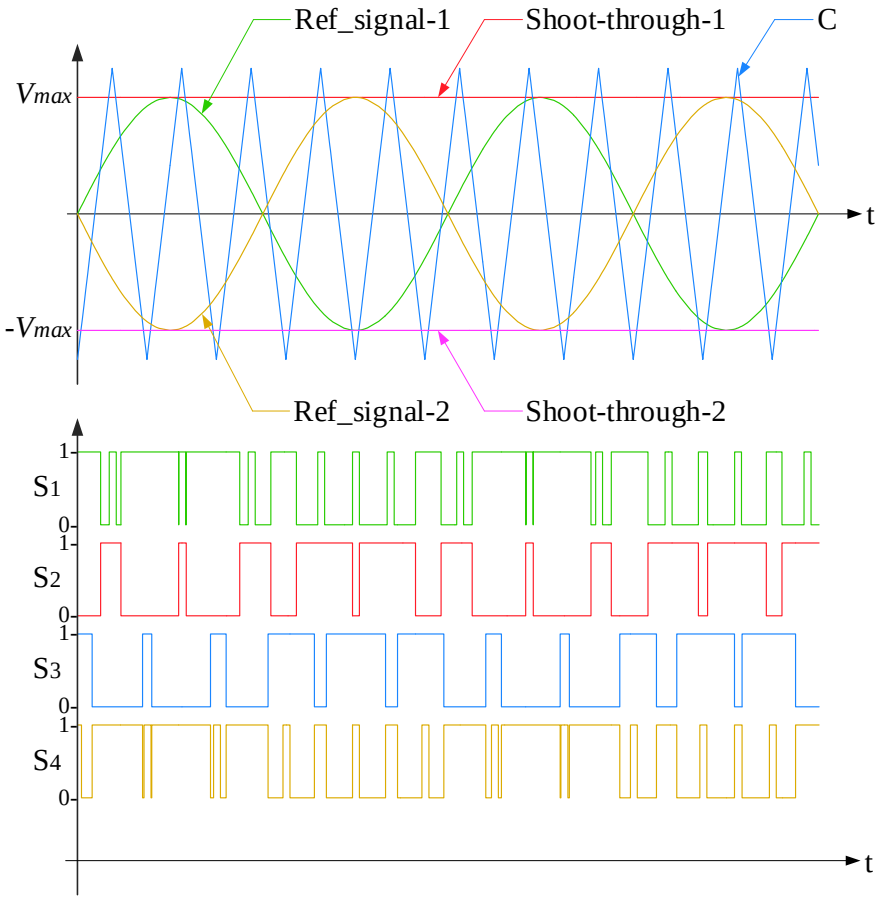


Figure 2.4. Simple boost control for the single quasi-z-source inverter topology.

The active mode: In this mode, the switching states are generated in the same manner as the traditional PWM technique. The two reference signals are compared with the carrier signal. The switching states for switch S_1 are generated whenever the first reference signal (Ref_signal-1) is higher than the carrier signal (C), but the switching states for switch S_2 are generated whenever the first reference signal (Ref_signal-1) is lower than the carrier signal (C). The switching states for switches S_3 and S_4 are generated similarly, but the second reference signal (Ref_signal-2) is

compared to the carrier signal (C) [68, 69]. All switching states for the active mode are summarized in Table 2-1.

Table 2-1: The simple boost control (SBC) switching states of the active mode

Reference Signal	Comparison	Carrier	Active Switch
Ref_signal-1	>	C	S_1
Ref_signal-1	<	C	S_2
Ref_signal-2	>	C	S_3
Ref_signal-2	<	C	S_4

The shoot-through mode: In this mode, the carrier signal is compared with the two straight-lines. The first shoot-through states for switch S_1 are generated whenever the carrier signal (C) is higher than the positive straight-line (Shoot-through-1). However, the other shoot-through states for switch S_4 are generated whenever the carrier signal (C) is lower than the negative straight-line (Shoot-through-2). Therefore, the shoot-through states cannot be generated in the same time for two switches in the same phase leg [54, 68-71]. All shoot-through states for the shoot-through mode are summarized in Table 2-2.

Table 2-2: The simple boost control (SBC) shoot-through states of the shoot-through mode

Carrier	Comparison	Shoot-through	Active Switch
C	>	$+V_{max}$	S_1
C	<	$-V_{max}$	S_4

2.4.2 Maximum Constant Boost Control (MCBC)

In this method, two reference signals are implemented by using two sinusoidal waves. The phase shift between the reference signals is 180^o. The carrier signal is implemented by using a high frequency triangle wave same as the traditional PWM technique. Also, the shoot-through is maintained to be a constant value. It is obtained by using two signals in the form of envelopes.

One is used to employ the positive value, and the other one is for the negative value [69, 72]. The details of this technique are shown in Figure 2.5.

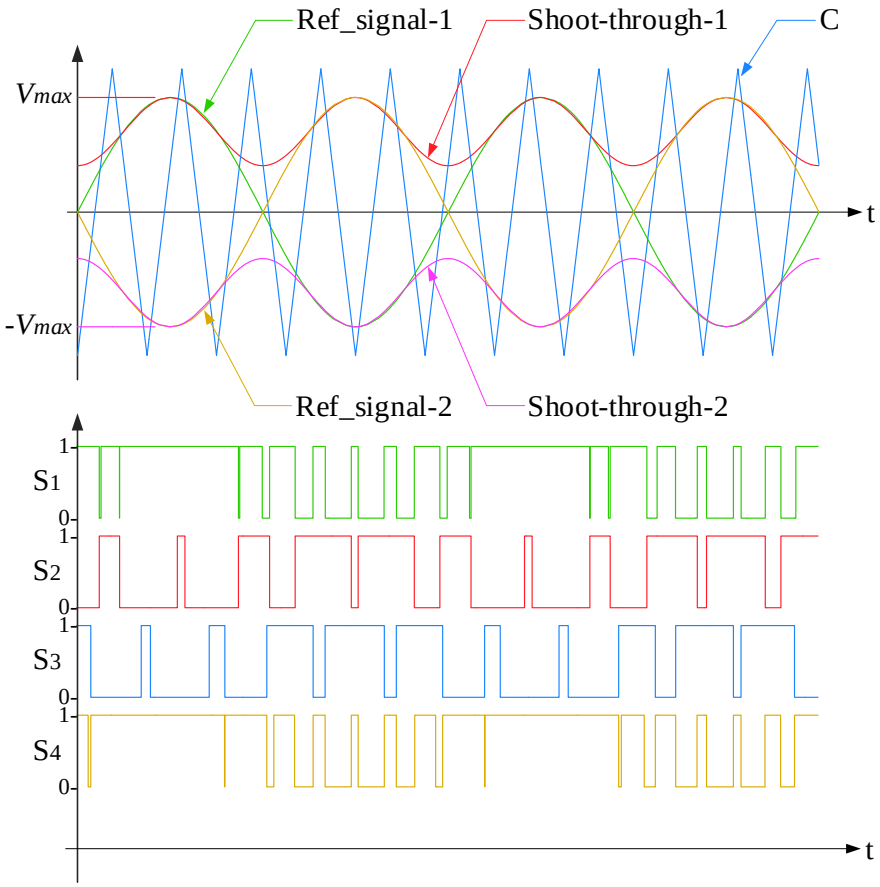


Figure 2.5. Maximum constant boost control for the single quasi-z-source inverter topology.

The active mode: In this mode, the switching states are generated in the same manner as the traditional PWM technique. The two reference signals are compared with the carrier signal. The switching states for switch S_1 are generated whenever the first reference signal (Ref_signal-1) is higher than the carrier signal (C), but the switching states for switch S_2 are generated whenever the first reference signal (Ref_signal-1) is lower than the carrier signal (C). The switching states for switches S_3 and S_4 are generated similarly, but the second reference signal (Ref_signal-2) is compared to the carrier signal (C) [69, 72, 73]. All switching states for the active mode are summarized in Table 2-3.

Table 2-3: The maximum constant boost control (MCBC) switching states of the active mode

Reference Signal	Comparison	Carrier	Active Switch
Ref_signal-1	>	C	S_1
Ref_signal-1	<	C	S_2
Ref_signal-2	>	C	S_3
Ref_signal-2	<	C	S_4

The shoot-through mode: In this mode, the carrier signal is compared with the two envelopes. The first shoot-through states for switch S_1 are generated whenever the carrier signal (C) is higher than the positive envelope (Shoot-through-1). However, the other shoot-through states for switch S_4 are generated whenever the carrier signal (C) is lower than the negative envelope (Shoot-through-2). Therefore, the shoot-through states cannot be generated in the same time for two switches in the same phase leg [54, 69, 72]. All shoot-through states for the shoot-through mode are summarized in Table 2-4.

Table 2-4: The maximum constant boost control (MCBC) shoot-through states of the shoot-through mode

Carrier	Comparison	Shoot-through	Active Switch
C	>	Shoot-through-1	S_1
C	<	Shoot-through-2	S_4

2.4.3 Modified Maximum Boost Control (MSBC)

In this method, two reference signals are implemented by using two sinusoidal waves. The phase shift between the reference signals is 180^o. The carrier signal is implemented by using a high frequency triangle wave same as the traditional PWM technique [72]. Also, the shoot-through is implemented by using the same reference signals in opposite order. One is used to employ the positive value, and the other one is for the negative value. The details of this technique are shown in Figure 2.6.

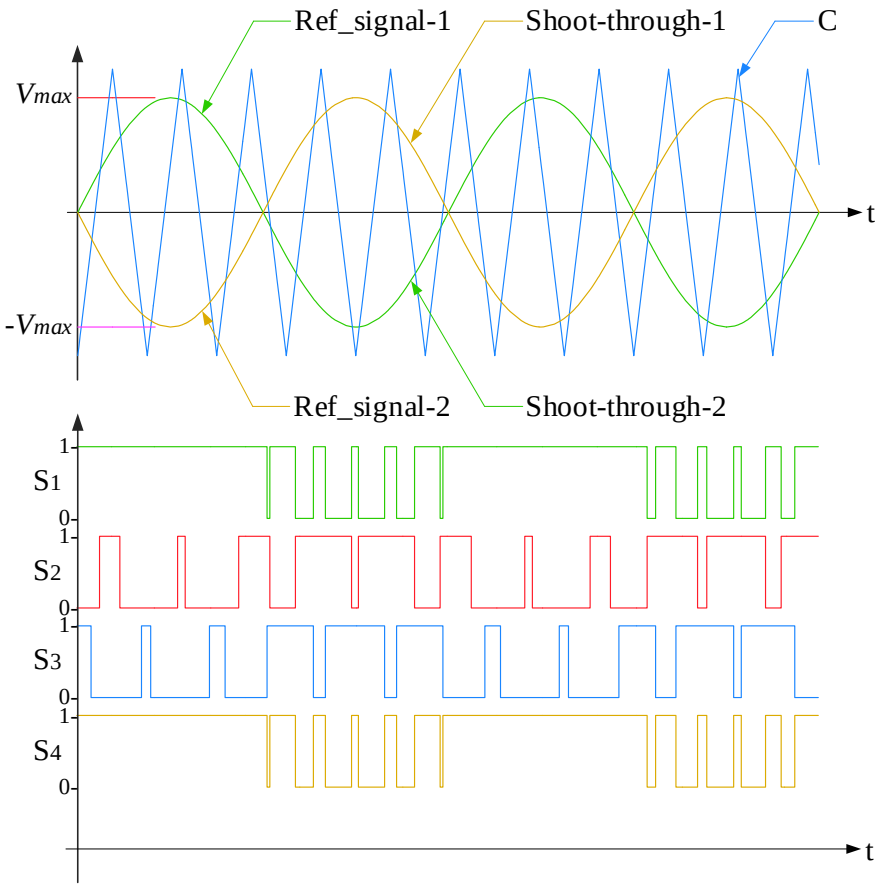


Figure 2.6. Modified maximum boost control for the single quasi-z-source inverter topology.

The active mode: In this mode, the switching states are generated in the same manner as the traditional PWM technique. The two reference signals are compared with the carrier signal. The switching states for switch S_1 are generated whenever the first reference signal (Ref_signal-1) is higher than the carrier signal (C), but the switching states for switch S_2 are generated whenever the first reference signal (Ref_signal-1) is lower than the carrier signal (C). The switching states for switches S_3 and S_4 are generated similarly, but the second reference signal (Ref_signal-2) is compared to the carrier signal (C) [72-74]. All switching states for the active mode are summarized in Table 2-5.

Table 2-5: The modified maximum boost control (MSBC) switching states of the active mode

Reference Signal	Comparison	Carrier	Active Switch
Ref_signal-1	>	C	S_1
Ref_signal-1	<	C	S_2
Ref_signal-2	>	C	S_3
Ref_signal-2	<	C	S_4

The shoot-through mode: In this mode, the carrier signal is compared with the same reference signals in opposite order. The first shoot-through states for switch S_1 are generated whenever the carrier signal (C) is higher than the second reference signal (Shoot-through-1). However, the other shoot-through states for switch S_4 are generated whenever the carrier signal (C) is lower than the first reference signal (Shoot-through-2). Therefore, the shoot-through states cannot be generated in the same time for two switches in the same phase leg [54, 70-72, 74]. All shoot-through states for the shoot-through mode are summarized in Table 2-6.

Table 2-6: The modified maximum boost control (MSBC) shoot-through states of the shoot-through mode

Carrier	Comparison	Shoot-through	Active Switch
C	>	Ref_singnal-2	S_1
C	<	Ref_singnal-1	S_4

2.4.4 Proposed Modulation Method Control (PMMC)

Since the proposed solid-state transformer stage consists of the multilevel cascaded quasi-z-source inverter topology, hence the modulation of this stage can be implemented by modifying the traditional PWM.

In this research, implementing traditional phase shifted pulse width modulation (PS-PWM) is more suitable for the fault-tolerant technique to balance the output again. However, it has to be modified to generate the shoot-through states as well as the normal states [47, 48]. The traditional

PS-PWM has one reference signal which is implemented by using a sinusoidal wave. The two carrier signals are implemented by using two high frequency tringle waves. The phase shift between the carriers are 180^{o} [75, 76]. The traditional PS-PWM is modified by adding one more signal in the form of a straight line to generate the shoot-through states [47, 48]. The simulation circuit of the switching logic in PLECS and the details of this technique are shown in Figure 2.7 and Figure 2.8.

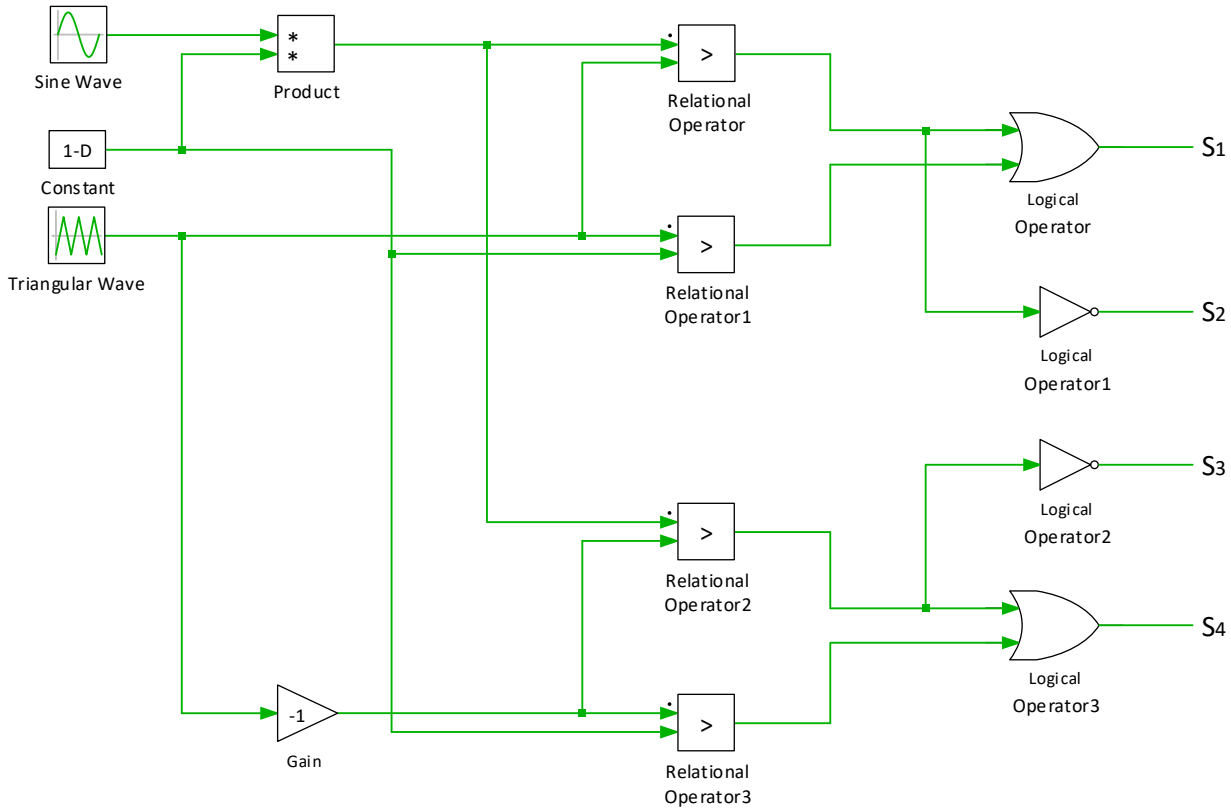


Figure 2.7. The simulation circuit for the switching logic in PLECS of the proposed modulation method control for the single quasi-z-source inverter topology.

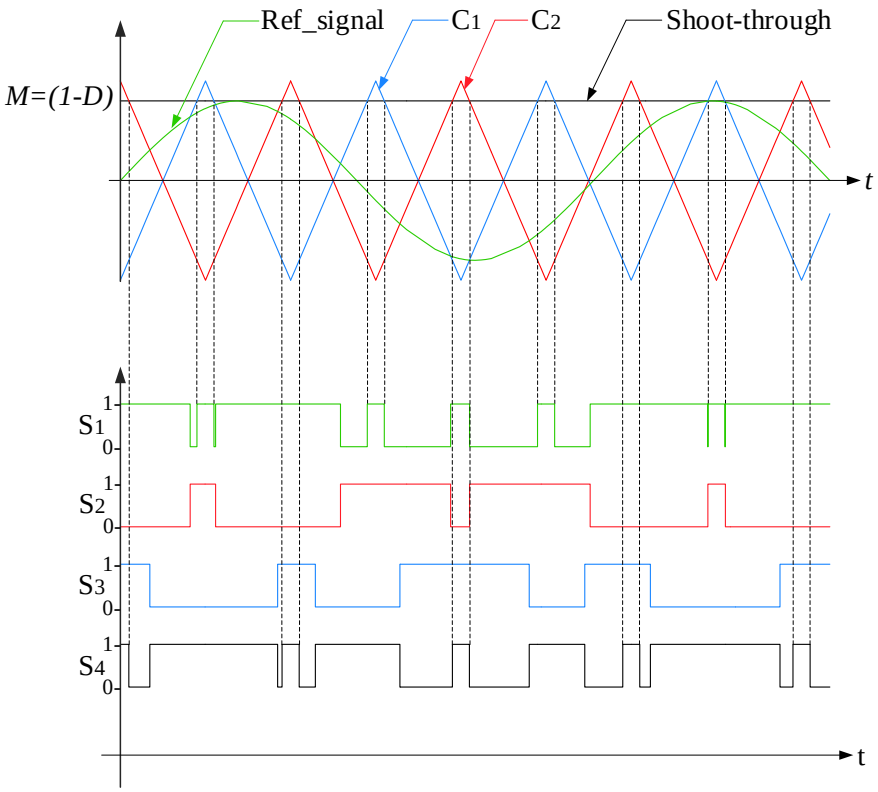


Figure 2.8. Proposed modulation method control for the single quasi-z-source inverter topology.

The active mode: In this mode, the switching states are generated in the same manner as the traditional PWM technique [47, 48, 77]. The reference signal is compared with the two carrier signals. The switching states for switch S_1 are generated whenever the reference signal (Ref_signal) is higher than the first carrier signal (C_1), but the switching states for switch S_2 are generated whenever the reference signal (Ref_signal) is lower than the first carrier signal (C_1). The switching states for switches S_4 and S_3 are generated similarly, but the reference signal (Ref_signal) is compared to the second carrier signal (C_2) [47, 48, 77]. All switching states for the active mode are summarized in Table 2-7.

Table 2-7: The proposed modulation method control (PMMC) switching states of the active mode

Reference Signal	Comparison	Carrier	Active Switch
Ref_signal	>	C_1	S_1
Ref_signal	<	C_1	S_2
Ref_signal	>	C_2	S_4
Ref_signal	<	C_2	S_3

The shoot-through mode: In this mode, the two carrier signals are compared with the straight-line. The first shoot-through states for switch S_1 are generated whenever the first carrier signal (C_1) is higher than the straight-line (Shoot-through). However, the other shoot-through states for switch S_4 are generated whenever the second carrier signal (C_2) is higher than the straight-line (Shoot-through). Therefore, the shoot-through states cannot be generated in the same time for two switches in the same phase leg [47, 48, 77]. All shoot-through states for the shoot-through mode are summarized in Table 2-8.

Table 2-8: The proposed modulation method control (PMMC) shoot-through states of the shoot-through mode

Carrier	Comparison	Shoot-through	Active Switch
C_1	>	$M=(1-D)$	S_1
C_2	>	$M=(1-D)$	S_4

Chapter 3

3.1 The Proposed Three-Phase Solid-State Transformer Topology

The proposed three-phase solid-sate transformer presents a new topology to improve the reliability of the high voltage stage. A multilevel cascaded quasi-z-source inverter topology will be used in the high voltage stage [47, 48]. According to the classification of the solid-state transformers explained in the introduction of this research, the proposed solid-state transformer is considered as a three-phase solid-state transformer with three stages with two DC links. The proposed topology is illustrated in Figure 3.1. The proposed topology is comprised of the input stage, the isolation stage including the high frequency transformer, and the output stage [47, 48].

3.1.1 The Input Stage

The input stage uses a multilevel cascaded h-bridge (CHB) topology with bidirectional power flow capability to convert the 60 Hz AC voltage from the high voltage AC (HVAC) grid side into DC. Therefore, the three-phase input AC voltage is converted to DC voltage by using an AC/DC multilevel cascaded h-bridge converter in each stage separately [47, 48]. This implementation is applied when the direction of supplied power is from the grid to the customers, where it works as a rectifier. However, the input stage can work as a DC/AC multilevel cascaded h-bridge converter, which means it can be implemented as an inverter when the direction of the power from the customer points back to the grid [47, 48].

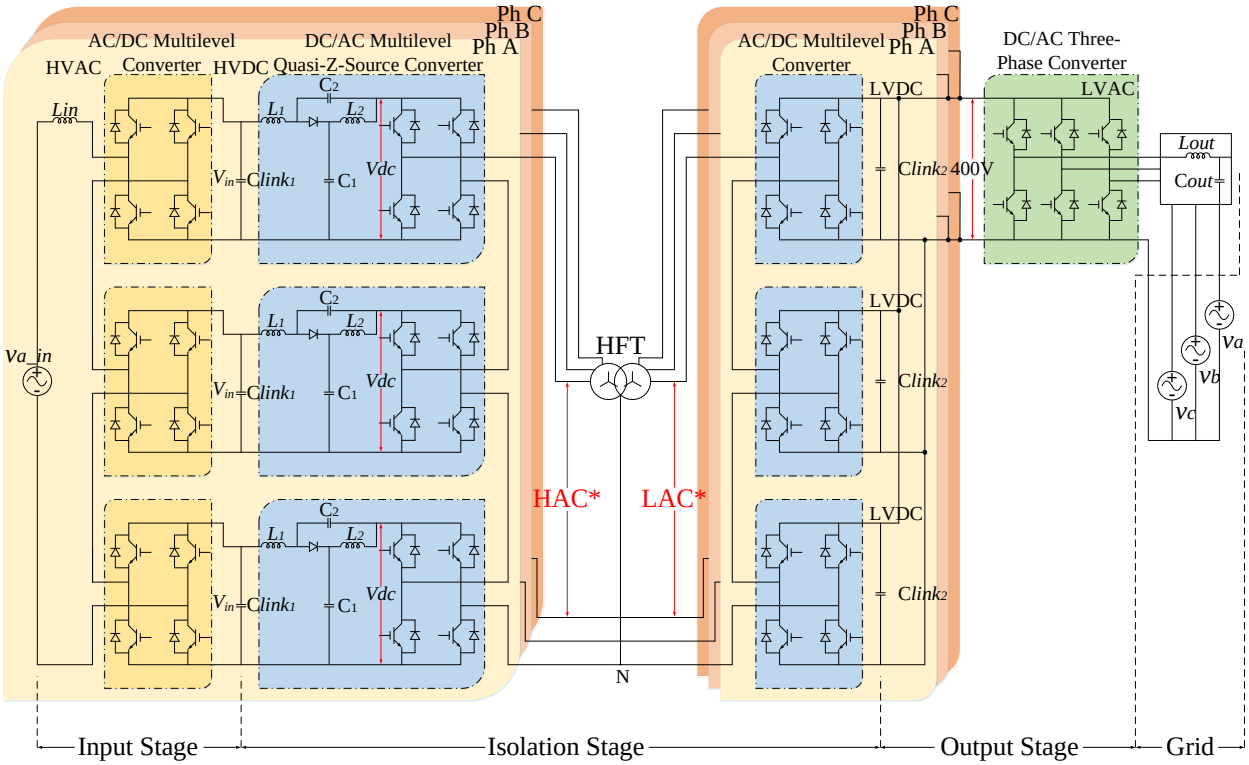


Figure 3.1. The proposed SST topology comprising the QZSI circuitry for fault-tolerant operation.

3.1.2 The Isolation Stage

The isolation stage is divided by the high frequency three-phase transformer to a high voltage side and a low voltage side. In this work, the use of a quasi-z-source inverter topology is proposed for the high voltage side of the isolation stage, which will be leveraged to implement the proposed fault-tolerant strategy [47, 48]. The proposed stage is working as a DC/AC multilevel cascaded h-bridge converter. It is connected to the primary side of the transformer, and the input of the transformer is high voltage with high frequency. Then the generated high frequency AC voltage by the multilevel cascaded quasi-z-source inverter stage is stepped down by the transformer. Finally, the second part of the isolation stage is designed as an AC/DC multilevel cascaded h-bridge converter. Therefore, the output voltage will be subsequently converted to a low DC voltage at the low voltage side. The isolation stage provides bidirectional power flow capability as well [47, 48].

3.1.3 The Output Stage

The output stage uses a conventional three-phase inverter because the input voltage level to this stage is low. This stage works as an inverter to synchronize the output of the proposed transformer to the grid at the customer points. Therefore, the 60 Hz AC output voltage from this stage is filtered and synchronized to the grid voltage. This is applied when the direction of the power is from the grid to the customers [47, 48]. However, this stage also provides bidirectional power flow capability. Therefore, it may also be implemented as an AC/DC three-phase converter if the direction of the power is from the customers back to the grid. The power factor of the injected power to the grid can be controlled using the output stage control circuitry as well. As a result of this, the supplied active and reactive power can be controlled [47, 48].

The multilevel cascaded quasi-z-source inverter stages illustrated in Figure 3.1 shows only three h-bridge cells in each phase as a case study. However, the proposed fault-tolerant topology can be implemented on a similar SST topology with higher number of h-bridge cells in each phase.

3.2 Fault Types

The proposed solid-state transformer in this research will be studied under different fault conditions to revamp the faulty operation to the pre-fault operation.

3.2.1 Quasi-Z-Source Inverter Switch Faults (QZSI Switch Faults)

The first fault type covered is a fault occurrence on one of the switches of the multilevel cascaded quasi-z-source inverter stage and termed a QZSI switch fault hereinafter. The switches of h-bridges in this stage are under very high voltage stress and thus vulnerable to faults. A faulty switch can become permanently open-circuit or permanently short-circuit based on the fault conditions [78]. In either case, the h-bridge with a faulty switch needs to be bypassed altogether using other functional switches, in order to ensure generation of symmetrical AC voltages at the

output of this stage [79-82]. Nevertheless, this will reduce the generated voltage level in the faulty phase significantly, and results in unbalanced three phase voltages are fed to the three-phase transformer [47]. Figure 3.2(a), (b), and (c) demonstrate the phasor diagram of the voltages for the healthy operation vs. faulty operation of the proposed solid-sate transformer shown in Figure 3.1 for a single QZSI switch fault in phase "a".

3.2.2 High Voltage AC Grid Faults (HVAC Grid Faults)

The second fault type covers the unbalanced voltage conditions on the high voltage AC grid faults (HVAC) grid side due to faults on the grid and termed HVAC grid faults hereinafter. Various types of faults (single line-to-ground, line-to-line, and etc.) over the HVAC grid can result in unbalanced voltages are fed to the three-phase solid-state transformer. In turn, the rectified voltages by the input stage will be unequal along the three phases. This will result in unbalanced voltages at the input of the multilevel cascaded quasi-z-source inverter stage, and eventually unbalanced high frequency three phase voltages are fed to the transformer. In this scenario, the multilevel cascaded quasi-z-source inverter stage can reach all of switching stages, however, the voltage steps between different levels will be unequal [48]. Figure 3.3(a), (b), and (c) demonstrate the phasor diagram of the voltages for the healthy operation vs. faulty operation of the proposed solid-sate transformer shown in Figure 3.1 for a single line-to-ground HVAC grid fault in phase "a".

3.3 The Operations of the Proposed Solid-State Transformer

3.3.1 Healthy Operation

The internal input-voltage to each h-bridge cell in the multilevel cascaded quasi-z-source inverter stage is termed as V_{dc} hereinafter. Accordingly, the output voltage for each h-bridge cell can be made equal to $-V_{dc}$, 0, or $+V_{dc}$ through switching [47, 48, 83-85].

As a result, the output voltage of each phase of the multilevel cascaded quasi-z-source inverter stage can have seven voltage levels of $-3V_{dc}$, $-2V_{dc}$, $-V_{dc}$, 0, $+V_{dc}$, $+2V_{dc}$, and $+3V_{dc}$ [47, 83-85]. Therefore, by proper switching, seven level high frequency AC phase voltages can be generated using the multilevel cascaded quasi-z-source inverter stage [47, 48]. The resulting line-to-line voltage phasors are shown in Figure 3.2(a), and they are formulated based on phase voltages using,

$$V_{ab}^{\ 2} = V_a^{\ 2} + V_b^{\ 2} - 2V_aV_b\cos(\theta_{ab}) \tag{3.1}$$

$$V_{bc}^{\ 2} = V_b^{\ 2} + V_c^{\ 2} - 2V_bV_c\cos(\theta_{bc}) \tag{3.2}$$

$$V_{ca}^{\ 2} = V_c^{\ 2} + V_a^{\ 2} - 2V_cV_a\cos(\theta_{ca}) \tag{3.3}$$

$$\theta_{ab} + \theta_{bc} + \theta_{ca} = 360^{o} \tag{3.4}$$

By normalizing the phase voltages to V_{dc}, the amplitude of the phase voltages for the proposed solid-sate transformer shown in Figure 3.1 will be equal to $V_a = V_b = V_c =$ 3 p.u. in the healthy condition. Substituting these values into (3.1)-(3.3) and assuming balanced operation in the healthy condition, i.e. $\theta_{ab} = \theta_{bc} = \theta_{ca} = 360^{o}/3 = 120^{o}$, results in balanced line-to-line voltages of $V_{ab} = V_{bc} = V_{ca} =$ 5.1962 p.u .

According to [63] the V_{dc} voltage for each h-bridge cell in the multilevel cascaded quasi-z-source inverter stage can be boosted by increasing the voltage boosting factor of the z-source circuitry through increasing the shoot-through duty ratio for each h-bridge. However, increasing the shoot-through duty ratio, increases the voltage stress ($+\Delta$ stress%) over h-bridge switches and needs to be done conservatively. The increased stress is calculated based on,

$$+\Delta\, stress\% = \frac{B_{new} - B_{HO}}{B_{HO}} \times 100\% \tag{3.5}$$

where B_{new} is the voltage boosting factor for the new operation, and B_{OH} is the voltage boosting factor for the healthy operation, which will be used as a reference for all other different operation conditions. Also, the new value of inverter gain in the faculty condition can then be calculated by using,

$$G_{new} = F_{NO} \times G_{HO} \tag{3.6}$$

where G_{HO} is the inverter gain in healthy operation, and F_{NO} is the fault gain in the new operation.

In the healthy operation and based on (3.6), the fault gain (F_{NO}) must equal to 1.00. Therefore, the value of the new inverter gain (G_{new}) is the same as the inverter gain in healthy operation (G_{HO}). In the case of study healthy operation with modulation index (*M*) equals to 0.75, and the shoot-through duty ratio (*D*) equals to 0.25. As a result of this, the value of the new inverter gain will be $G_{new} = G_{HO}$ = 1.50, and the voltage boosting factor will be $B_{new} = B_{HO}$ = 2.00. Therefore, there will be no increased stress ($+\Delta$ stress% = +0.00%) because the proposed solid-sate transformer is operated in healthy operation.

3.3.2 Faulty Operation

Based on the type of fault and the number of the faulty switches in the multilevel cascaded quasi-z-source inverter stage, the output terminal voltage levels ($-V_{dc}$, 0, or $+V_{dc}$) will not be generated by the faulty multilevel cascaded quasi-z-source inverter stage cells. As a result, the generated phase voltages by h-bridge that has faulty cells are no longer symmetric around the zero-volt level. Therefore, the generated phase voltage by the faulty phase of the multilevel cascaded quasi-z-source inverter stage will be unbalanced because of the dc offset components [47].

In order to restore the healthy operation, the first step in the faulty operation is preventing the generation of the dc offset by bypassing all of the faulty multilevel cascaded quasi-z-source

inverter stage cells to make the generated phase voltages symmetric around zero-volt level. However, the amplitude of the new generated voltages by all of the three phases is not the same. The phases with bypassed cells (phase “a” in a case study) are no longer able to generate all of the voltage levels. Therefore, the amplitude of the generated voltages by these phases (phase “a”) will be lower than the amplitude of the other healthy phases (phase “b” and phase “c”) [47].

In the second step, to balance the generated voltage to the pre-fault condition in the faulty operation, there will be two different proposed methods that will be explained in this research under the two different aforementioned type of faults. They are the alternative method and the proposed fault-tolerant strategy method.

3.4 Implementing Alternative Method Solution for Faults

For the two previous faults, one immediate solution imagined is to increase the shoot-through duty ratio of the remaining healthy h-bridges in phase “a” of the multilevel cascaded quasi-z-source inverter stage to restore the “a” phase voltage to the pre-fault conditions. However, this solution increases the voltage stress over the healthy switches in the phase “a” considerably and can lead to more switch failures. Also, the inductor currents in all remaining healthy cells in the phase “a” will be increased considerably as well. However, to fully recover the faulty operation by increasing the shoot-through of the phase “a” for a faulty switch in phase “a”, the fault gain (F_{NO}) is formulated as,

$$F_{NO} = \frac{N_{THC}}{N_{RHC}} \tag{3.7}$$

where N_{THC} is the total number of healthy cells in phase “a”, and N_{RHC} is the remaining healthy cells in phase “a”.

3.4.1 Rebalancing Quasi-Z-Source Inverter Switch Faults (QZSI Switch Faults) Using the Alternative Method

In the case of a QZSI switch fault, with only one faulty switch in phase "a" of the proposed transformer shown in Figure 3.1, the generated phase voltages will be unbalanced, i.e. $V_a' = 2$ p.u, $V_b = 3$ p.u, and $V_c = 3$ p.u. This will also result in unbalanced line-to-line voltages of $V_{bc}' = 5.1962$ p.u and $V_{ab}' = V_{ca}' = 4.3589$ p.u . Therefore, balancing the line-to-line voltages again requires a new method to calculate the fault gain (F_{NO}) in order to increase the line-to-line voltages to their pre-fault values.

It should be noted that the proposed solid-state transformer shows only three h-bridge cells in each phase, which means the total number of healthy cells in phase "a" (N_{THC}) is equal to 3. Also, for a faulty switch in one cell in phase "a", the remaining healthy cells in phase "a" (N_{RHC}) are equal to 2. As a result of this, the fault gain (F_{NO}) is found as 1.50. Therefore, the value of the new inverter gain (G_{new}), the shoot-through duty ratio (D), and the modulation index (M) will be set to 2.25, 0.36, and 0.64 respectively. Also, the voltage boosting factor (B_{new}) will be set to 3.57, which means the increased stress will be equal to ($+\Delta$ stress% = +78.50%). However, because the voltage stress is high, it is required to resolve this type of faults with low stress using another proposed method. The new proposed method will be described further down in the end of this chapter. The phasor diagram of the voltages for the healthy operation vs. rebalanced post-fault operation using the alternative method for a single QZSI switch fault in phase "a" is demonstrated in Figure 3.2(d).

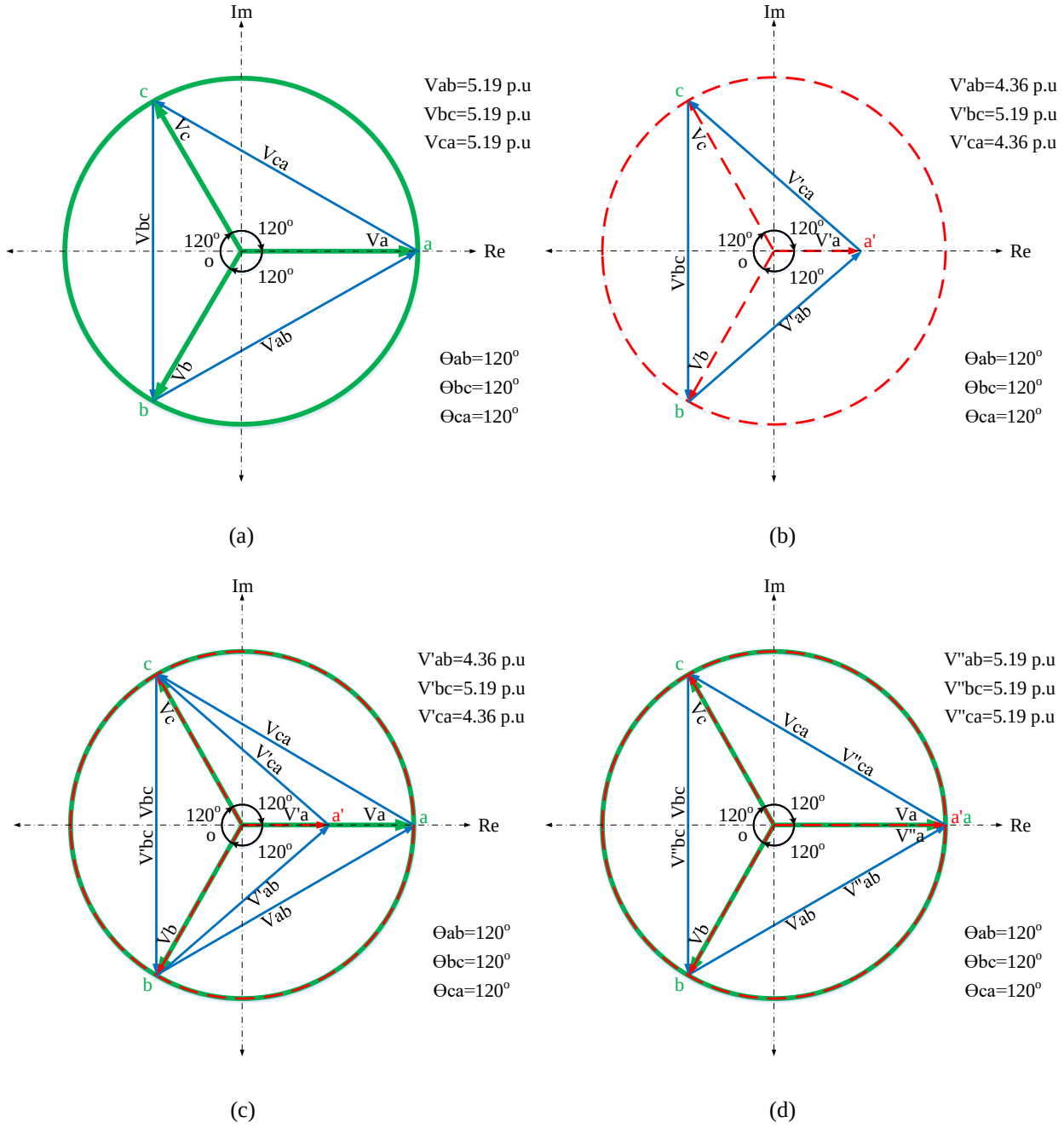


Figure 3.2. Phasor diagrams of the phase and line-to-line voltages for the high voltage side of the isolation stage in the proposed SST: (a) healthy SST operation, (b) a single QZSI switch fault in phase “a”, (c) the healthy operation vs. the faulty operation, and (d) rebalancing line-to-line voltages using the alternative method.

3.4.2 Rebalancing High Voltage AC Grid Faults (HVAC Grid Faults) Using the Alternative Method

In the case of faults on the HVAC grid side, the amplitude of three phase voltages is fed to the input stage of the proposed solid-state transformer will be dependent on the type and severity of the fault. An unbalanced set of HVAC voltages will result in unequal values of V_{dc} for the three phases of the multilevel cascaded quasi-z-source inverter stage, which in turn results in unbalanced high frequency voltages generated by this stage. In the case of this fault type, the generated phase voltages will be unbalanced, i.e. V_a' = 0 p.u, V_b = 3 p.u, and V_c = 3 p.u. This will also result in unbalanced line-to-line voltages of V_{bc}' = 5.1962 p.u and $V_{ab}' = V_{ca}'$ = 3 p.u.

However, the alternative method cannot be implemented to solve this issue in the previous case. The reason for that is the remaining healthy cells in phase "a" (N_{RHC}) are equal to zero. As a result of this, the fault gain (F_{NO} =3/0=???). However, because the alternative method does not have the capability to recover the faulty operation. It is required to resolve this type of fault using the new proposed method. This method will be described further on in this chapter as well.

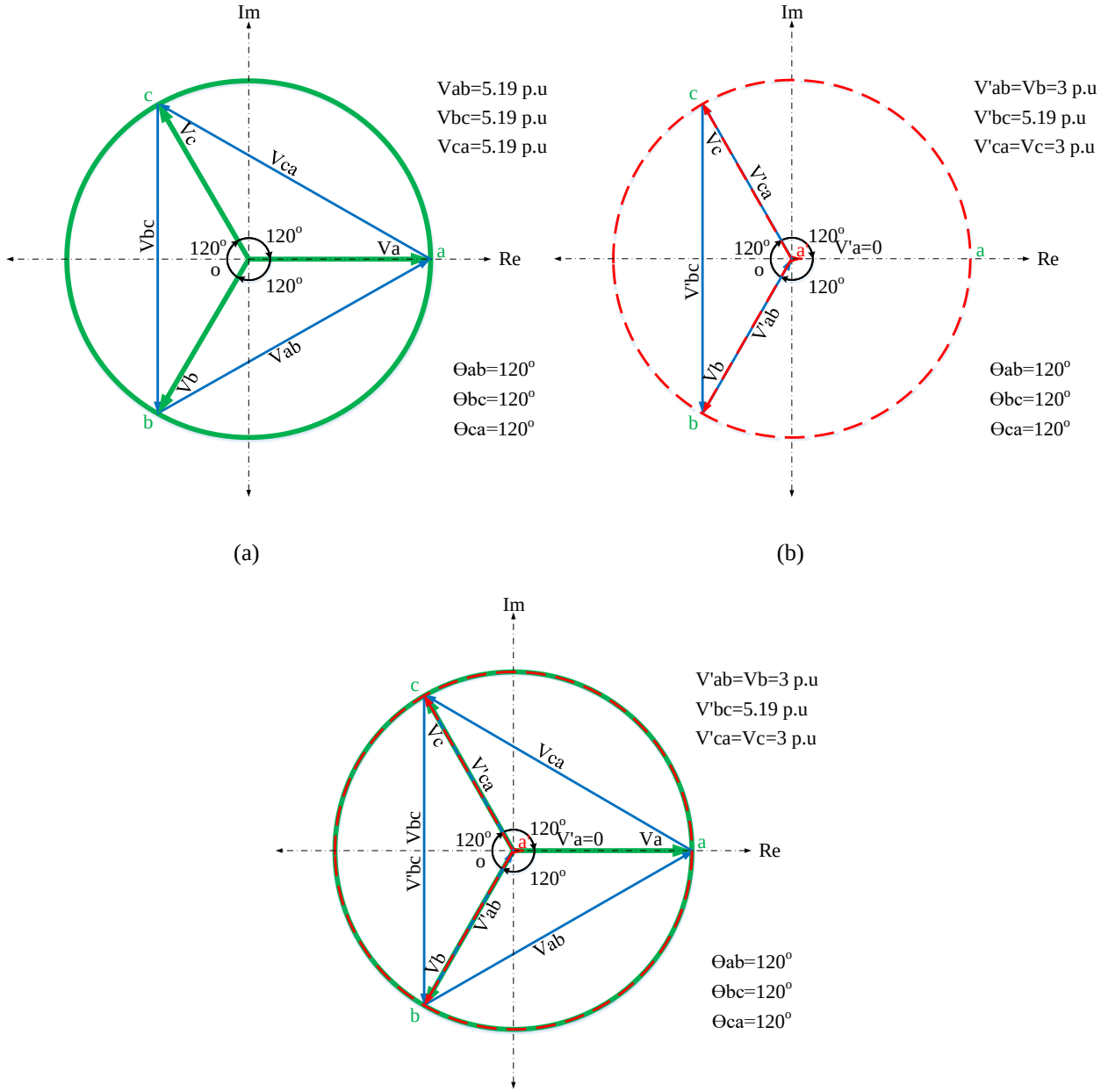


Figure 3.3. Phasor diagrams of the phase and line-to-line voltages for the high voltage side of the isolation stage in the proposed SST: (a) healthy SST operation, (b) a single line-to-ground HVAC grid fault in phase “a”, and (c) the healthy operation vs. the faulty operation.

3.5 The Proposed Fault-Tolerant Strategy

The voltage stress and the current of the inductors on all remaining healthy cells in the multilevel cascaded quasi-z-source inverter stage were increased significantly by using the alternative method to overcome the faulty conditions in the fault switches. Also, the alternative method does not have the ability to recover the faulty operation in the case of HVAC grid faults. Therefore, it is necessary to propose another method to overcome these drawbacks.

In the new proposed method, after bypassing the faulty cells, the phase angles of the multilevel cascaded quasi-z-source inverter stage, phase voltages (θ_{ab}, θ_{bc}, and θ_{ca}), will be modified by solving (3.1)-(3.4) to balance the generated line-to-line voltages. In the two previous fault cases, it is clear that the amplitude of the phase voltages is not equal [47, 48, 79-82]. However, by adjusting the phase angles (θ_{ab}, θ_{bc}, and θ_{ca}) to the calculated values, the amplitude of the line-to-line voltages (V_{ab}, V_{bc}, and V_{ca}) will be the same. Therefore, to balance the line-to-line voltages, the phase shifts between phase voltages should be modified to the obtained values [79-82]. Using phase shifted pulse width modulation will modify the phase angles of the phase voltages of the multilevel cascaded quasi-z-source inverter stage by modifying the phase angles of the sinusoidal reference signals [47, 48].

Nevertheless, the amplitude of the new line-to-line voltages will be lower than the line-to-line voltages during the healthy operation [79-82]. This work proposes the use of the quasi-z-source inverter topology boosting capability to restore the amplitude of the line-to-line voltages to their pre-fault condition, which results in fully restored operation of the proposed SST [47, 48].

The proposed solution is to slightly increase the shoot-through duty ratio for all three phases of the quasi-z-source inverter topology in order to distribute the required extra switching stress over all remaining healthy switches in the three phases of this stage. This will increase all the three

phase voltages of the multilevel cascaded quasi-z-source inverter stage, which in turn increases the rebalanced line-to-line voltages to their pre-fault conditions [47, 48]. Increasing the phase voltages can also be done by increasing the modulation index for each phase as well. Increasing the modulation index increases the voltage stress over the switches considerably less than when increasing the shoot-through duty ratio. Therefore, the proposed method finds the minimum amount of the shoot-through duty cycle required for increasing the line-to-line voltages to their pre-fault conditions, through first maximizing the modulation index. Hence, to minimize the dc link voltage for any multilevel cascaded quasi-z-source inverter stage cell, the amount of shoot-through duty ratio needs to be minimized while the modulation index is maximized [47, 48]. As a result, the voltage gain (G) in (2.9) can be expressed again as,

$$G_{new} = M_{\max} \times B_{\min} = \left(1 - D_{\max}\right) \times \frac{1}{1 - 2D_{\min}} \tag{3.8}$$

The modulation index is always greater than zero and less than (1-D). To maximize the modulation index and to minimize the shoot-through duty ratio, the shoot-through duty ratio must be equaled to 1-M. Therefore, while the maximized modulation index will be equal to,

$$M_{\max} = 1 - D_{\min} \tag{3.9}$$

By careful inspection of (3.8), one can realize the shoot-through duty ratio ($D_{\min}$) is,

$$D_{\min} = \frac{\left(G_{new} - 1\right)}{\left(2G_{new} - 1\right)} \tag{3.10}$$

However, in the proposed method, the fault gain (F_{NO}) is formulated as,

$$F_{NO} = \frac{VLL_{HO}}{VLL_{AFO}} \tag{3.11}$$

where VLL_{HO} is the line-to-line voltages in the healthy operation, and VLL_{AFO} is the rebalanced line-to-line voltages after modifying the angles in the faulty operation.

Finally, the new value of inverter gain (G_{new}) in the faculty condition can be calculated using (3.6). The new inverter gain is then substituted in (3.10) to find the minimum required shoot-through duty ratio. The maximized modulation index ($M_{\max}$) is then calculated from (3.9) using this shoot-through duty ratio ($D_{\min}$). The calculated maximized modulation index ($M_{\max}$) and minimized shoot-through duty ratio ($D_{\min}$) will be realized using the new modulation method was described in chapter 2.

The proposed fault-tolerant operation strategy will be introduced for the proposed solid-state transformer in this research under different fault conditions to revamp the faulty operation to the pre-fault operation.

3.5.1 Rebalancing Quasi-Z-Source Inverter Switch Faults (QZSI Switch Faults) Using the Proposed Method

The proposed strategy modifies the phase angles in (3.1)-(3.4) with the goal of rebalancing the post-fault line-to-line voltages. The values of new phase angles that result in balanced line-to-line voltages can be found by solving (3.1)-(3.4) for $V_{ab}' = V_{bc}' = V_{ca}'$ and using the post-fault values of phase voltages (V_a' = 2 p.u and $V_b = V_c$ = 3 p.u),

$$V_a'^2 + V_b^2 - 2V_aV_b\cos(\theta_{ab}') = V_b^2 + V_c^2 - 2V_bV_c\cos(\theta_{bc}') \tag{3.12}$$

$$V_b^2 + V_c^2 - 2V_bV_c\cos(\theta_{bc}') = V_c^2 + V_a'^2 - 2V_cV_a'\cos(\theta_{ca}') \tag{3.13}$$

$$\theta_{ab} + \theta_{bc} + \theta_{ca} = 360^o \tag{3.14}$$

This will result in modified phase angles of $\theta_{ab}' = \theta_{ca}'$ = 130.5288°, and θ_{bc}' = 98.9424° which in turn will result in balanced line-to-line voltages of $V_{ab}' = V_{bc}' = V_{ca}'$ = 4.5605 p.u. The voltage phasors in this condition are illustrated in Figure 3.4(a) and (b). The balanced line-to-line voltages

are fed to the three-phase transformer and will result in balanced transformer phase voltages and currents; thus, it will resolve the unbalanced operation issue. However, the amplitude of the new balanced line-to-line voltages is lower than the line-to-line voltages during the healthy operation.

For the faulty switch in phase "a" and based on (3.11), the fault gain (F_{NO}) is found as 1.1394 to balance line-to-line voltages with the same pre-fault voltage amplitude of 5.1962 p.u. Therefore, the value of the new inverter gain (G_{new}), the minimized shoot-through duty ratio ($D_{\min}$), and the maximized modulation index ($M_{\max}$) will be set to 1.71, 0.29, and 0.71 respectively. Also, the voltage boosting factor (B_{new}) will be set to 2.38, which means the increased voltage stress will be equal to ($+\Delta$ stress% = +19.00%). Therefore, this solution is recommended and is better than the previous solution (alternative method) because of the low voltage stress. The phasor diagram of the voltages for the healthy operation vs. rebalanced post-fault operation using the proposed method for a single QZSI switch fault in phase "a" is demonstrated in Figure 3.4(c). Also, the results of implementing the alternative method and the proposed method are summarized and compared with the healthy operation in Table 3-1.

Table 3-1: Comparison between the healthy operation, the alternative method and the proposed method

Operation / Parameters	The Healthy Operation	The Alternative Method	The Proposed Method
Fault gain (F_{NO})	1.00	1.50	1.1394
New inverter gain (G_{new})	1.50	2.25	1.71
Shoot-through duty ratio (D)	0.25	0.36	0.29
Modulation index (M)	0.75	0.64	0.71
Voltage boosting factor (B_{new})	2.00	3.57	2.38
$+\Delta$ stress%	0.00%	+78.50%	+19.00%

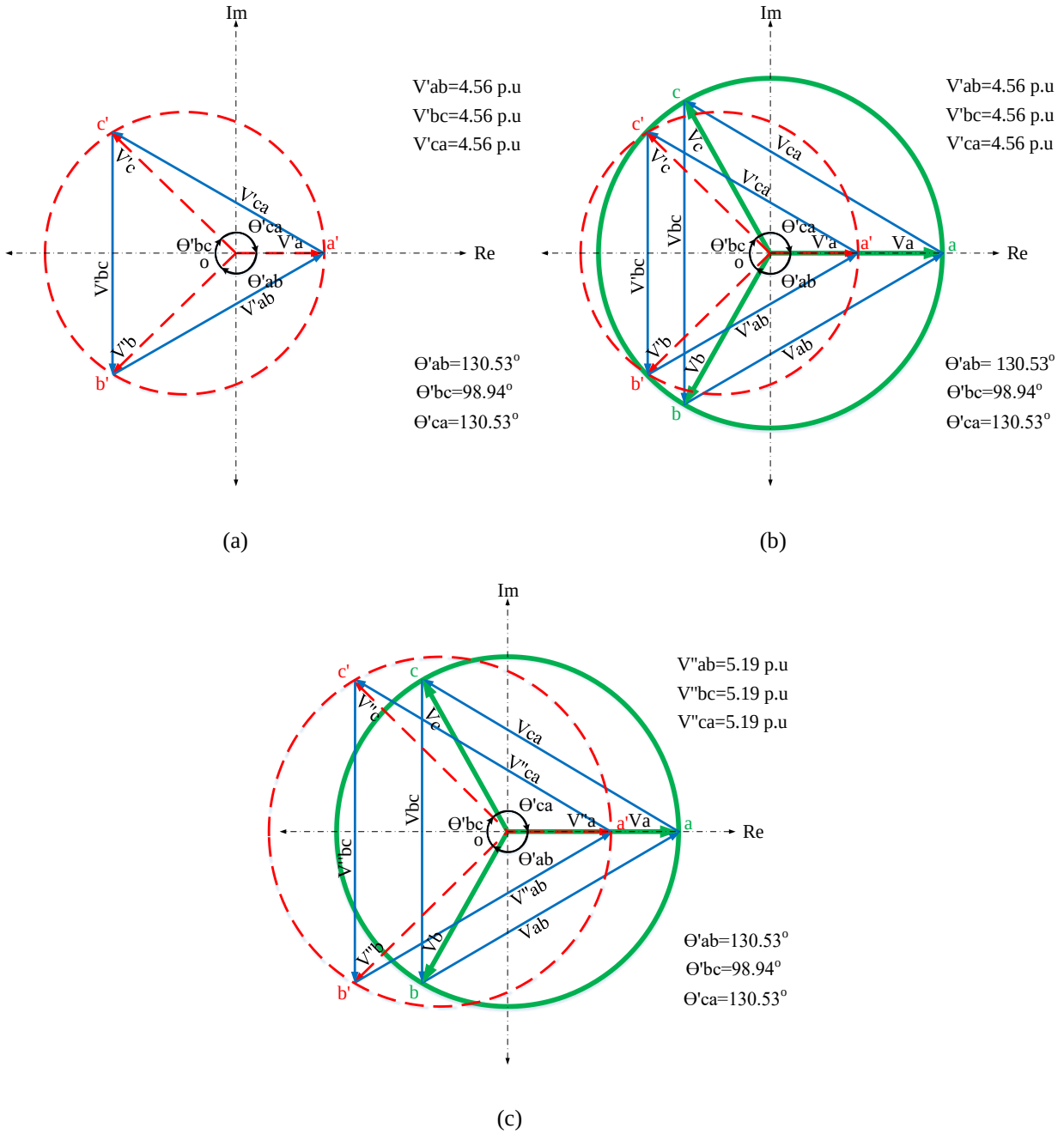


Figure 3.4. Phasor diagrams of the phase and line-to-line voltages for the high voltage side of the isolation stage in the proposed SST in the case of a single QZSI switch fault in phase "a" when using the proposed fault-tolerant strategy: (a) modifying the phase angles to rebalance line-to-line voltages, (b) the healthy operation vs. the modifying the phase angles operation, and (c) the healthy operation vs. the modifying the phase angles and increasing the line-to-line voltages to their pre-fault values using boosting property of QZSI circuits operation.

3.5.2 Rebalancing High Voltage AC Grid Faults (HVAC Grid Faults) Using the Proposed Method

The proposed fault-tolerant method can resolve this issue similarly to the previous fault case by modifying the phase angles of the multilevel cascaded quasi-z-source inverter stage phase voltages. Subsequently, in the case of a single line-to-ground fault on phase "a" of the HVAC grid, after modifying the angles to $\theta_{ab}' = \theta_{ca}' = 150^{o}$, and $\theta_{bc}' = 60^{o}$ which in turn will result in balanced line-to-line voltages of $V_{ab}' = V_{bc}' = V_{ca}' =$ 3.00 p.u. The voltage phasors in this condition are illustrated in Figure 3.5(a) and (b). However, the amplitude of the new line-to-line voltages will be lower than the line-to-line voltages during the healthy operation. Therefore, to generate balanced line-to-line voltages with the same pre-fault voltage amplitude of 5.1962 p.u the fault gain (F_{NO}) was recalculated in this case study based on (3.11), and it was found as $\sqrt{3}$ = 1.7321. Therefore, the value of the new inverter gain (G_{new}), the minimized shoot-through duty ratio ($D_{\min}$), and the maximized modulation index ($M_{\max}$) will be set to 2.60, 0.38, and 0.62 respectively. As a result of this, the amplitude phase voltages of the multilevel cascaded quasi-z-source inverter stage will be increased to $V_b' = \sqrt{3}V_{ab} =$ 5.1962 p.u and $V_c' = \sqrt{3}V_{ca} =$ 5.1962 p.u. The phasor diagram of the voltages for the healthy operation vs. rebalanced post-fault operation using the proposed method for a single line-to-ground HVAC grid fault in phase "a" is demonstrated in Figure 3.5(c). Finally, using the proposed method for rebalancing QZSI switch faults in the case of a single QZSI switch fault in phase "a" and for rebalancing HVAC grid faults in the case of a single line-to-ground HVAC grid fault in phase "a" are summarized and compared with the healthy operation for each case as illustrated in Figure 3.6.

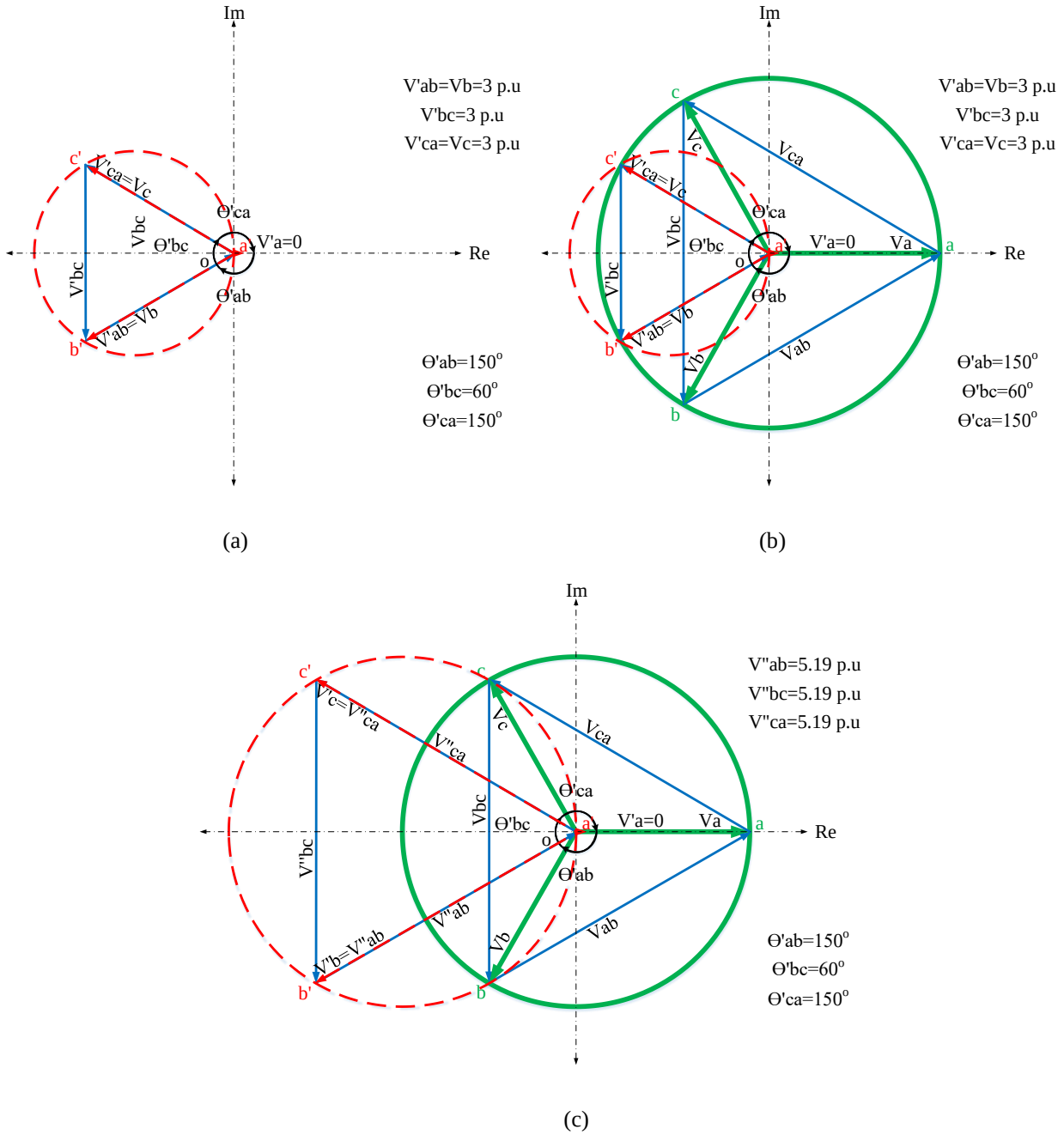


Figure 3.5. Phasor diagrams of the phase and line-to-line voltages for the high voltage side of the isolation stage in the proposed SST in the case of a single line-to-ground HVAC grid fault in phase "a" when using the proposed fault-tolerant strategy: (a) modifying the phase angles to rebalance line-to-line voltages, (b) the healthy operation vs. the modifying the phase angles operation, and (c) the healthy operation vs. the modifying the phase angles and increasing the line-to-line voltages to their pre-fault values using boosting property of QZSI circuits operation.

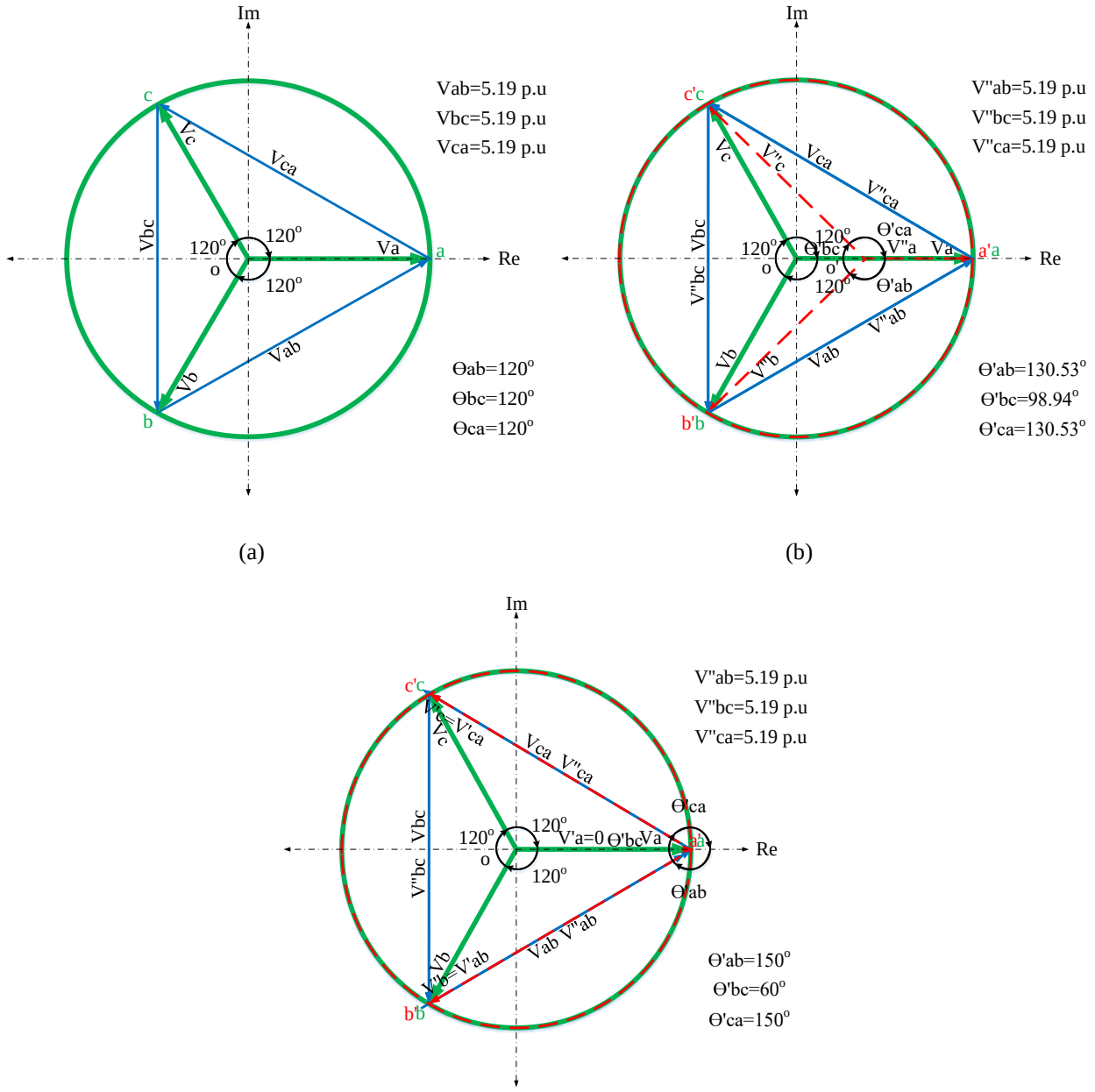


Figure 3.6. Phasor diagrams of the phase and line-to-line voltages for the high voltage side of the isolation stage in the proposed SST when using the proposed fault-tolerant strategy: (a) the healthy operation, (b) the healthy operation vs. the modifying the phase angles and increasing the line-to-line voltages to their pre-fault values in the case of a single QZSI switch fault in phase “a”, and (c) the healthy operation vs. the modifying the phase angles and increasing the line-to-line voltages to their pre-fault values in the case of a single line-to-ground HVAC grid fault in phase “a”.

3.6 Comparison between the Conventional Method and the Proposed Method

The function of the conventional solutions is completely to bypass cells in the healthy phases to equalize the total number of the remaining healthy cells in the faulty phase to balance out the voltages. As result, the output voltages will be balanced with a reduced amplitude.

However, in the proposed method, the function of faulty cells is compensated by using all the remaining healthy cells in all three phases and using the boosting factor of the quasi-z-source inverter topology to completely restore the pre-fault operation. The results in Table 3-2 are calculated for only one faulty switch in phase "a" using the healthy operation as a reference with the phase voltages amplitude of 3 p.u and the line-to-line voltages amplitude of 5.1962 p.u.

Table 3-2: Comparison between the conventional method and the proposed method

	The Conventional Method	The Proposed Method
Amplitude	V_p (p.u)	V_p (p.u)
V_a	2	2.2788
V_b	2	3.4182
V_c	2	3.4182
V_{ab}	3.4641	5.1962
V_{bc}	3.4641	5.1962
V_{ca}	3.4641	5.1962
$+\Delta stress\%$	50%	19%

The results in Table 3-2 are calculated for the minimum number of cells, which is three, to show the ability of the proposed SST to overcome the faulty operation. The voltage stress will be decreased if the number of cells is increased for both of the conventional and proposed method. However, the performance of the proposed method is better than the performance conventional method because the total of bypassed cells in the conventional method is equal to three times the

number of the faulty cells of the proposed three-phase SST. Therefore, to minimize the voltage stress in the conventional method, it is required to increase the number of cells. However, increasing the number of cells for the proposed method, which is not required, will give more flexibly to distribute the voltage stress over more cells. As result, using the proposed method will always increase the voltage stress lower than using the conventional method.

3.7 Comparison between the Alternative Method and the Proposed Method

The function of the alternative solutions is only to increase the voltage amplitude of the remaining healthy cells of the faulty phase. Therefore, the proposed SST can overcome the faulty operation to restore the pre-fault operation. As result, the proposed SST can fully rebalance the faulty operation, but the voltage stress is only increased in the faulty phase. However, the voltage stress over the healthy cells in the faulty phase will be increased a lot and can lead to more switch failures. The results in Table 3-3 are calculated for only one faulty switch in phase "a" using the healthy operation as a reference with the same values in Table 3-2.

Table 3-3: Comparison between the alternative method and the proposed method

	The Alternative Method	The Proposed Method
Amplitude	V_p (p.u)	V_p (p.u)
V_a	3	2.2788
V_b	3	3.4182
V_c	3	3.4182
V_{ab}	5.1962	5.1962
V_{bc}	5.1962	5.1962
V_{ca}	5.1962	5.1962
$+\Delta stress\%$ for only phase "a"	78.5%	19%

According to Table 3-3 the performance of the proposed method is better than the performance of the alternative method because of the voltage stress. Both of the proposed and alternative method can be improved by increasing the number of cells in the proposed SST. However, increasing the number of the cells in the proposed method, which is not required, will improve the proposed method more than alternative method.

Finally, the conventional method cannot restore the pre-fault operation, but the proposed method can completely restore the pre-fault operation. Also, in the conventional and alternative method, it is required to increase the number of cells to improve the performance of the proposed SST, but in the proposed method it is not required. In the conventional and alternative method, the number of cells cannot be increased a lot to improve the performance of the proposed SST because they will increase the size. Hence, the proposed method is succeeded to fully restore the pre-fault operation with better performance than the conventional and alternative method.

3.8 The Output Stage of the Proposed Solid-State Transformer

As explained in the beginning of this chapter, the output stage essentially consists of a conventional three-phase inverter. The inverter filters and synchronizes the output of the proposed three phase solid-state transformer to the grid. Also, the generated DC power from the isolation stage can be controlled and converted into AC power to be easily connected to the grid because most applications and devices need AC electricity. Therefore, it is required to design an accurate control method for the inverter to guarantee and increase the reliability of the proposed three phase solid-state transformer. The control methods are designed in different ways, but they are mainly classified based on controlling the voltage or controlling the current [86].

In this chapter, the three-phase inverter connected to the grid is studied by presenting the mathematical model for the inverter. Thus, the control method can be introduced and applied in the studied faults to confirm the output results of the proposed three phase solid-state transformer.

The three-phase inverter is a device that converts a DC source into an AC source with desired magnitude and frequency [66, 73, 87, 88]. Also, in the proposed three phase solid-state transformer, the output voltage is desired to be the grid with (120V with 60 Hz). Therefore, to provide a three-phase balanced (fundamental) voltage source [89, 90], the output stage is designed as a three-phase inverter. The output stage of the proposed phase solid-state transformer (the three-phase inverter (VSI)) is shown in Figure 3.7.

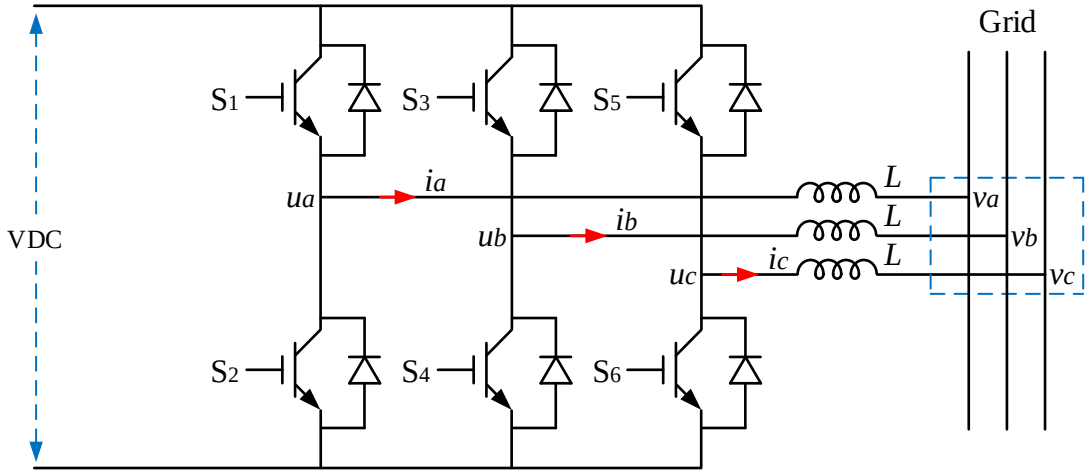


Figure 3.7. The output stage of the proposed solid-state transformer (The three-phase inverter).

3.9 Control Strategy for the Output Stage of the Proposed Solid-State Transformer (The Three-Phase Inverter)

Controlling the active and reactive power of the three-phase inverter can be achieved by implementing current a control method or a voltage control method [91]. In the voltage control method, the phase angle between output voltage of the three-phase inverter and the grid is used to control the active and reactive power of the three-phase inverter [92]. However, in the current

control method, the injected current into the grid, with the both active and reactive components, is controlled to control the active and reactive power [91]. The current control method is widely used if it is compared to the voltage control method because of its features such as [93]:

- It has fast response.
- It is less sensitive to small phase errors.
- It is less sensitive to small harmonic currents.
- It is less sensitive to distortion in the grid voltage.
- Therefore, it is considered as a main part in controlling the inverters.

The current control method can be implemented by different ways such as hysteresis current control, predictive current control, and proportional integral current control (PI) [94].

3.9.1 Hysteresis Current Control (HCC)

The output currents of the inverter are compared with the commanded currents for each phase individually. The current errors of the comparison are used to generate and determine the pulse width modulation states for the power switches of the inverter [95-99]. However, since the states of the inverter are determined directly, the hysteresis current control does not require a modulator. Therefore, it is insensitive to system parameters and has simplicity of the design. Also, the dynamic response is fast, but it has some disadvantages such as high ripples of the output currents with variable switching frequency [94, 97, 99].

This type of control has an error band within a fixed range. Then in the case of the output currents are lower than the lower limit of the hysteresis band of the commanded currents, the output voltages and output currents will be increased. However, when the output currents are higher than the upper limit of the hysteresis band of the commanded currents, the output voltages and output currents will be decreased [94-99].

3.9.2 Predictive Current Control

In predictive control method, the system is modeled to predict the future behavior of the controlled variables and to follow the reference values. This type of control is complicated control method, and it requires the system parameters to be known accurately [94, 100, 101]. The stability of the predictive current control is affected by the parameters since, the parameters may vary with environmental conditions such as: temperature and core saturation. Although it may lead to parameter sensitivity problems, its dynamic response is fast. Also, the steady-state performance is perfect. It is considered as one of the best current control methods with minimum distortion [94, 100-102].

3.9.3 Proportional Integral Current Control (PI)

One of the most known current control methods is the proportional integral (PI) compensator. In this type of control method, the error values are calculated as the difference between the commanded currents of the inverter and the injected currents into the grid. Hence, the error between them is minimized by the controller [97, 99]. A PI controller has two separate constant parameters, which are the proportional parameter (k_p) and the integral parameter (k_i).

The proportional parameter (k_p) is usually called the gain of the controller, and it reduces the overall error with time. However, as the error is minimized to zero, but it cannot converge, the effect of the k_p will be reduced. Therefore, there will be a small steady-state error. The small steady-state error can be fixed through the integral parameter (k_i) by integrating this error. However, over time, the error will be accumulated into a large error value. Then by multiplying the accumulated error by the k_i, it will become the integral output of the PI controller. Therefore, by adding both outputs of proportional and integral signals, the movement of the process will be

accelerated, and the small steady-state error will be eliminated. The PI current controller does not need system models. Therefore, it is insensitive to system parameters. Also, performance of the steady-state response is perfect with low current ripples [99].

Comparison between the three current control methods are summarized in Table 3-4 to explain the advantages and disadvantages between them.

Table 3-4: The comparison between the three current control methods

Control Method / Performance	Hysteresis Current Control	Predictive Current Control	Proportional Integral Current Control (PI)
Dynamic response	Very fast	Fast	Fast response, but it is slower than the other methods
Steady-state response	High THD	Low THD	Very low THD
Sensitivity to system parameters	No	Yes	No

Therefore, it can be concluded that the proportional integral current control (PI) is the best choice to be implemented for the output stage of the proposed three phase solid-state transformer.

3.10 Mathematical Model for the Output Stage of the Proposed Solid-State Transformer (The Three-Phase Inverter)

The mathematical model for the three-phase inverter shown in Figure 3.7 is presented in [103-105] as follows:

The three-phase grid voltages are represented as,

$$v_b = V_a \cos(\omega t) \tag{3.15}$$

$$v_b = V_b \cos(\omega t - 120^o) \tag{3.16}$$

$$v_c = V_c \cos(\omega t + 120^o) \tag{3.17}$$

where $V_a = V_b = V_c = V_s = 120\sqrt{2}$ V and ($\omega = 2\pi * f$) are the maximum phase voltage and angular frequency of the grid respectively. Hence, the system equations can be presented as,

$$u_a = L\frac{d}{dt}i_a + v_a \tag{3.18}$$

$$u_b = L\frac{d}{dt}i_b + v_b \tag{3.19}$$

$$u_c = L\frac{d}{dt}i_c + v_c \tag{3.20}$$

where L is the inductance between the inverter and the grid, u_a, u_b, and u_c are the output voltages of the inverter, and i_a, i_b, and i_c are the injected currents into the grid. Therefore, the voltage at the inverter AC terminals can be given by (3.21), and the n equivalent circuit is shown in Figure 3.8(a).

$$u_n = L\frac{d}{dt}i_n + v_n \tag{3.21}$$

where the subscript n denotes phase “a”, phase “b”, and phase “c”.

Then this equation can be transformed by using q-d transformation to be rewritten into two-phase stationary q-d reference frame [105, 106] as given in (3.22) and (3.23), and the circuits are shown in Figure 3.8(b) and (c) respectively.

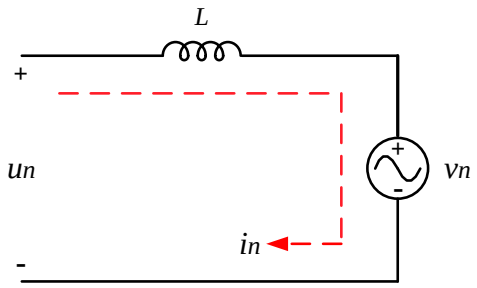
$$u_q = L\frac{d}{dt}i_q + \omega L i_d + v_q \tag{3.22}$$

$$u_d = L\frac{d}{dt}i_d - \omega L i_q + v_d \tag{3.23}$$

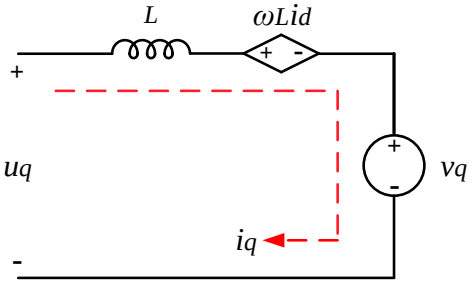
where u_q and u_d are q-d transformation of the output voltages of the inverter, i_q and i_d are q-d transformation of the injected currents into the grid, and v_q and v_d are q-d transformation of the three-phase grid voltages, which are presented as [105, 107-110],

$$\begin{bmatrix} v_q \\ v_d \end{bmatrix} = (2/3)\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & -\sqrt{3}/2 & \sqrt{3}/2 \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{3.24}$$

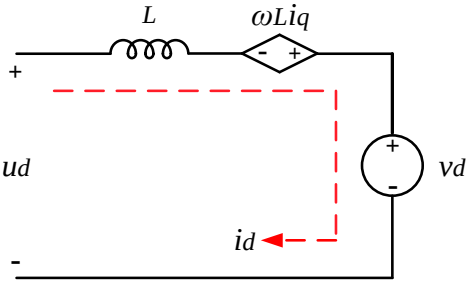
However, it should be noted that the transformation matrix in (3.24) is calculated based on q-axis of the q-d axis is aligned with a-axis of the a-b-c axis, and the zero sequence component is ignored.



(a). The n equivalent circuit.



(b). The q equivalent circuit.



(c). The d equivalent circuit.

Figure 3.8. The equivalent circuits for the output stage of the proposed solid-state transformer (The three-phase inverter).

The voltage across the inductor is proportional to the change of current through the inductor; thus, the voltages in stationary q-d reference frame can be given as,

$$v_{Lq} = L\frac{d}{dt}i_q \tag{3.25}$$

$$v_{Ld} = L\frac{d}{dt}i_d \tag{3.26}$$

Also, the PI current controllers are implemented to force the output currents to track their reference values as described in (3.27) and (3.28),

$$v_{Lq}^{*} = k_p \left(i_q^{*} - i_q \right) + k_i \int \left(i_q^{*} - i_q \right) dt \tag{3.27}$$

$$v_{Ld}^{*} = k_p \left(i_d^{*} - i_d \right) + k_i \int \left(i_d^{*} - i_d \right) dt \tag{3.28}$$

where v_{Lq}^{*} and v_{Ld}^{*} are the output voltages of the current controllers.

Since v_q in (3.22) and v_d in (3.23) are constant values, both of them can be neglected when rewriting these equations in reference values of the inverter AC-side voltages as,

$$u_q^{*} = v_{Lq}^{*} + \omega L i_d \tag{3.29}$$

$$u_d^{*} = v_{Ld}^{*} - \omega L i_q \tag{3.30}$$

Then the active and reactive power in the stationary q-d reference frame are expressed in [107-109] as,

$$P = \frac{3}{2} \left(v_q i_q + v_d i_d \right) \tag{3.31}$$

$$Q = \frac{3}{2} \left(v_q i_d - v_d i_q \right) \tag{3.32}$$

Also, v_q and v_d are presenting the q-d transformation of the three-phase grid voltages. Hence, the function of the active and reactive power can be presented as,

$$P = f \left(i_q \right) \tag{3.33}$$

$$Q = f \left(i_d \right) \tag{3.34}$$

Then the active power can be controlled only by controlling i_q, and the reactive power can be controlled only by controlling i_d. The controlling method can be implemented by:

PI controller as described in (3.35) and (3.36).

$$i_q^* = k_p\left(P^* - P\right) + k_i\int\left(P^* - P\right)dt \tag{3.35}$$

$$i_d^* = k_p\left(Q^* - Q\right) + k_i\int\left(Q^* - Q\right)dt \tag{3.36}$$

Proposed control method: solving the active and reactive power equations for unknown currents by using the reference values, where $v_q^* = v_q$ and $v_d^* = v_d$ are for the grid. Therefore, (3.31) can be solved for i_q^* and (3.32) for i_d^* using the reference values as,

$$i_q^* = \frac{\left(\frac{2}{3}P^* - v_d i_d^*\right)}{v_q} \tag{3.37}$$

$$i_d^* = \frac{\left(\frac{2}{3}Q^* + v_d i_q^*\right)}{v_q} \tag{3.38}$$

However, the performance of the inverter by using the proposed control method is better than using the PI controller. The comparison between the two different methods are summarized in Table 3-3.

Table 3-5: The comparison between 4-PI controller and proposed control method

Performance	4-PI Controller	Proposed Control Method
Response	Slow response	Fast response
Reliability	Good reliability	Excellent reliability
Stability	Limited stability range	Extended stability range

By using all described equations above, the block diagram of three-phase inverter control system can be illustrated in Figure 3.9.

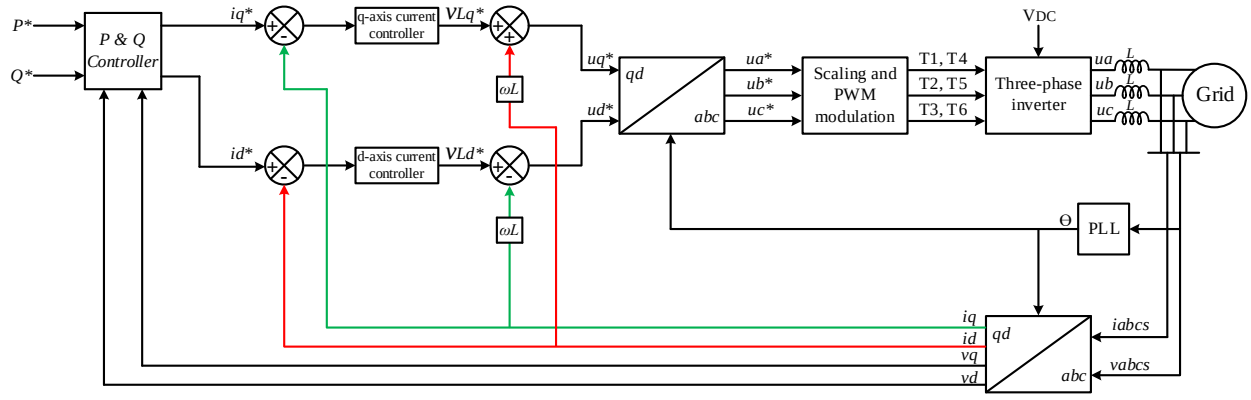


Figure 3.9. The block diagram for the output stage of the proposed solid-state transformer (The three-phase inverter) control system.

As shown in the figure, the block diagram comprises two inner control loops and two outer control loops.

The two outer control loops can be implemented by two PI controllers or using the proposed method control. Therefore, the measured active and reactive power (P and Q) are forced to track their reference values (P^* and Q^*). Then the reference values of the output currents of the inverter in the stationary q-d reference frame (i_q^* and i_d^*) can be obtained from the output of the two outer control loops. These currents are needed to be the input of the two inner control loops.

The two inner control loops are implemented by two PI controllers. Hence, the measured currents (i_q and i_d) are forced to track their reference values (i_q^* and i_d^*), which are provided by outer control loops. Thus, the reference values of the output voltages of the inverter in the stationary q-d reference frame (u_q^* and u_d^*) can be obtained from the output of the two inner control loops.

As a result, the reference output voltages of the inverter (u_a^*, u_b^*, and u_c^*) are calculated from (u_q^* and u_d^*) by using inverse q-d transformation. Then they are scaled to generate pulses for the inverter switches individually by using the pulse width modulation algorithm [97]. Thus, the

desired inverter voltages can be generated. These voltages are needed to generate the currents that are required to be injected into the grid. Therefore, the power factor can be set to unity by setting the reactive power to be zero ($Q^* = 0$). Therefore, $i_d^* = 0$ and the active power can be increased to reach its maximum value by controlling i_q.

Chapter 4

4.1 Simulation Results

This chapter presents the simulation results and the analyses of testing the proposed three-phase the solid-state transformer under the two type of faults, which are demonstrated in the previous chapter. The setup of the proposed three-phase solid-state transformer shown in Figure 3.1 was implemented using PLECS. In this setup, the high voltage AC side of the isolation stage is set to 6.6 kV for each phase. The generated high frequency AC voltages have a frequency of 10 kHz, and the voltage at the low voltage DC bus is regulated to 400 V, which will be the input of the output stage. The components of the isolation stage for each phase are L_1=L_2= 0.30 mH, C_1=C_2 = 300 uF, Cl_{ink1}=Cl_{ink2}= 150 uF, and the high frequency transformer is connected in Y-Y configuration. The output stage with low voltage AC grid has a voltage of 120 V with 60 Hz to be synchronized with the grid, the active power is equal to 8 kW, and the reactive power is controlled to be zero Var. The components of the output stage for each phase are L_{out}= 2 mH. The PLECS simulation details of the isolation stage, the output stage, and the active and reactive power controller for the proposed three-phase solid-state transformer are shown in Figure 4.1, Figure 4.2, and Figure 4.3 respectively.

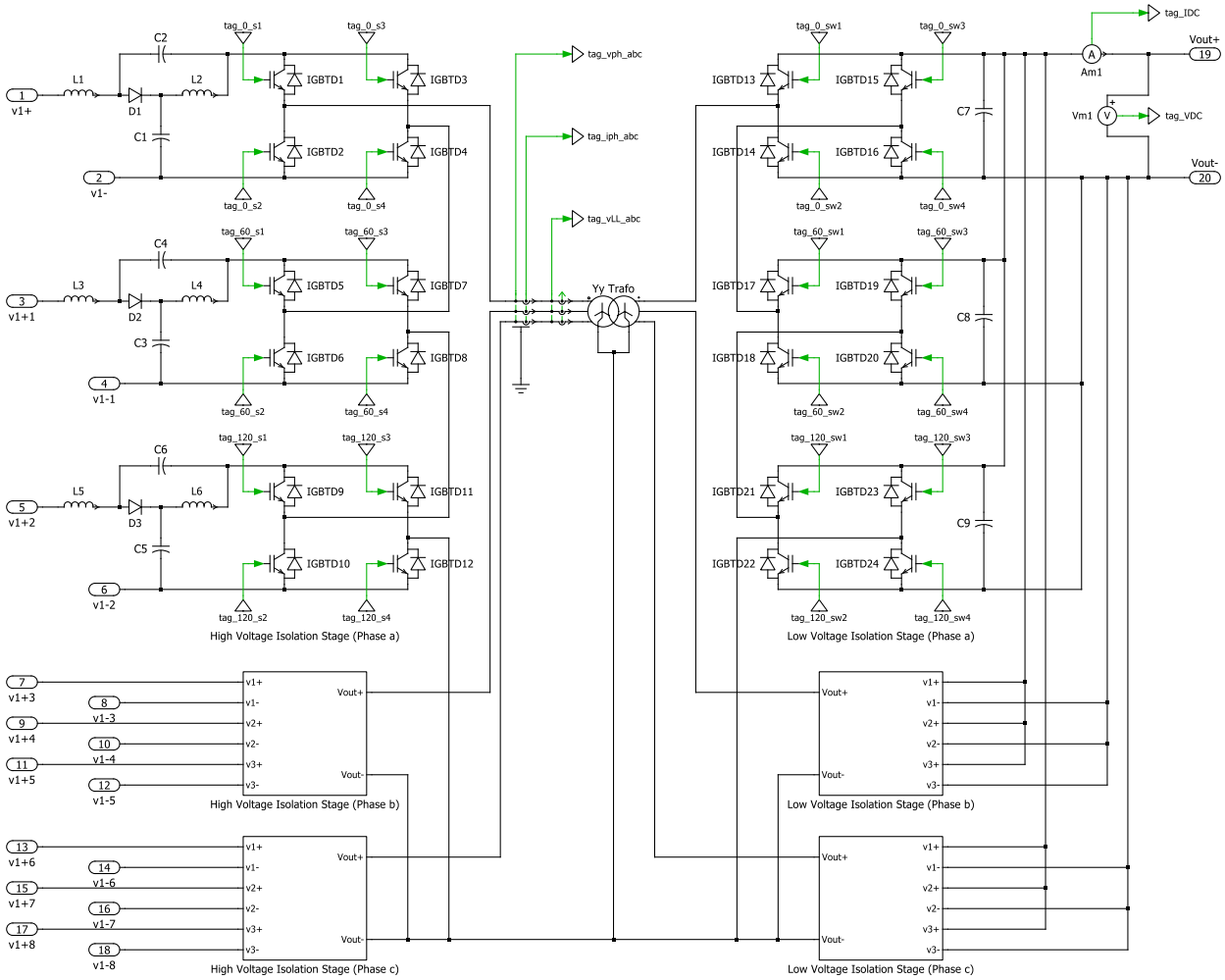


Figure 4.1. The isolation stage of the proposed three-phase solid-state transformer in PLECS.

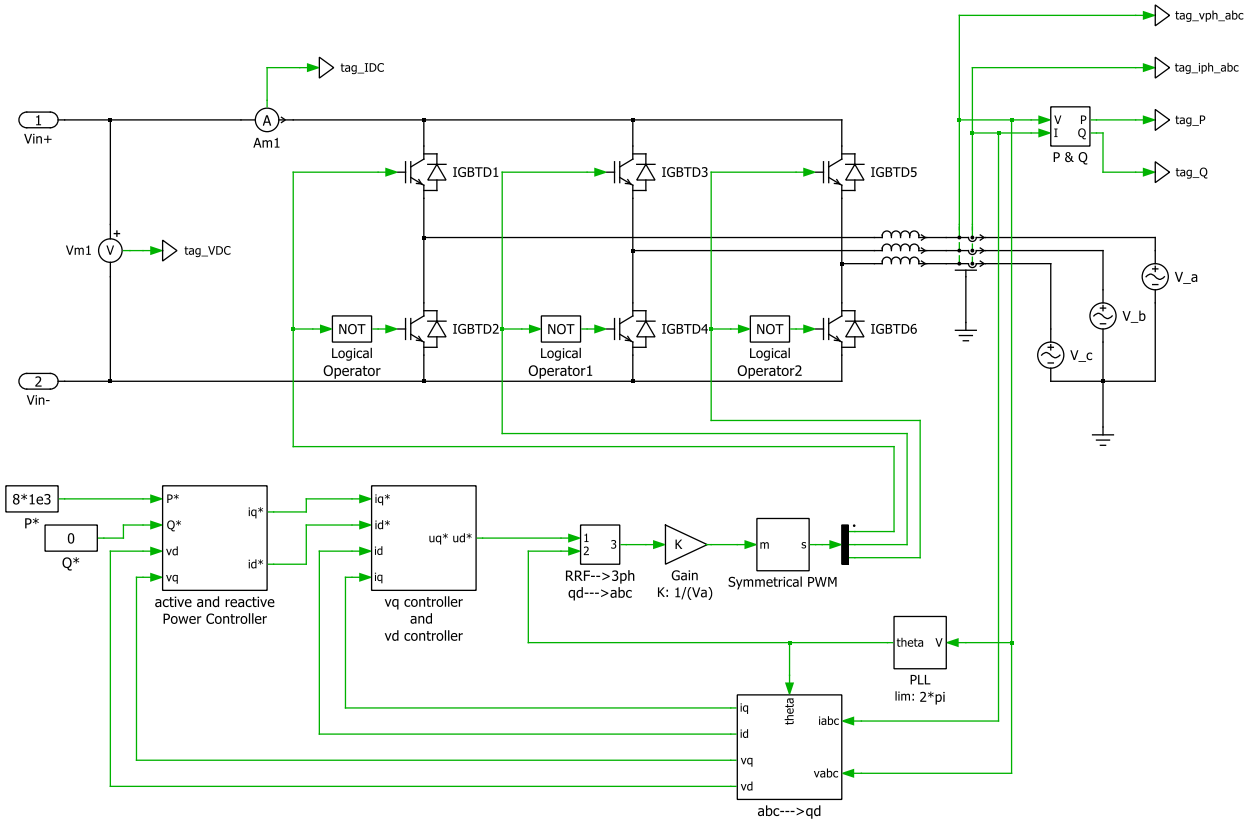


Figure 4.2. The output stage of the proposed three-phase solid-state transformer in PLECS.

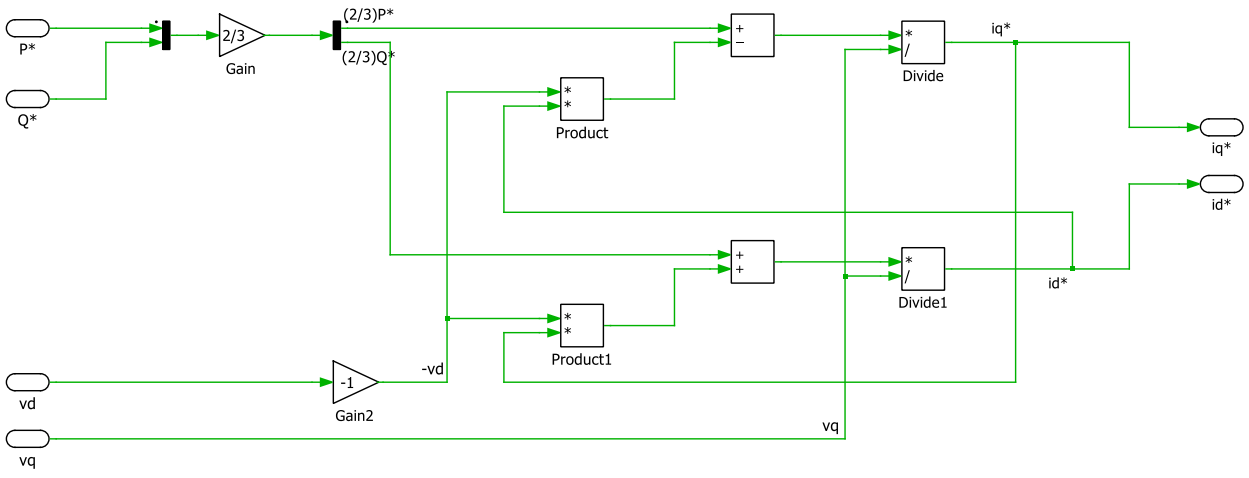


Figure 4.3. The active and reactive power controller for the output stage of the proposed three-phase solid-state transformer in PLECS.

As mentioned in chapter 3, in the healthy operation, the system was balanced. Therefore, the healthy operation will be used as a reference for other operations. The generated phase voltages and the generated line-to-line voltages are summarized in Table 4-1 based on the per unit values and actual values, where the base value is (2.2 kV).

Table 4-1: Calculated phase voltages and line-to-line voltages during the healthy operation

	Phase Voltages			Line-to-Line Voltages		
Amplitude	V_a	V_b	V_c	V_{ab}	V_{bc}	V_{ca}
V_p (p.u)	3	3	3	5.1962	5.1962	5.1962
V_p (kV)	6.6	6.6	6.6	11.4315	11.4315	11.4315

4.2 The Analysis of the Faults

4.2.1 The Analysis of Quasi-Z-Source Inverter Switch Faults (QZSI Switch Faults)

The first analysis is the fault occurrence in one of the switches of the multilevel cascaded quasi-z-source inverter stage in phase “a”. The first step is to bypass the faulty cell in phase “a”. As a result, the remaining healthy cells will be two cells, whereas the total number of the cells in the healthy operation for each phase is three cells. Therefore, the generated line-to-line voltages will be unbalanced. In this condition, to balance the generated line-to-line voltages, the phase shifts between the generated phase voltages of the multilevel cascaded quasi-z-source inverter stage have to be modified to their obtained values in chapter 3. In this case study, the modified phase angles are $\theta_{ab}' = \theta_{ca}' =$ 130.5288^o, and $\theta_{bc}' =$ 98.9424^o which will balance the generated line-to-line voltages. However, the amplitude of the new balanced generated line-to-line voltages is lower than the amplitude of the generated line-to-line voltages during the healthy operation. Subsequently, to balance the generated line-to-line voltages with the same pre-fault voltage amplitude of 5.1962

p.u, the fault gain (F_{ON}) is calculated based on (3.11) and is found as 1.1394. Finally, using the new fault gain with the modified phase shifts (using the phase shifted pulse width modulation) to fully restore the healthy operation of the multilevel cascaded quasi-z-source inverter stage in phase "a" to the pre-fault conditions. The generated phase voltages and the generated line-to-line voltages are summarized in Table 4-2 in the per unit values and actual values, where the base value is (2.2 kV).

Table 4-2: Calculated phase voltages and line-to-line voltages using the proposed method

	Phase Voltages			Line-to-Line Voltages		
Amplitude	V_a "	V_b '	V_c '	V_{ab} "	V_{bc} "	V_{ca} "
V_p (p.u)	2.2788	3.4182	3.4182	5.1962	5.1962	5.1962
V_p (kV)	5.0134	7.5200	7.5200	11.4315	11.4315	11.4315

The proposed three-phase solid-state transformer was tested under the fault switch in phase "a" to confirm the validity of the work for the proposed method by comparing the calculated values with the measured values. The analysis was divided as,

- The first time period at ($0 \le t < t_1$) is healthy operation.
- The second time period at ($t_1 \le t < t_2$) is faulty operation.
- The third time period at ($t_2 \le t < t_3$) is faulty operation with the modified phase angles.
- The fourth time period at ($t \ge t_3$) is faulty operation with the modified phase angles and increased boosting factor (*B*).

Healthy operation at ($0 \le t < t_1$): The system is working normally till ($t < t_1$). The generated phase voltages and the generated line-to-line voltages are balanced, and they have all seven voltage levels with the equal phase angles. As pictured in Figure 4.4 and Figure 4.5, the amplitude of the generated phase voltages is equal, and the amplitude of generated line-to-line voltages is equal too.

Therefore, the operation of the multilevel cascaded quasi-z-source inverter stage is balanced. The measured voltages during this operation are compared to the calculated voltages and summarized in Table 4-3. Also, they will be compared with the rebalanced calculated and measured voltages after implementing the proposed method in the same table. The line currents of this stage during this operation are shown in Figure 4.6.

Faulty operation at ($t_1 \le t < t_2$): During this period of the operation, there is a fault in one cell of phase "a". The faulty cell was bypassed, therefore, the generated voltage of phase "a" has only five voltage levels while the other two phase voltages have all seven voltage levels. As pictured in Figure 4.4 and Figure 4.5, the amplitude of the generated phase voltages is unequal, and the amplitude of generated line-to-line voltages is unequal too. Therefore, the operation of the multilevel cascaded quasi-z-source inverter stage is unbalanced. The line currents of this stage during this operation are shown in Figure 4.6.

Faulty operation with modified phase angles at ($t_2 \le t < t_3$): To balance the generated line-to-line voltages, the first step of the proposed fault tolerant method is applied in this period of the operation. The phase shift angles between the waves of the generated phase voltages are adjusted to be $\theta_{ab}' = \theta_{ca}' = 130.5288^{o}$ and $\theta_{bc}' = 98.9424^{o}$ using the proposed method. As pictured in Figure 4.4 and Figure 4.5, the amplitude of the generated phase voltages is not equal, but the amplitude of the generated line-to-line voltages is equal. However, it is lower than the amplitude of the generated line-to-line voltages in the healthy operation, but the operation of the multilevel cascaded quasi-z-source inverter stage is balanced. Although the operation is balanced, it needs to fully restore the healthy operation by boosting the generated line-to-line voltages to be the same values as the generated line-to-line voltages in the healthy operation. The line currents of this stage during this operation are shown in Figure 4.6.

Faulty operation with the modified phase angles and increased boosting factor (B) at ($t \geq t_3$): To fully restore the healthy operation, the boosting factor was increased as a second step of the proposed method by increasing the shoot-through duty ratio to the new minimized value was calculated in chapter 3. As pictured in Figure 4.4 and Figure 4.5, even though the amplitude of the generated phase voltages is unequal, the amplitude of generated line-to-line voltages is equal to the same amplitude of the generated line-to-line voltages in the healthy operation. Therefore, the operation of the multilevel cascaded quasi-z-source inverter stage is balanced. The measured voltages during this operation are compared to the calculated voltages and summarized in Table 4-3. Also, they are compared with the calculated and measured voltages in the healthy operation in the same table. The line currents of this stage during this operation are shown in Figure 4.6.

Table 4-3: Validity of the proposed method to fully restore the healthy operation

	Healthy operation ($0 \leq t < t_1$)			Faulty operation with modified phase angles and increased boosting factor (B) ($t \geq t_3$)		
	Calculated Amplitude		Measured Amplitude	Calculated Amplitude		Measured Amplitude
	V_p (p.u)	V_p (kV)	V_p (kV)	V_p (p.u)	V_p (kV)	V_p (kV)
V_a	3	6.6	6.58	2.2788	5.0134	5.00
V_b	3	6.6	6.58	3.4182	7.5200	7.49
V_c	3	6.6	6.58	3.4182	7.5200	7.49
V_{ab}	5.1962	11.4315	11.4	5.1962	11.4315	11.4
V_{bc}	5.1962	11.4315	11.4	5.1962	11.4315	11.4
V_{ca}	5.1962	11.4315	11.4	5.1962	11.4315	11.4

According to Table 4-3, it is clear that all measured voltages are very close to their calculated values. Additionally, the measured generated line-to-line voltages are rebalanced again with the same pre-fault values, which confirms the validity of the proposed method. As a result, the

capability of the controller in the output stage is achieved to control the input voltage, the input current, the output active power, which are shown in Figure 4.7, Figure 4.8, and Figure 4.9 respectively. Also, the capability of the controller to synchronize the output voltage of the output stage with the grid is achieved as shown in Figure 4.10. The injected currents to the grid are shown in Figure 4.11. Figure 4.7, Figure 4.8, and Figure 4.9 display the waveforms for the output stage input voltage, input current, and output active power vs. time. According to these figures, during the switch fault, the lost power is one third of delivered power by phase “a”, which is one ninth of the total delivered power by the proposed three-phase solid-state transformer. However, by using the proposed method, the healthy operation was fully restored. Therefore, the output stage input voltage, input current, and output active power converged to 400 V, 20 A, and 8 kW, which are the same values of the steady state response in the healthy operation. Additionally, Figure 4.10 and Figure 4.11 display the waveforms for the output stage output voltages and output currents vs. time. According to these two figures, the output voltages of the output stage always have the same amplitude and phase angle of the grid voltages, and the output currents of the output stage are converged to 31.427 A. They are the same values of the steady state response in the healthy operation.

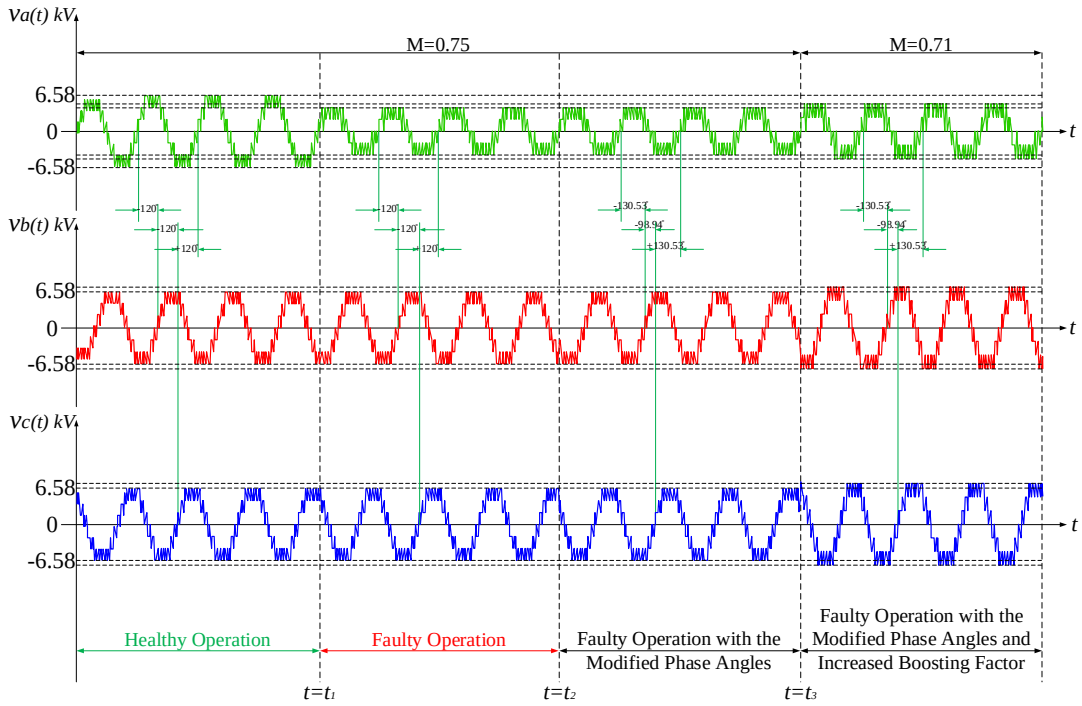


Figure 4.4. Performance of the proposed fault-tolerant method for the QZSI switch fault case with a single faulty switch in phase "a": phase voltages of the high voltage side for the isolation stage.

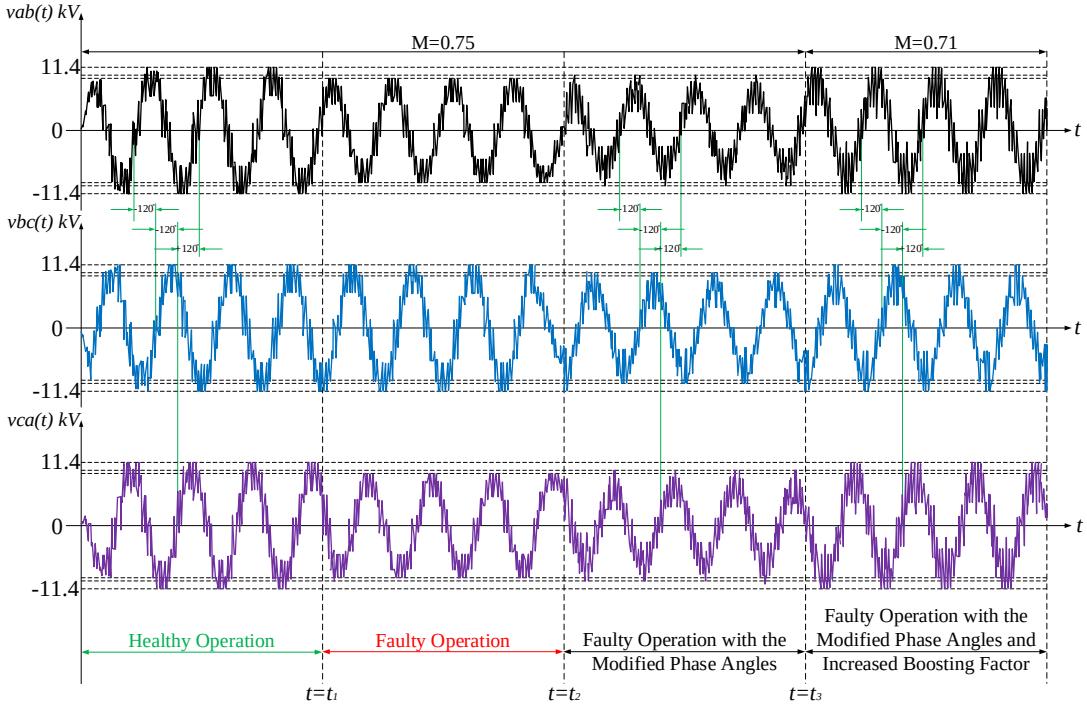


Figure 4.5. Performance of the proposed fault-tolerant method for the QZSI switch fault case with a single faulty switch in phase "a": line-to-line voltages of the high voltage side for the isolation stage.

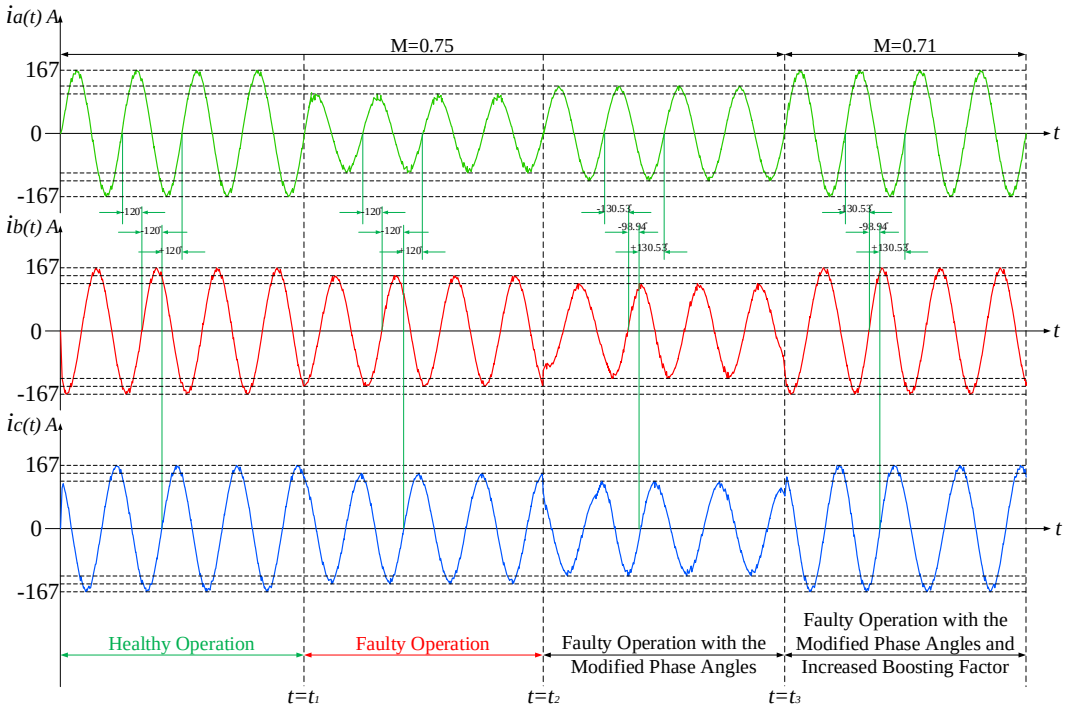


Figure 4.6. Performance of the proposed fault-tolerant method for the QZSI switch fault case with a single faulty switch in phase "a": line currents of the high voltage side for the isolation stage.

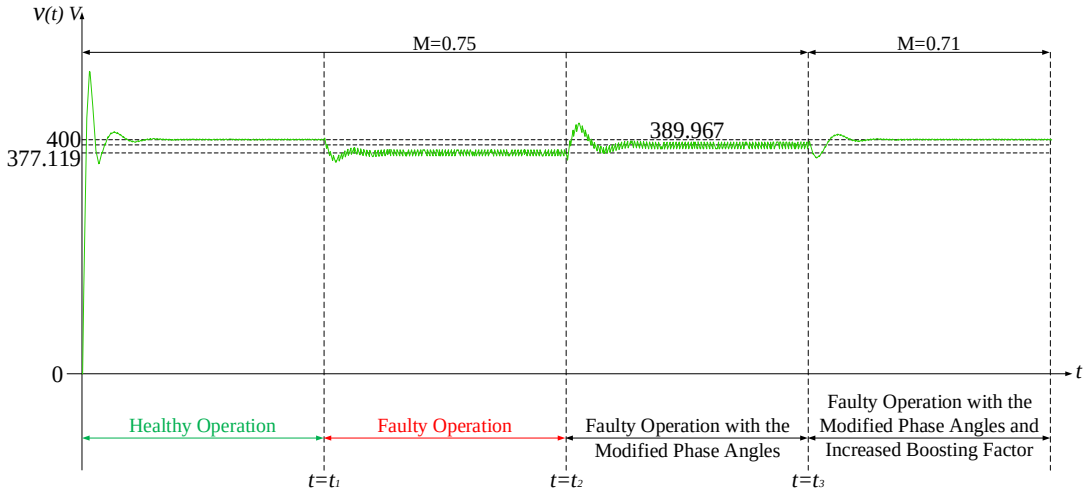


Figure 4.7. Performance of the proposed fault-tolerant method for the QZSI switch fault case with a single faulty switch in phase "a": input voltages of the output stage.

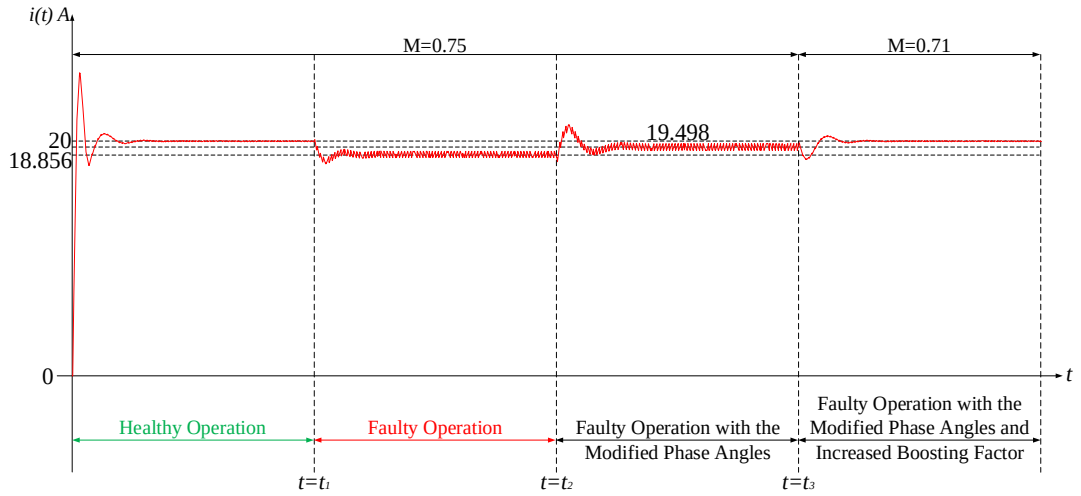


Figure 4.8. Performance of the proposed fault-tolerant method for the QZSI switch fault case with a single faulty switch in phase "a": input current of the output stage.

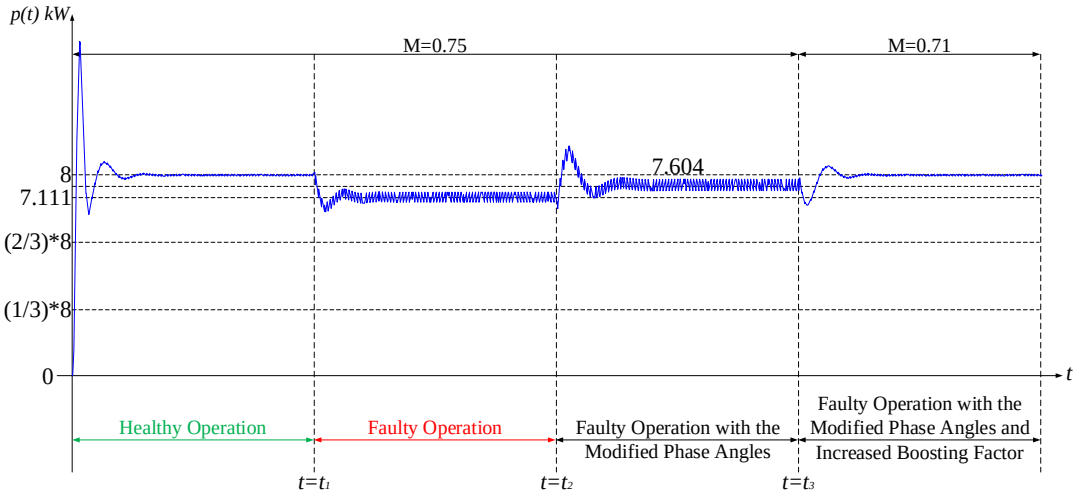


Figure 4.9. Performance of the proposed fault-tolerant method for the QZSI switch fault case with a single faulty switch in phase "a": output active power of the output stage.

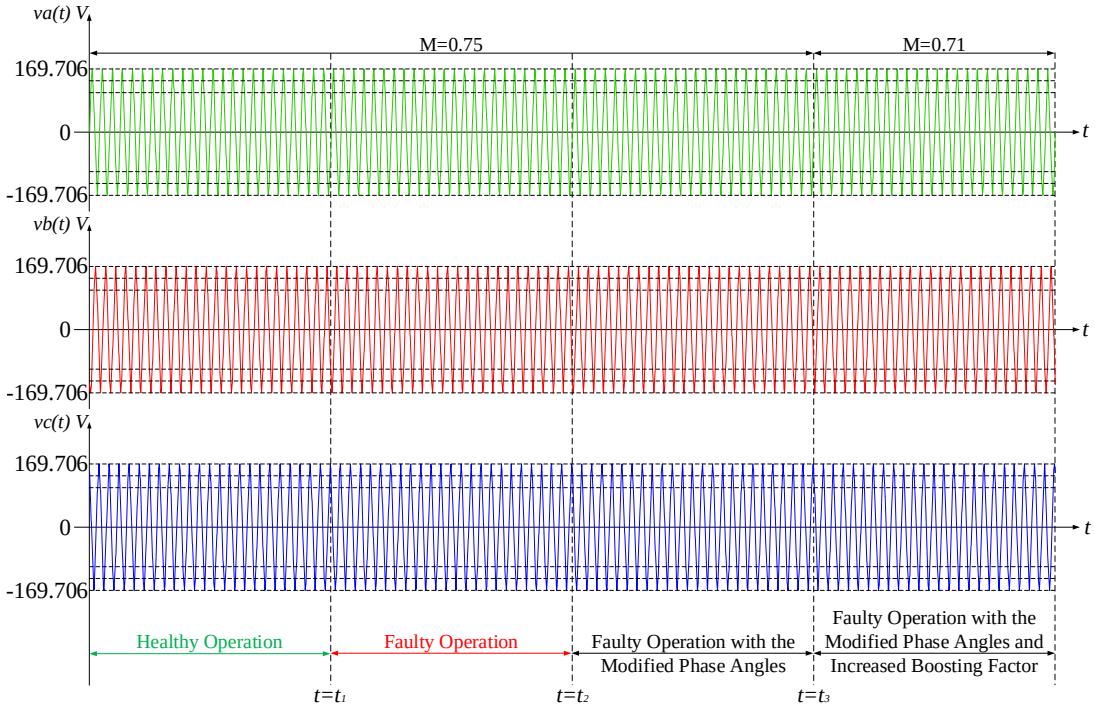


Figure 4.10. Performance of the proposed fault-tolerant method for the QZSI switch fault case with a single faulty switch in phase "a": output voltages of the output stage.

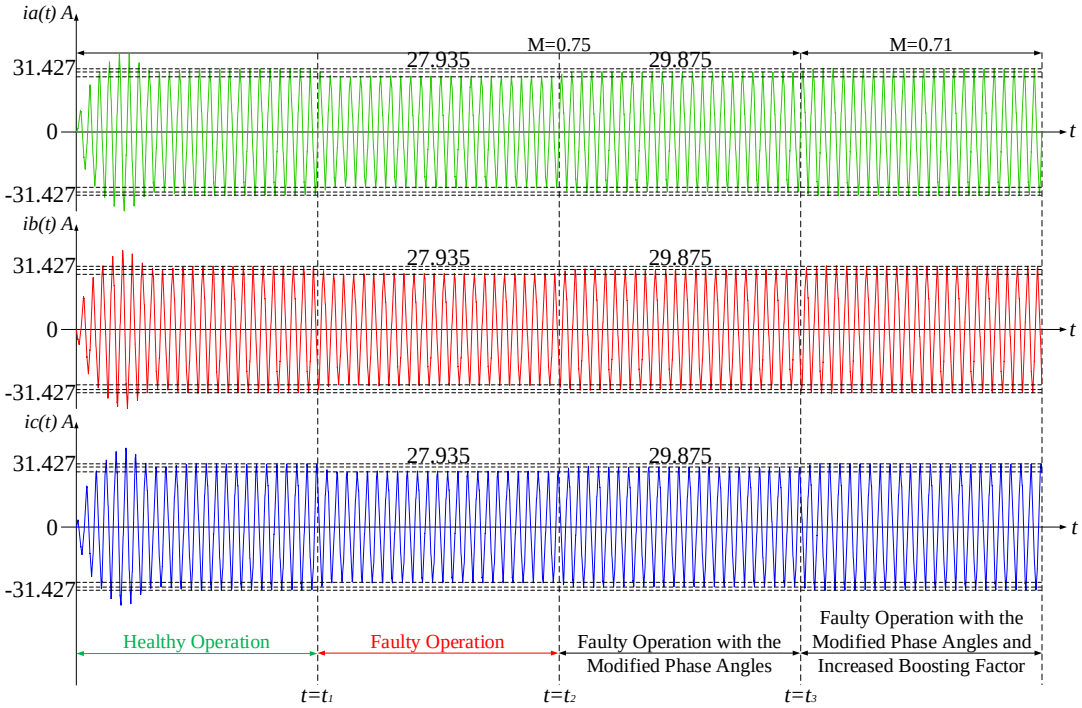


Figure 4.11. Performance of the proposed fault-tolerant method for the QZSI switch fault case with a single faulty switch in phase "a": output currents of the output stage.

4.2.2 The Analysis of High Voltage AC Grid Faults (HVAC Grid Faults)

The second analysis is the high voltage grid fault occurrence in phase "a". The first step is to bypass the faulty phase, which is phase "a". As a result, the remaining healthy phases will be two phases, phase "b" and phase "c". Therefore, the generated line-to-line voltages will be unbalanced. In this condition, to balance the generated line-to-line voltages, the phase shifts between the generated phase voltages of the multilevel cascaded quasi-z-source inverter stage have to be modified to their obtained values in chapter 3. In this case study, the modified phase angles are $\theta_{ab}' = \theta_{ca}' = 150^{o}$, and $\theta_{bc}' = 30^{o}$ which will balance the generated line-to-line voltages. However, the amplitude of the new balanced generated line-to-line voltages is lower than the amplitude of the generated line-to-line voltages during the healthy operation. Subsequently, to balance the generated line-to-line voltages with the same pre-fault voltage amplitude of 5.1962 p.u, the fault gain (F_{ON}) is calculated based on (3.11) and is found as $\sqrt{3}$ = 1.7321. Finally, using the new fault gain with the modified phase shifts (using the phase shifted pulse width modulation) to fully restore the healthy operation of the proposed three-phase solid-state transformer to the pre-fault conditions. The generated phase voltages and the generated line-to-line voltages are summarized in Table 4-4 in the per unit values and actual values, where the base value is (2.2 kV).

Table 4-4: Calculated phase voltages and line-to-line voltages using the proposed method

	Phase Voltages			Line-to-Line Voltages		
Amplitude	V_a''	V_b'	V_c'	V_{ab}''	V_{bc}''	V_{ca}''
V_p (p.u)	0	5.1962	5.1962	5.1962	5.1962	5.1962
V_p (kV)	0	11.4315	11.4315	11.4315	11.4315	11.4315

The proposed three-phase solid-state transformer was tested under the high voltage AC grid faults in the case of a single line-to- ground fault on phase "a" of the HVAC grid to confirm the

validity of the work for the proposed method by comparing the calculated values with the measured values. The analysis was divided similarly to the analysis of the previous fault.

Healthy operation at ($0 \le t < t_1$): This operation is explained in the previous section, and it will be used as a reference for analyzing this type of fault. The generated phase voltages, the generated line-to-line voltages, and the line currents of this stage during this operation are shown in Figure 4.12, Figure 4.13, and Figure 4.14 respectively. The measured voltages during this operation are compared to the calculated voltages and summarized in Table 4-5. Also, they will be compared with the rebalanced calculated and measured voltages after implementing the proposed method in the same table.

Faulty operation at ($t_1 \le t < t_2$): During this period of the operation, there is a single line-to-ground fault on phase "a" of the HVAC grid. The faulty phase "a" was bypassed, therefore, the generated voltage of phase "a" is always zero while the other two phase voltages have all seven voltage levels. As pictured in Figure 4.12 and Figure 4.13, the amplitude of the generated phase voltages is unequal, and the amplitude of generated line-to-line voltages is unequal too. Therefore, the operation of the multilevel cascaded quasi-z-source inverter stage is unbalanced. The line currents of this stage during this operation are shown in Figure 4.14.

Faulty operation with modified phase angles at ($t_2 \le t < t_3$): To balance the generated line-to-line voltages, the first step of the proposed fault tolerant method is applied in this period of the operation. The phase shift angles between the waves of the generated phase voltages are adjusted to be $\theta_{ab}' = \theta_{ca}' = 150^{o}$ and $\theta_{bc}' = 30^{o}$ using the proposed method. As pictured in Figure 4.12 and Figure 4.13, the amplitude of the generated phase voltages is not equal, but the amplitude of generated line-to-line voltages is equal. However, it is lower than the amplitude of the generated line-to-line voltages in the healthy operation, but the operation of the proposed three-phase solid-

state transformer is balanced. Even though the operation is balanced, it needs to fully restore the healthy operation by boosting the generated line-to-line voltages to be the same values as the generated line-to-line voltages in the healthy operation. The line currents of this stage during this operation are shown in Figure 4.14.

Faulty operation with the modified phase angles and increased boosting factor (B) at ($t \geq t_3$): To fully restore the healthy operation, the boosting factor was increased as a second step of the proposed method by increasing the shoot-through duty ratio to the new minimized value was calculated in chapter 3. As pictured in Figure 4.12 and Figure 4.13, even though the amplitude of the generated phase voltages is unequal, the amplitude of generated line-to-line voltages is equal to the same amplitude of the generated line-to-line voltages in the healthy operation. Hence, the operation of the multilevel cascaded quasi-z-source inverter stage is balanced is balanced. The measured voltages are compared to the calculated voltages during this operation and in the healthy operation as summarized in Table 4-5.

Table 4-5: Validity of the proposed method to fully restore the healthy operation

	Healthy operation ($0 \leq t < t_1$)			Faulty operation with modified phase angles and increased boosting factor (B) ($t \geq t_3$)		
	Calculated Amplitude		Measured Amplitude	Calculated Amplitude		Measured Amplitude
	V_p (p.u)	V_p (kV)	V_p (kV)	V_p (p.u)	V_p (kV)	V_p (kV)
V_a	3	6.6	6.58	0	0	0
V_b	3	6.6	6.58	5.1962	11.4315	11.4
V_c	3	6.6	6.58	5.1962	11.4315	11.4
V_{ab}	5.1962	11.4315	11.4	5.1962	11.4315	11.4
V_{bc}	5.1962	11.4315	11.4	5.1962	11.4315	11.4
V_{ca}	5.1962	11.4315	11.4	5.1962	11.4315	11.4

The line currents of this stage during this operation are shown in Figure 4.14. According to Table 4-5, it is clear that all measured voltages are very close to their calculated values. Additionally, the measured generated line-to-line voltages are rebalanced again with the same pre-fault values, which confirms the validity of the proposed method. As a result, the capability of the controller in the output stage is achieved to control the input voltage, the input current, the output active power, which are shown in Figure 4.15, Figure 4.16, and Figure 4.17 respectively. Also, the capability of the controller to synchronize the output voltage of the output stage with the grid is achieved as shown in Figure 4.18. The injected currents to the grid are shown in Figure 4.19. Figure 4.15, Figure 4.16, and Figure 4.17 display the waveforms for the output stage input voltage, input current, and output active power vs. time. According to these figures, during the switch fault, the delivered power by phase "a" is lost, which is one third of the total delivered power by the proposed three-phase solid-state transformer. However, by using the proposed method, the healthy operation was fully restored. Therefore, the output stage input voltage, input current, and output active power converged to 400 V, 20 A, and 8 kW, which are the same values of the steady state response in the healthy operation. Additionally, Figure 4.18 and Figure 4.19 display the waveforms for the output stage output voltages and output currents vs. time. According to these two figures, the output voltages of the output stage always have the same amplitude and phase angle of the grid voltages, and the output currents of the output stage are converged to 31.427 A. They are the same values of the steady state response in the healthy operation.

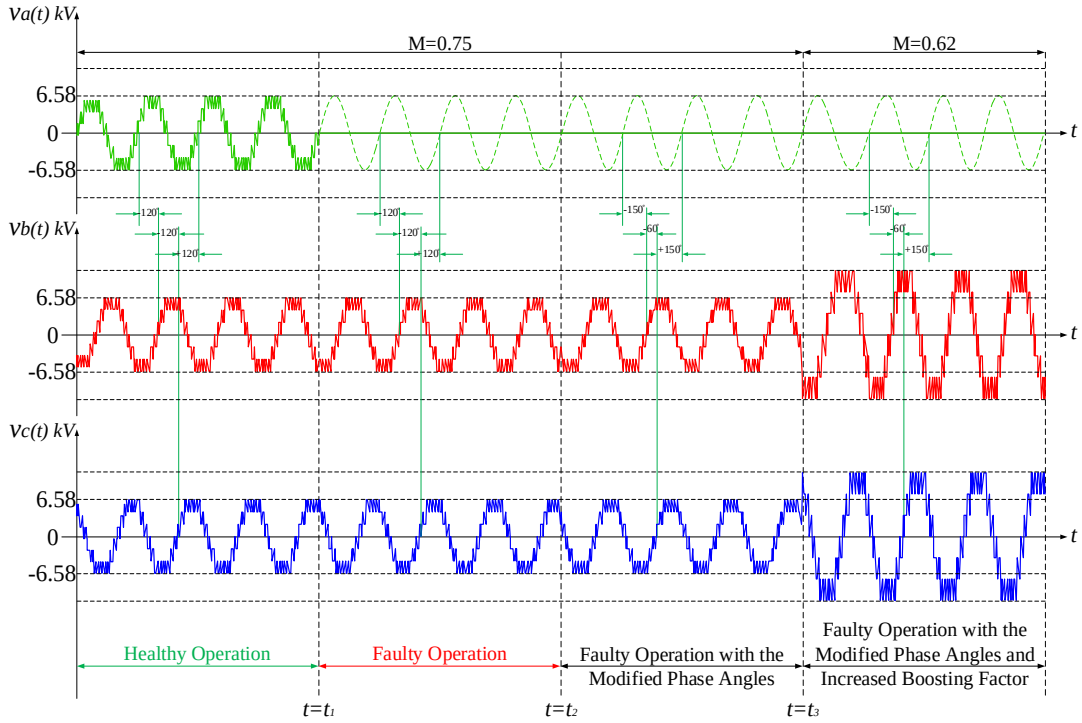


Figure 4.12. Performance of the proposed fault-tolerant method for the HVAC grid fault case with a single line-to-ground fault in phase "a": phase voltages of the high voltage side for the isolation stage.

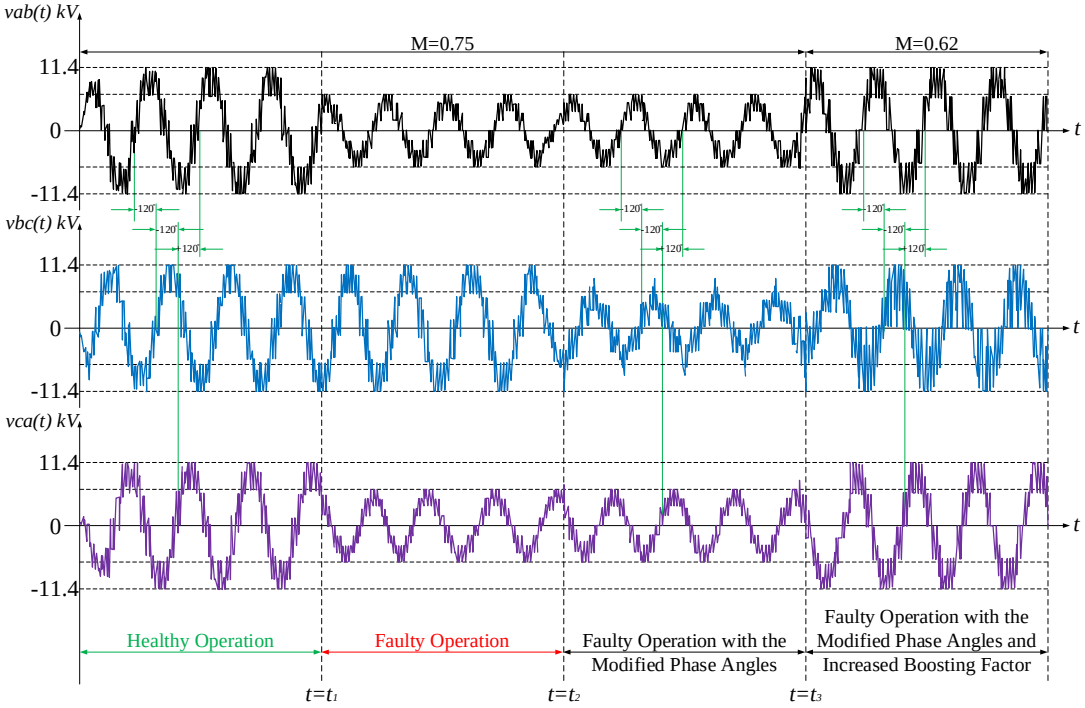


Figure 4.13. Performance of the proposed fault-tolerant method for the HVAC grid fault case with a single line-to-ground fault in phase "a": line-to-line voltages of the high voltage side for the isolation stage.

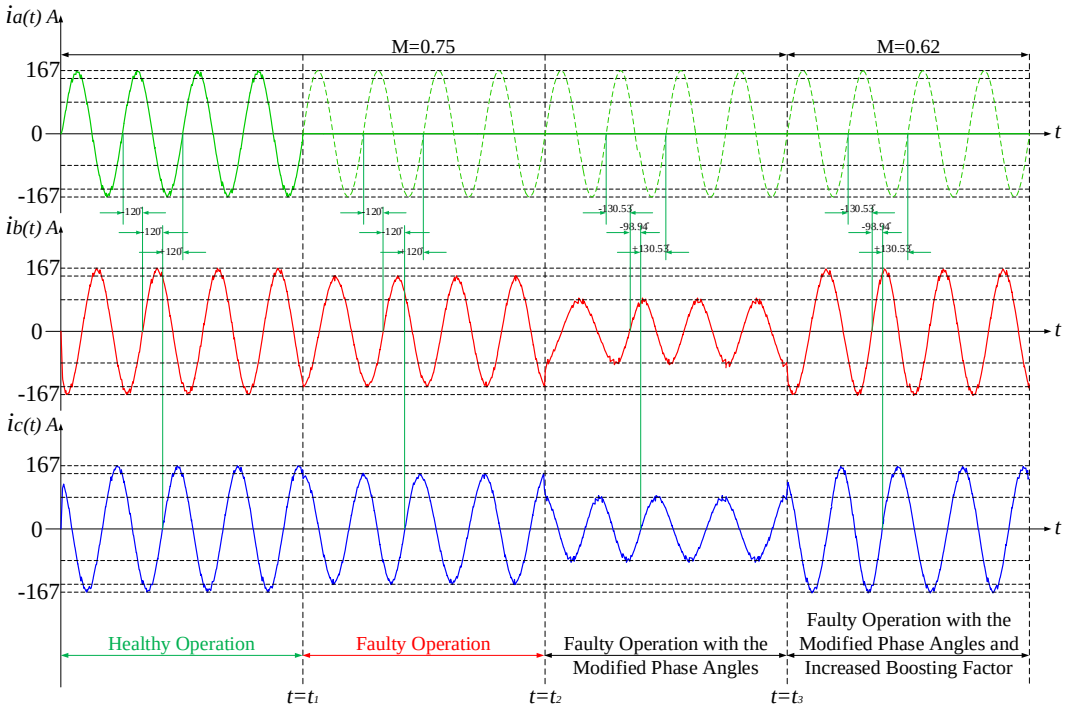


Figure 4.14. Performance of the proposed fault-tolerant method for the HVAC grid fault case with a single line-to-ground fault in phase "a": line currents of the high voltage side for the isolation stage.

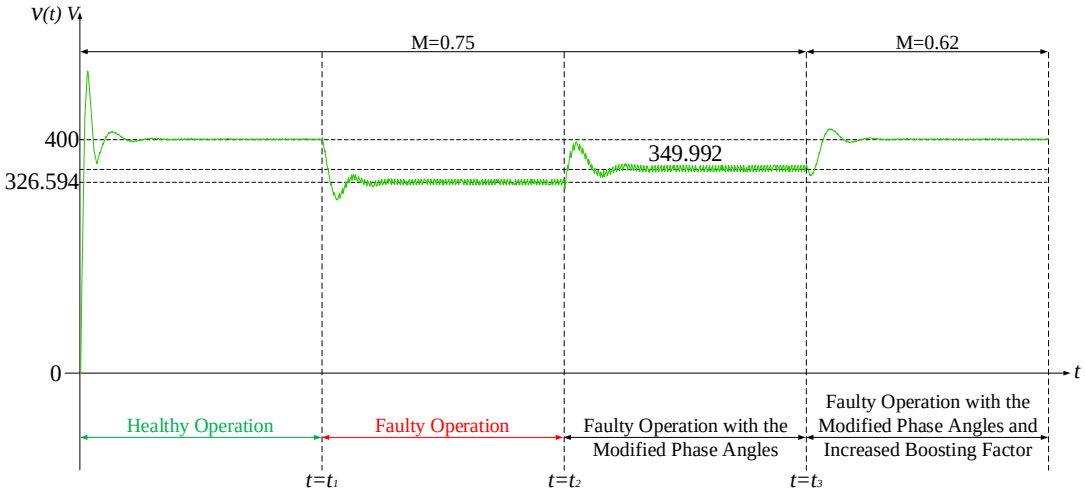


Figure 4.15. Performance of the proposed fault-tolerant method for the HVAC grid fault case with a single line-to-ground fault in phase "a": input voltages of the output stage.

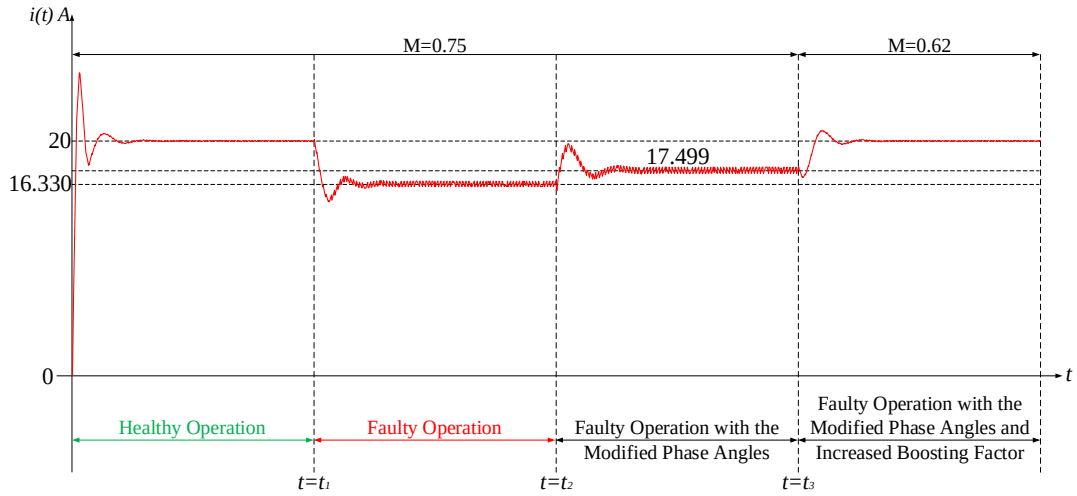


Figure 4.16. Performance of the proposed fault-tolerant method for the HVAC grid fault case with a single line-to-ground fault in phase "a": input current of the output stage.

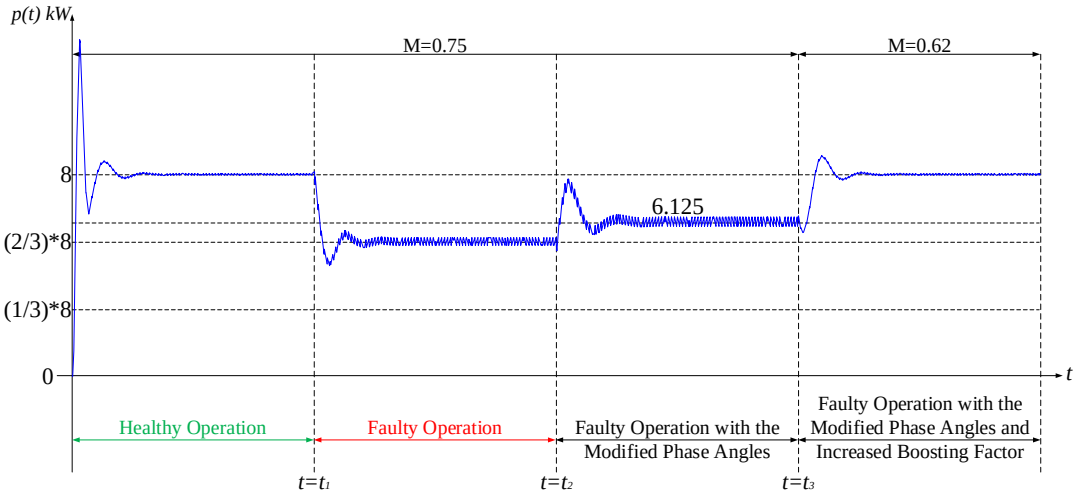


Figure 4.17. Performance of the proposed fault-tolerant method for the HVAC grid fault case with a single line-to-ground fault in phase "a": output active power of the output stage.

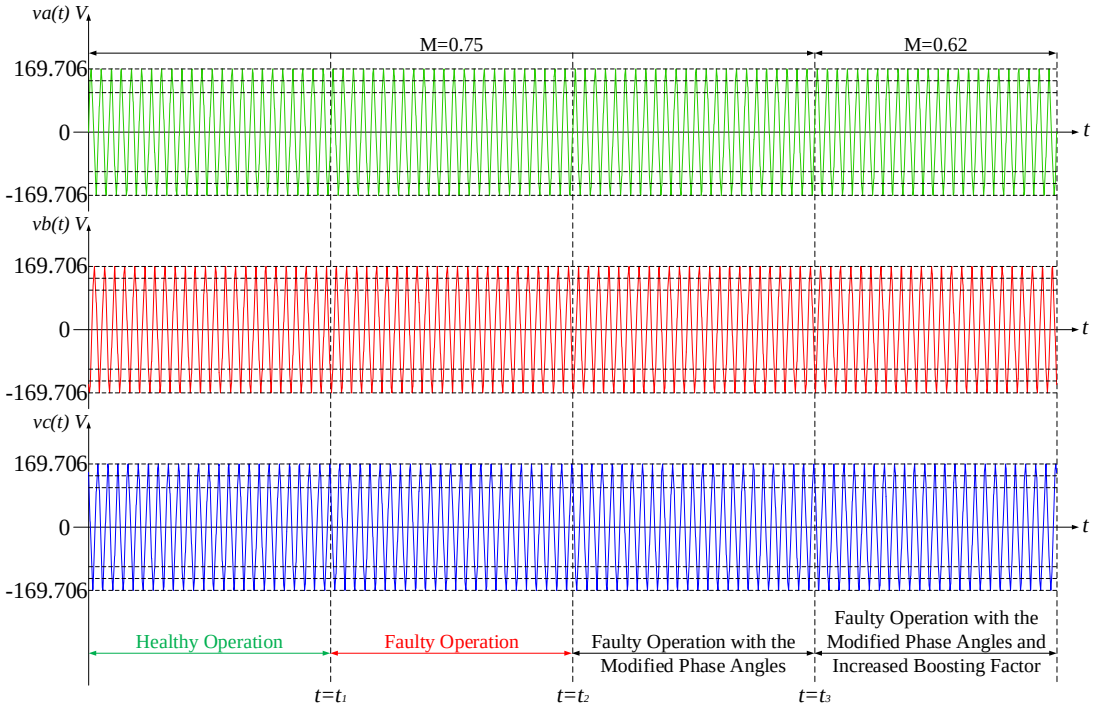


Figure 4.18. Performance of the proposed fault-tolerant method for the HVAC grid fault case with a single line-to-ground fault in phase "a": output voltages of the output stage.

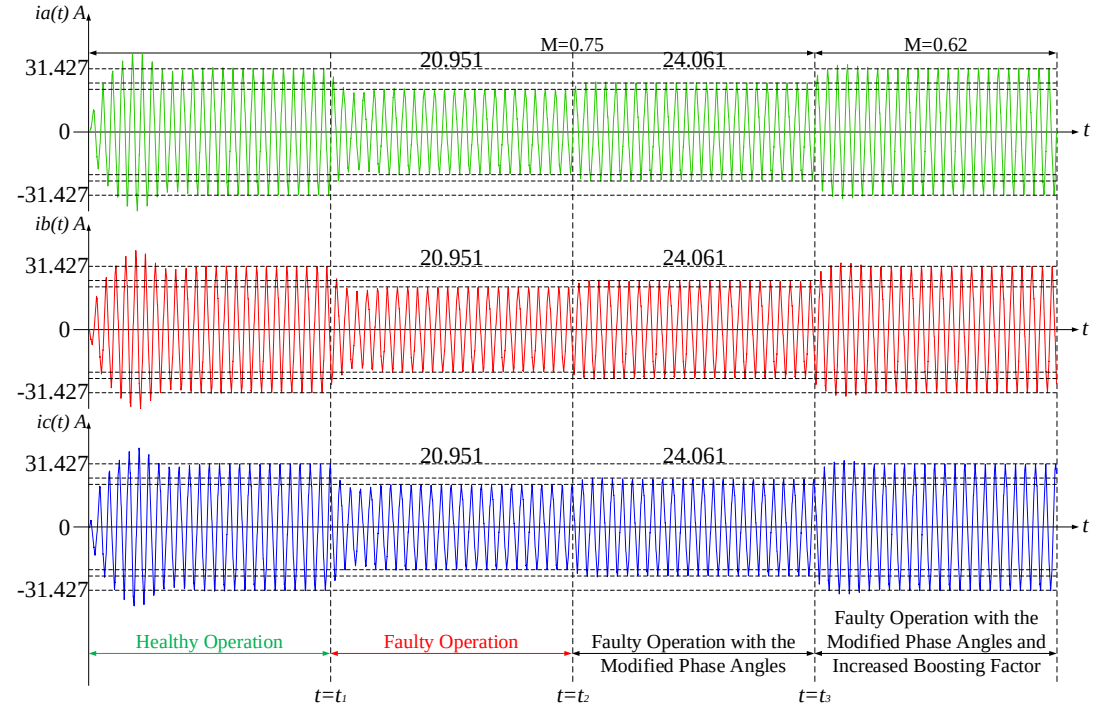


Figure 4.19. Performance of the proposed fault-tolerant method for the HVAC grid fault case with a single line-to-ground fault in phase "a": output currents of the output stage.

Chapter 5

5.1 Conclusion

The proposed solid-state transformer was developed by replacing a traditional inverter in the high voltage side of the isolation stage with quasi-z-source inverter topology to work as a DC/AC multilevel cascaded h-bridge converter. The characteristics of quasi-z-source inverter topology are employed to improve the reliability and the ability of the proposed solid-state transformer. Therefore, the healthy operation can be fully restored. Also, the stress on the high voltage stage cells was distributed between all cells in the three phases of the high voltage stage. Then the lifetime of the proposed solid-state transformer was able to be increased.

The new modulation method was proposed to offer appropriate control required by the isolation stage in the proposed solid-state transformer. In this research, the traditional phase shifted pulse width modulation (PS-PWM) was modified to make the control system comparable to the other control methods such as a simple boost control and maximum boost control. The proposed method works well to make the total harmonic distortion of the generated voltages acceptable.

The fault-tolerant strategy was introduced to the proposed solid-state transformer in order to improve its operation to overcome the faulty conditions. In implementing the proposed fault-tolerant strategy, the function of faulty cells can be fully compensated for without needing any extra switches or backup power cells. Therefore, the line-to-line voltages can be rebalanced again

with minimum total harmonic distortions of the generated voltages in the faulty conditions. The proposed strategy can be easily implemented, but it requires a number of remaining healthy cells to compensate for the faulty cells.

This research was focused on how to restore the normal operation of the proposed solid-state transformer in the case of two type of faults, quasi-z-source inverter switch faults (QZSI switch faults) and high voltage AC grid faults (HVAC grid faults). The normal operation was restored by integrating the quasi-z-source inverter topology into the SST topology to develop a new SST topology in conjunction with a proposed fault-tolerant method that can fully rebalance transformer voltages in the case of the two aforementioned fault scenarios.

The quasi-z-source inverter switch fault (QZSI switch fault) was solved by bypassing altogether the h-bridge with a faulty switch using the function of other healthy switches. Therefore, the generated AC voltage output of the isolation stage will be symmetrical, but the amplitude of the faulty phase will be lower than the other two healthy phases. Then restoring the healthy operation can be done by two proposed methods. It can be restored by only increasing the voltage amplitude of the remaining healthy h-bridges in the faulty phase. However, this solution increases the voltage stress over the healthy switches in the faulty phase. Subsequently, it may lead to more switch failures especially in high voltage applications. Hence, to overcome the drawback of increasing the stress, the proposed fault-tolerant strategy was introduced and the phase angles of the QZSI CHB converter phase voltages were modified to balance the generated line-to-line voltages. However, the amplitude of the new line-to-line voltages is lower than the line-to-line voltages during the healthy operation. Therefore, in order to fully restore the healthy operation, the voltage amplitude was increased for the remaining healthy h-bridges in all three phases. Also, the

extra switching stress can be distributed over all remaining healthy switches in the three phases of this stage.

The high voltage AC grid faults (HVAC grid fault) can be remedied by utilizing the features of the proposed solid-state transformer. Even though the type and severity of the fault affected the three-phase input voltage of the input stage, the proposed solid-state transformer had the ability to overcome this type of fault. In the case of a single line-to-ground fault, the fault is remedied similar to the previous fault. The single line-to-ground fault can be considered as the quasi-z-source inverter switch fault, but there is a fault in all switches in faulty phase. However, restoring the healthy operation cannot be done by only increasing the voltage amplitude of the remaining healthy h-bridges because there are no remaining healthy cells in the faulty phase. Therefore, after bypassing the faulty phase, the phase angles of the QZSI CHB converter of the two remaining healthy phase voltages were modified to balance the generated line-to-line voltages but with lower amplitude of the line-to-line voltages in the healthy operation. Then the healthy operation of the proposed solid-state transformer was restored by using the QZSI boosting capability with the proposed fault-tolerant strategy to increase the voltage amplitude for the healthy cells of the other two remaining healthy phases.

Finally, the proposed controller for the output stage of the proposed SST was introduced to control the output active power and to compensate for the reactive power. It works well to synchronize the output voltage to the grid as well. The proposed method offers a better performance comparable to conventional control methods. The capability of delivering the same power after the fault by the proposed solid-state transformer is restored completely with faster dynamic behavior and a better steady-state response.

5.2 Future Work

The proposed methods in this research have opened future studies to improve and analyze challenges for the use of a solid-state transformer in various applications. The future work of this research can be listed as follows:

- Investigating more fault scenarios and evaluating performance of the proposed methods in various fault situations.
- Investigating the safety requirements of the proposed solid-state transformer under different fault scenarios.
- Studying the effectiveness of employing various modulation methods on the total harmonic distortion of the generated voltages by the proposed solid-state transformer.
- Exploring the behavior of the solid-state transformer by replacing the quasi-z-source inverter topology in the isolation stage with different converter topologies.
- Employing the proposed solid-state transformer to work as compensator for the reactive power of the grid.

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