New Topology and Improved Control of Modular Multilevel Based Converters

By

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Submitted to the graduate degree program in Department of Electrical Engineering and Computer Science and the Graduate Faculty of the University of Kansas in partial fulfillment of the requirements for the degree of Doctor of Philosophy.

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Date Defended: 5 December 2019

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Date Approved: 5 December 2019

Abstract

Trends toward large-scale integration and the high-power application of green energy resources necessitate the advent of efficient power converter topologies, multilevel converters. Multilevel inverters are effective solutions for high power and medium voltage DC-to-AC conversion due to their higher efficiency, provision of system redundancy, and generation of near-sinusoidal output voltage waveform. Recently, modular multilevel converter (MMC) has become increasingly attractive. To improve the harmonic profile of the output voltage, there is the need to increase the number of output voltage levels. However, this would require increasing the number of submodules (SMs) and power semi-conductor devices and their associated gate driver and protection circuitry, resulting in the overall multilevel converter to be complex and expensive. Specifically, the need for large number of bulky capacitors in SMs of conventional MMC is seen as a major obstacle. This work proposes an MMC-based multilevel converter that provides the same output voltage as conventional MMC but has reduced number of bulky capacitors. This is achieved by introduction of an extra middle arm to the conventional MMC. Due to similar dynamic equations of the proposed converter with conventional MMC, several previously developed control methods for voltage balancing in the literature for conventional MMCs are applicable to the proposed MMC with minimal effort. Comparative loss analysis of the conventional MMC and the proposed multilevel converter under different power factors and modulation indexes illustrates the lower switching loss of proposed MMC. In addition, a new voltage balancing technique based on carrier-disposition pulse width modulation for modular multilevel converter is proposed.

The second part of this work focuses on an improved control of MMC-based high-power DC/DC converters. Medium-voltage DC (MVDC) and high-voltage DC (HVDC) grids have been the focus of numerous research studies in recent years due to their increasing applications in

rapidly growing grid-connected renewable energy systems, such as wind and solar farms. MMC-based DC/DC converters are employed for collecting power from renewable energy sources. Among various developed DC/DC converter topologies, MMC-based DC/DC converter with medium-frequency (MF) transformer is a valuable topology due to its advantages. Specifically, they offer a significant reduction in the size of the MMC arm capacitors along with the ac-link transformer and arm inductors due to the ac-link transformer operating at medium frequencies. As such, this work focuses on improving the control of isolated MMC-based DC/DC (IMMDC) converters. The single phase shift (SPS) control is a popular method in IMMDC converter to control the power transfer. This work proposes conjoined phase shift-amplitude ratio index (PSAR) control that considers amplitude ratio indexes of MMC legs of MF transformer's secondary side as additional control variables. Compared with SPS control, PSAR control not only provides wider transmission power range and enhances operation flexibility of converter, but also reduces current stress of medium-frequency transformer and power switches of MMCs. An algorithm is developed for simple implementation of the PSAR control to work at the least current stress operating point. Hardware-in-the-loop results confirm the theoretical outcomes of the proposed control method.

Dedication

To my lovely little sister;

And to my family for their help, patience, and motivation.

Acknowledgements

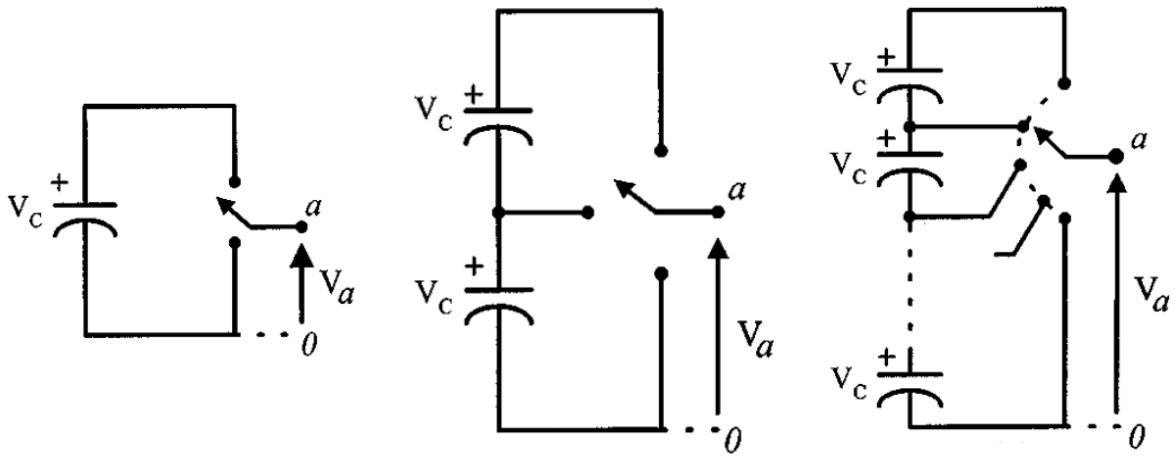
I am grateful to my advisor Dr. Reza Ahmadi, whose guidance, support, motivation and expertise have helped me a lot in this process. I highly appreciate Prof. Parsad Kulkarni for agreeing to serve as the committee chair. Many thanks to Prof. Glenn Prescott, Dr. James Stiles, Dr. Alessandro Salandrino, and Dr. Xiaoli (Laura) Li for their great feedback and being in my thesis committee.

I also like to thank all my friends and my lab mates at Power Electronics lab for the time we spent together. I feel very lucky to have great friends whom I had always enjoyed my time with. In addition, I would like to thank the department faculty and staff for the friendly environment that I experienced at University of Kansas. I like to thank Dr. David O. Johnson for the great time that I had working as his GTA. I also like to thank my master's advisor, Prof. Mohammad Ardebili at K. N. Toosi University of Technology who had always been more than kind to me.

Table of Contents

Chapter I: Introduction and Literature Review

For past decade renewable energy sources have been the focus of many research and investigation. Trends toward large-scale integration and the high-power application of green energy resources necessitate the advent of efficient power converter topologies, multilevel inverters. The main component of multilevel inverters can be considered as power semiconductor switches and capacitor voltage sources or direct current (DC) voltage sources [1-5]. By turning ON/OFF the switches with gating signals, different capacitor voltage sources can be added to or bypassed from the circuit of output voltage. Adding/removing these capacitor voltage sources will result in generating different desirable output voltages. Multilevel inverters provide several advantages over conventional two-level inverters. Fig. 1 shows three DC to alternative current (AC) inverters with different output voltage levels. The output voltage is measured with respect to negative terminal of the voltage source. Fig. 1(a) shows a two-level inverter that generates output voltage with two values, while Fig. 1(b) depicts a three-level inverter, and Fig. 1(c) a general *n*-level inverter. It must be noted the term multilevel is defined for inverters with three-level and more. Fig 2 shows the corresponding normalized output voltage waveform of each of the three mentioned inverters. It can be seen as the number of levels in the generated output voltage increases, the output voltage waveform will be more close to a sinusoidal waveform. Increasing the number of levels would decrease the total harmonic distortion (THD) of the output voltage waveform. Therefore, multilevel inverters are effective solutions for high power and medium voltage DC-to-AC conversion due to their higher efficiency, provision of system redundancy, and generation of near-sinusoidal output voltage waveforms [1-5].



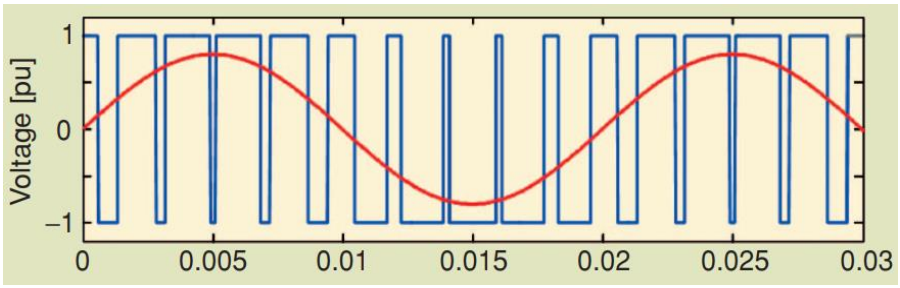
(a) (b) (c)

Fig. **1**. (a) Two-level inverter, (b) three-level inverter, and (c) *n*-level inverter [1]

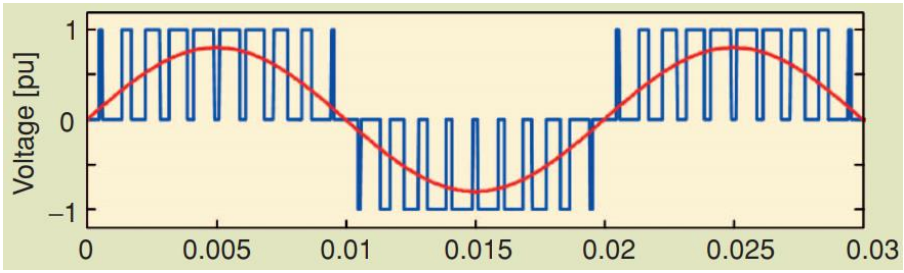
These characteristics of the multilevel inverters have led researchers in power electronics area to work on improving the performance of multilevel inverters. These efforts include optimization based design and control [6, 7], voltage balancing techniques of the capacitor voltage sources [8, 9], harmonic elimination methods [10], advanced control strategies [11, 12], new multilevel inverter topologies [13, 14], and so on.

1.1 Limitations of Classical Multilevel Topologies

Among many proposed multilevel topologies, the neutral-point-clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) converters are the most well-known classical multilevel topologies. The NPC converter also named diode-clamped converter, proposed by Nabae *et al.* [15], is shown in Fig. 3. Fig. 3 (a) and (b) show a three-level NPC and a 5-level NPC, respectively. A *k*-level NPC converter has *k*-1 capacitor voltage sources on the DC bus. The middle



(a)



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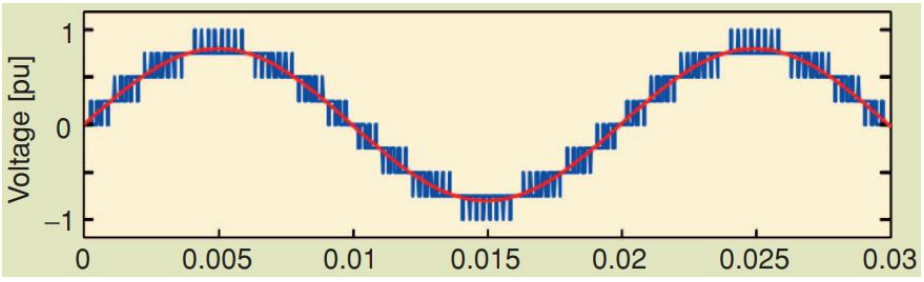


(c)

Fig 2. Normalized output phase voltage waveform of (a) two-level inverter, (b) three-level inverter, and (c) *n*-level inverter (*n* is assumed to be 9). [3]

point between the top and bottom capacitors can be defined as the neutral point *n*. The clamping diodes complete the circuit between the middle point of transistors and the neutral point *n*. The three-level NPC shown in Fig. 3 (a) can generate output voltages of $+\frac{V_{dc}}{2}$, 0, and $-\frac{V_{dc}}{2}$. The DC-bus has two capacitors where the voltage across each capacitor is $+\frac{V_{dc}}{2}$. It must be noted switches S_1 and S_2 act complementary to switches $\overline{S_1}$ and $\overline{S_2}$; respectively. For generating output voltage of

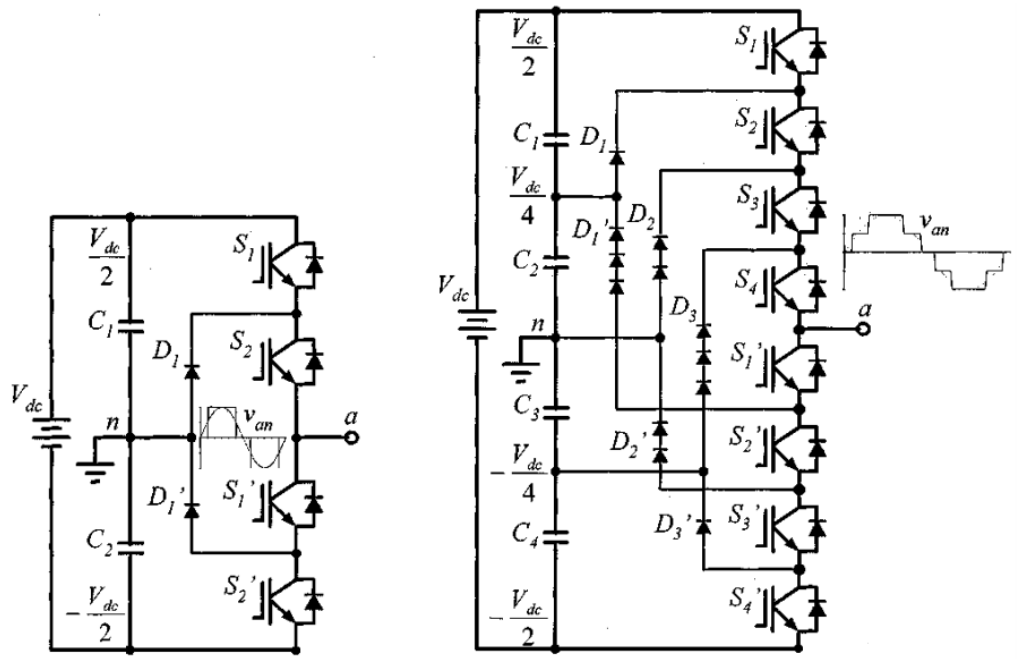


Fig. 3. Power circuit of (a) three-level NPC (b) five-level NPC [1]

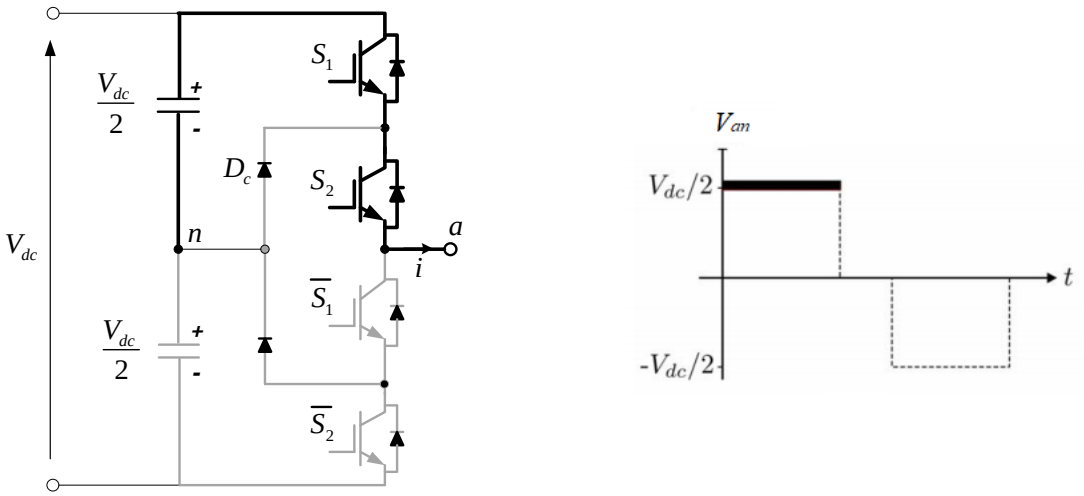
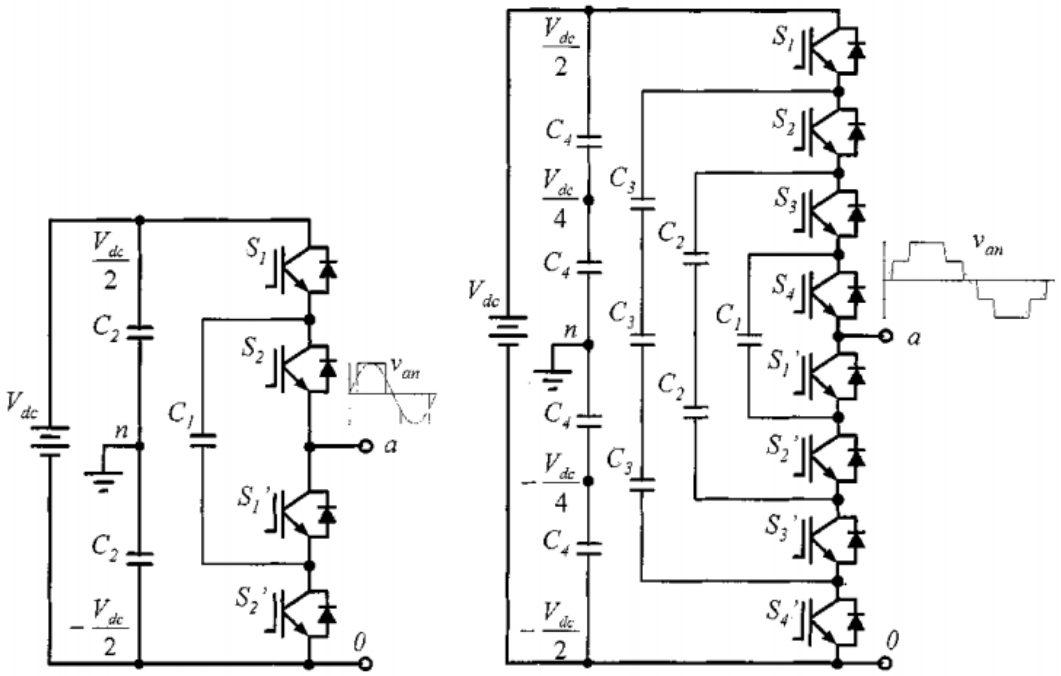


Fig. 4. Conduction path of three-level NPC for generating $+\frac{V_{dc}}{2}$ voltage level.

$+\frac{V_{dc}}{2}$ switches S_1 and S_2 need to be turned on, while for output voltage of $-\frac{V_{dc}}{2}$ switches $\bar{S_1}$ and $\bar{S_2}$, and for output voltage of 0 switches $\bar{S_1}$ and S_2 need to be turned on. The conduction path for generating the voltage level of $+\frac{V_{dc}}{2}$ is shown in Fig. 4 as an example where the semiconductor switches S_1 and S_2 are turned on, while their contemporary switches are turned off. Regarding the direction of output current, either the bolded transistor or its anti-parallel diode will conduct. If the output current *i* is positive, it will pass through the transistors, and if it is negative, it will pass through the corresponding anti-parallel diodes.

It must be mentioned for generation of output voltages with higher number of levels than five, the number of required clamping diodes in NPC increases rapidly. For generating output voltage with *k*-level, number of required clamping diode is $(k-1)\times(k-2)$. Hence, with high values of *k* the circuit implementation will be impractical. Also NPC converter suffer from significant capacitor voltage balancing problem when delivering active power [16]. The unbalance in capacitor voltages occur as charging time (for rectifier operation) or discharging time (for inverter operation) is different for each capacitor. The voltage unbalance problem can be solved by using controlled DC voltage sources or batteries, but this will add to cost and complexity of the system.

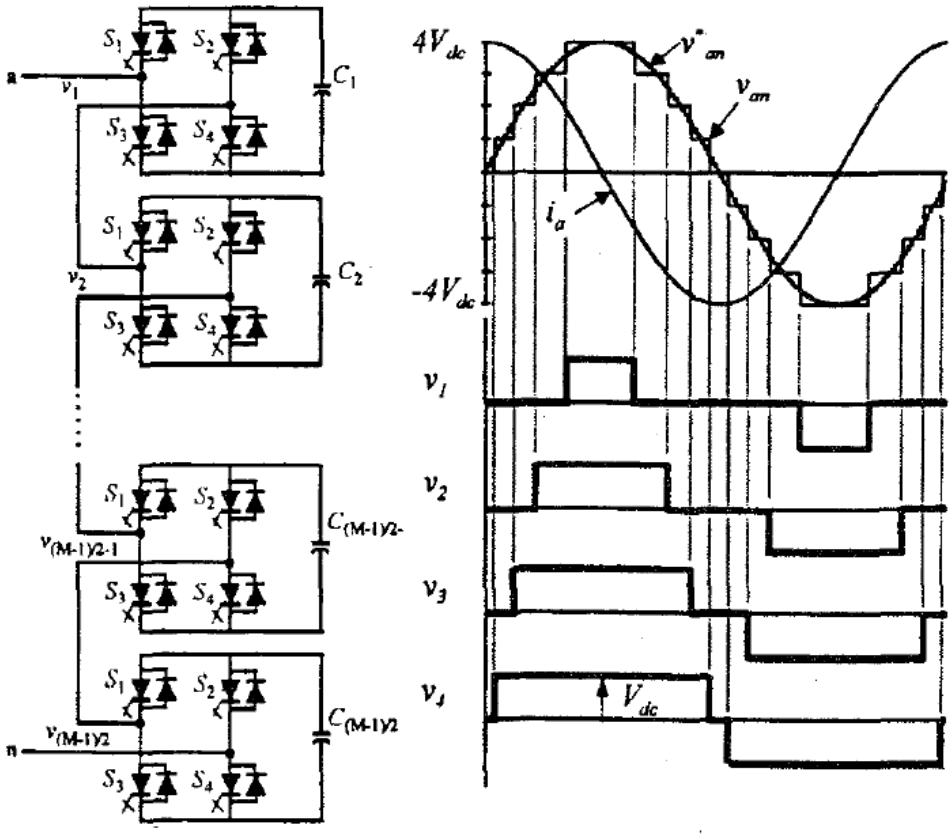
Fig. 5 shows the circuit for a three-level and five-level FC converter. Similar to NPC converter, a *k*-level FC converter has *k*-1 capacitor voltage sources on the DC bus. The advantageous of FC converter over NPC converter is it has more available switching combinations to generate the same output voltage level. For generating output voltage of $+\frac{V_{dc}}{2}$ switches S_1 and S_2 need to be turned on, while for output voltage of $-\frac{V_{dc}}{2}$ switches $\bar{S_1}$ and $\bar{S_2}$, and for output voltage of 0 switches either combinations of $\bar{S_1}$ and S_2 or S_1 and $\bar{S_2}$ need to be turned on.



(a) (b)

Fig. 5. Power circuit of (a) three-level FC (b) five-level FC [1]

It must be mentioned beside difficulty for balancing voltage of capacitors in case of active power delivery, FC would require high numbers of capacitors for generating output voltages with more than five levels. Beside the already mentioned *k*-1 capacitors on the main DC bus, the FC would need $(k-1)\times(k-2)/2$ storage capacitors for generating *k*-1 level output voltage. Due to availability of more than one switching state for most of the voltage levels, one can choose a suitable switching combination to balance the voltage of capacitors. It must be noted although this approach is viable, but the control algorithm may get complicated. In addition, there will be need for higher switching frequency to balance the capacitor voltages, resulting in higher loss of the converter.



(a) (b)

Fig. 6. (a) Power circuit of a CHB (b) Phase output voltage of a nine-level CHB [5]

CHB converter avoids extra clamping diodes and capacitors and consists of several full-bridge converters with separate DC-sources. A nine-level CHB converter with four separated DC sources is shown in Fig. 6. Each full-bridge has four semiconductor switches (S_1, S_2, S_3, S_4) and can generate output voltage of $+V_{dc}$, 0, and $-V_{dc}$. Voltage level $+V_{dc}$ is generated by turning on S_1 and S_4. Voltage level $-V_{dc}$ is generated by turning on S_2 and S_3. Voltage level 0 is generated by either turning on S_1 and S_3 or turning on S_2 and S_4. The terminals of each full-bridge are connected in series, and the output voltage of CHB is synthesized by sum of output voltage of full-bridge converters. For a CHB with *k* number of separate DC-sources, the number of output voltage

level will be $2k+1$. CHB has less number of components for generating same number of levels than NPC and FC, and its modular structure makes the circuit implementation easier. In addition, CHB's structure suits well for renewable sources such as photovoltaic cells. It must be noted that CHBs also come with disadvantages. They require bulky multi-winding transformers to realize several isolated DC sources.

1.2 Modular Multilevel Converter (MMC) Limitation

Apart from the three well-known classical multilevel topologies, a new type of multi-level converter topology named modular multilevel converter (MMC) was first presented by Marquardt in 2003 [17] as shown in. Fig. 7 and has become increasingly attractive due to its modularity, high efficiency, excellent output voltage waveform, and no need for separate DC sources [18]. However, MMC also shows some drawbacks: circulating current, and high number of bulky capacitors. The circulating current i_{circ} is caused due to the difference of the sum of voltage of upper arm and lower arm with the DC bus. Existence of the circulating current i_{circ} is known as one of the disadvantages of the MMC [18]. The circulating current does not have any effect on the AC-side of the MMC and is better to be suppressed either by selecting a large value inductor or using a circulating current suppression method. Several circulating suppression control exist in the literature for single-phase and three-phase systems [8, 19]. Another issue regarding MMC while generating high number of output voltage levels is the required number of bulky SM capacitors. To improve the harmonic profile of the output voltage, there is the need to increase the number of output voltage levels. However, this would require increasing the number of submodules (SMs) and power semi-conductor devices and their associated gate driver and protection circuitry, resulting in the overall multilevel converter to be complex and expensive [20].

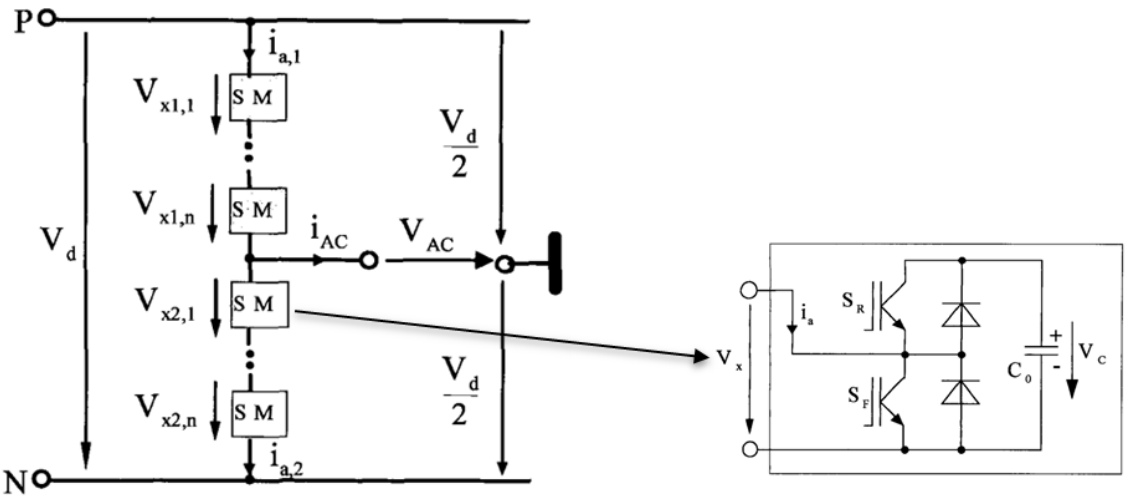


Fig. 7. MMC presented by Marquardt in 2003 [17]

The use of large number of SM capacitors dramatically increases the cost and volume of MMC and can result in higher failure rates. Several studies have been carried out in recent years on reducing the required total capacitance and subsequent cost and volume of MMC [13-19], [21-25]. The MMC size and mass can generally be reduced either by reducing the required capacitance of each SM while having same number of SMs, or by reducing the number of required SMs while having same SM capacitor size. The first approach can be fulfilled by using new control methods to suppress the voltage fluctuations of the SM capacitors. When SM is in the ON state, the SM capacitor is inserted into the circuit and its voltage varies according to the amplitude and direction of the arm current. On the other hand, when the SM is in the OFF state, the SM capacitor is bypassed and its voltage remains unchanged. Hence, the change in the voltage of SM capacitor depends on length and the sequence of the SM in the ON state, and the arm current. The arm current constitutes terms of ac current and circulating current. References in [21-23] added a common-mode voltage to the ac-side voltage and applied appropriate control of the circulating current in the phase-legs of the MMC to compensate the fundamental frequency fluctuations in

arm power. The drawbacks of this method are lower available output voltage due to harmonics and harmful effect on lifetime of the rotor bearing due to the injected common-mode voltage [24]. On the other hand, since the arm current includes ac term and circulating term, the voltage fluctuations and subsequent SM capacitance can be reduced by injecting second-order harmonics into the circulating current [25]. The operation of this method was later analyzed when the MMC is connected to an unbalanced grid [26]. A discontinuous modulation technique based on adding zero-sequence to the original modulation signal was presented in [27]. This resulted in significant reduced capacitor voltage ripple especially when operating under low modulation indices.

The second approach can be realized by proposing new MMC topologies that require less total capacitance for generating the same output voltages. As surveyed in [28], new MMC topologies are derived by mainly proposing new SM configurations and much less efforts have been made on proposing new topologies based on the conventional MMC. An active power decoupling method for MMCs was suggested in [29] that proposes a new SM with a buck-type active power filter which absorbs the low-frequency ripples. The capacitance reduction in this method however comes with the cost of doubling the total number of the MMC switches and adding an energy storage capacitor and a smoothing inductor into each SM of MMC. A three-level SM was introduced in [30] to improve the capacitor voltage balancing at low switching frequencies, but comes with the cost of double semiconductor switches than conventional half bridge SMs. In [31], a hybrid MMC topology is proposed comprising half bride SMs and extra auxiliary full bridge SMs. Compared with the traditional MMC, the auxiliary full bridge SMs are added to each arm to produce intermediate voltage levels resulting in less number of SMs to produce an output voltage with the same number of levels. In [32] a new MMC is proposed that compared to conventional MMC employs a middle SM in each phase. Each phase can be divided

into three parts of upper arm, lower arm, and the middle SM. While conventional MMC would require 2*N* SMs for generating *N*+1 voltage levels, the new MMC with middle SM would require 2*N*-1 SMs. The drawback of this topology is that voltage balancing will be more complicated [32]. This topology was further improved in [33] where the capacitors of the top SMs and bottom SMs are connected by two accessorial cables to reduce second-order capacitor voltage ripples, while the number of employed SMs remained the same. Several other new topologies have been proposed, as examples in [34-37]. Majority of the new proposed topology focus mainly on decreasing components parts, and provide steady state results of the converter with multilevel output voltage feeding an R-L load. Therefore no results on the dynamic performance of the converter or employment of the converter in a more complicated system is given.

Fewer efforts have been devoted to proposing MMC-based multilevel topologies focusing on reduced part count. This work proposes an MMC-based multilevel converter that provides the same output voltage as conventional MMC but has reduced number of bulky capacitors. This is achieved by introduction of an extra middle arm to the conventional MMC. Also due to similar dynamic equations of the proposed converter, several previously developed control methods for voltage balancing and circulating current suppression in the literature for conventional MMCs are applicable to the proposed MMC with minimal effort. In addition, as the loss analysis can be gainful in design stage of the proposed converter, comparative loss analysis of the conventional MMC and the proposed multilevel converter is presented. The derived new topology is explained in chapter II.

1.3 Carrier-disposition PWM techniques for MMC

For controlling the output voltage of MMC, different modulation schemes have been proposed in literature. Modulation schemes based on fundamental frequency, such as nearest level modulation (NLM) and selective harmonic elimination (SHE) are among the proposed methods [38]. Carrier based pulse width modulation (PWM) techniques have been widely employed for MMC, and can be classified into carrier-disposition PWM techniques (or level-shifted PWM), and subharmonic techniques (or phase-shifted PWM) [28]. In carrier-disposition PWM technique, N carriers are placed vertically in a way that the covered band is contiguous and generates the output waveform. N is the number of SMs in the arm. Carrier-disposition PWM techniques are further classified into phase disposition (PD), phase-opposition-disposition (POD), and alternative-phase-opposition-disposition (APOD).

Voltage transitions for triangular carrier of PD carrier-disposition PWM are shown in Fig. 8(a) as an example. V_{ref_u} denotes the reference voltage of the upper arm, and is normalized between 0 and 1. Each carrier is associated with insertion/bypass of a particular SM. Carrier 1 to carrier 4 in Fig. 8(a) are responsible for insertion/bypass of SM number 1 ($SM_{u,1}$) to SM number 4 ($SM_{u,4}$) of the upper arm, respectively.

However, carrier-disposition PWM techniques will result in uneven distribution of voltage ripple along the capacitors of different SMs in each arm, and therefore will affect the output voltage harmonics and also cause large magnitudes of circulating current. Also, the unequal device conduction periods (DCPs) of the carrier disposition techniques affect the charging and discharging of capacitor voltages and cause non-uniform power and heat distribution in each arm of the inverter [39]. To negate these drawbacks and distribute the switching evenly, carrier rotation techniques have been proposed. Two carrier rotation techniques have been discussed in [39]. In

the first method, carrier signals are rotated at the end of each carrier cycle as shown in Fig. 8(b). In the second method, the rotation is performed at the end of each modulation cycle as shown in Fig. 8(c). Also, a modified carrier rotation technique is proposed in [40]. However, even with the mentioned capacitor voltage balancing techniques, the output voltages have a relatively high total harmonic distortion [41]. To overcome the problems of the previously mentioned techniques, a modified PD carrier-disposition PWM with voltage balancing is presented in [42]. In this method, the voltage transition of any carrier and the corresponding gating signal is not assigned to a specific SM and its switches. This method which is proposed for PD carrier-disposition PWM, initially determines the number of output voltage levels and subsequently the number of inserted SMs in one arm. Then by subtracting it from *N*, the required number of inserted SMs in the other arm are obtained. This method could be implemented for POD and APOD carrier-disposition PWM, but requires modification in the algorithm for obtaining the required number of inserted SMs. Part of this work presents a novel modified carrier deposition PWM technique with SM capacitor voltage balancing that can be employed for any of three carrier deposition PWM methods without any modification. The proposed voltage balancing method will result in even distribution of voltage ripple along the capacitors of different SMs in each arm, and also avoid large magnitudes of circulating current. Also, the unequal DCPs of the carrier disposition techniques will be avoided which results in uniform power and heat distribution in each arm of the MMC. The proposed method will be explained in Chapter II.

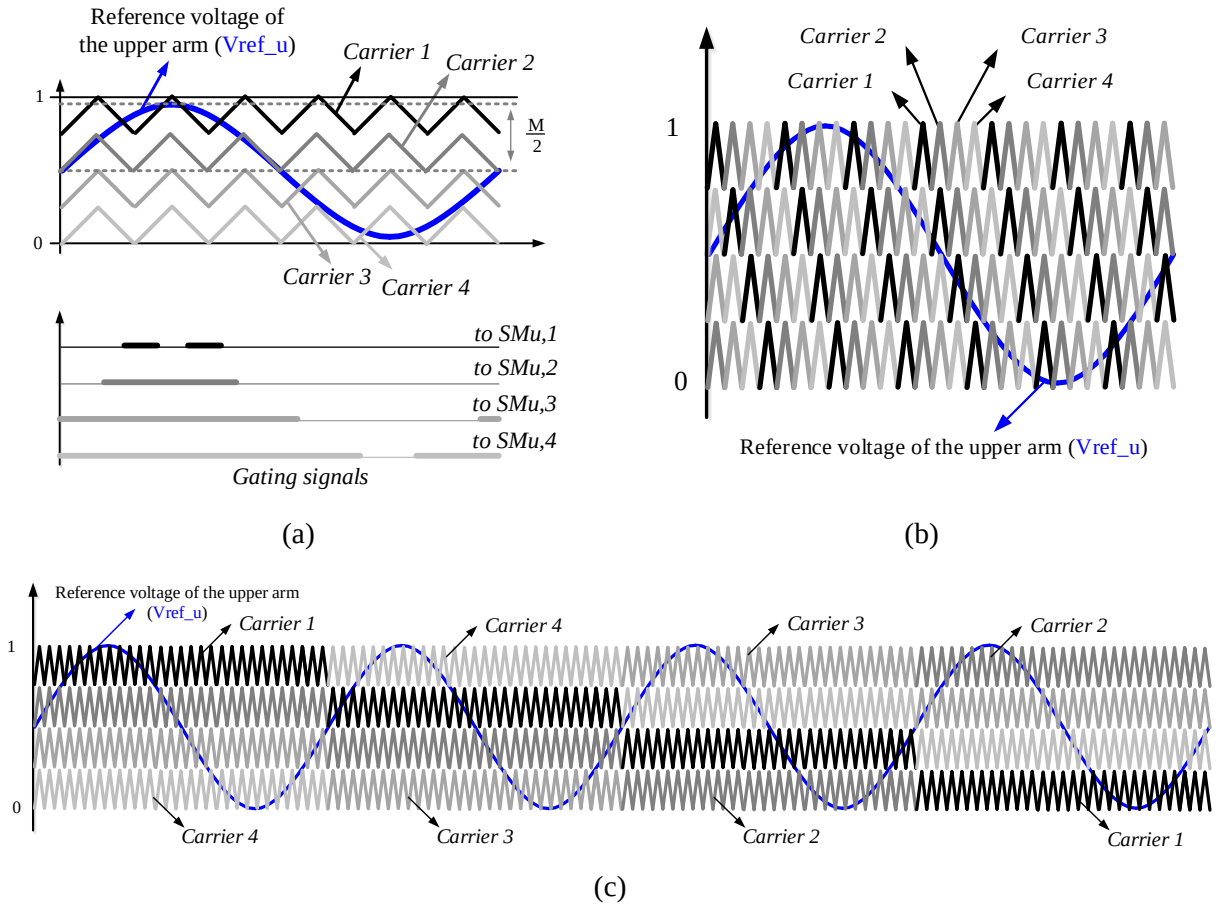


Fig. 8. (a) Triangular carrier of PD carrier-disposition PWM (b) Carrier signal rotation at the end of each carrier cycle (c) Carrier signal rotation at the end of each modulation cycle

1.4 Control of Isolated MMC-based DC-DC converters

Furthermore, Chapter III of this work proposes an improved control of isolated MMC-based DC-DC converters. With the development of power electronics, DC distribution and transmission have been efficiently used in grid-connected renewable energy systems such as off-shore wind parks [43-45], electric shipboards and more electric aircrafts [46], and the DC grids. For wind or wave farms placed far offshore it will be beneficial to use DC grid rather than AC for

energy collection and grid integration [47, 48]. Through use of DC power systems, possible congestion can be avoided as higher power transfer capacity will be achieved [48]. The use of medium-voltage direct-current (MVDC) and high-voltage DC (HVDC) power systems is rapidly growing in modern smart grids due to their higher flexibility and efficiency [49]. Therefore, with the rapid development of DC grids, the need for interconnection of different voltage levels becomes important. Regarding multi-level inverter topologies in the medium-voltage DC and high-voltage DC applications, MMC offers superior features such as high modularity, high scalability, high quality multilevel AC voltage and low switching frequencies at submodule level [47].

The high-voltage isolated DC-DC converter with MMC-transformer-MMC configuration was first introduced by Kenzelman in 2011 [47] for energy collection and distribution. The isolated MMC-based high-power DC-DC converter can serve the voltage matching between two different DC voltage levels, control power flow between them, and act as DC circuit breaker. A transformer that provides galvanic isolation links the two MMCs. It had been shown in [50] that this isolated MMC-based DC-DC (IMMDC) converter is capable of handling AC and DC faults without needing any additional DC or AC circuit breakers. In case of short circuit on either AC or DC side, the gating signals of all SMs are locked and the short circuit current through the DC-DC converter can be efficiently avoided [49]. Also, the transformer can be operated with higher frequency than line frequency, resulting in reduced size of transformer and SM capacitors [47].

In [51], multilevel AC-link voltage waveform scheme (also known as sinusoidal AC-link voltage waveform scheme) and two-level AC-link voltage waveform scheme (also known as square AC-link voltage waveform scheme) have been compared for a case study that steps up the voltage from 5 kV to 30 kV. The multilevel AC-link voltage waveform scheme results in

conventional staircase voltage waveforms, while the two-level AC-link voltage waveform scheme is adopted based on the two-level voltage waveform of double active bridge. For the sinusoidal AC-link voltage waveform scheme, a transformer with turns ratio of 1:6 was used for voltage elevation, while for the case of square AC-link voltage waveform scheme a transformer with unitary turns ratio was used and voltage elevation of 6 was done in the secondary MMC with a 14/10 modulation. It has been shown in [51] that both AC-link voltage waveform scheme can provide efficiencies over 98% over a wide range for AC-link frequency up to 800 Hz. The normalized mass kg/kVA of the transformer for square AC-link voltage waveform scheme is less than sinusoidal AC-link voltage waveform scheme, resulting in higher power density of converter with square AC-link voltage waveform scheme. To lessen the high exerted dv/dt of transformer in square AC-link voltage waveform scheme, a staircase waveform can be created towards the transition periods to the negative voltage level by introducing small phase shift angle between gating signals of SMs in one arm [52], that is known as quasi-square AC-link voltage waveform scheme. A comparative experimental study between the three different AC-link voltage waveform schemes of sinusoidal, square, and quasi-square (also known as trapezoidal) is carried out in [53]. It is concluded in [53] that square wave and quasi-square AC-link voltage waveform schemes provide highest and lowest power capability, respectively. Also, the sinusoidal AC-link voltage waveform scheme is found to be a better option when the design and manufacturing challenges of the medium-frequency transformer (MFT) are considered. In [54] a quasi-square AC-link voltage waveform scheme with phase shift angle between arms has been proposed to improve energy balance between the arms. It must be mentioned square wave modulation is employed in this work.

In single-phase-shift (SPS) control, a phase shift is exerted between the primary and secondary voltage of the transformer to control the transferred power between the two DC

networks. Although power flow control can be done by either the common phase-shift control or by changing the voltage amplitude through modulation index [55], phase-shift control is the most common approach employed in literature in such isolated DC-DC converters due to low inertia, good transient performance, easy to implement, and so on [53]. Usually it is desired to have large modulation ratio index in IMMDC, i.e. equal to one, since the AC voltage of the MMC stage can be as high as DC bus voltage and result in low-magnitude currents [56]. But as in this method the power flow is sole function of the phase-shift angle, high current stress and increased loss is experienced for power devices and magnetic components [57]. Several control methods have been introduced to improve the performance of isolated DC-DC converters. In [58, 59] the single-phase shift control is combined with variable duty cycle ratio which is calculated online and will add to the complexity of the system. In an effort to add more degrees of freedom to the external phase shift between the primary and secondary voltages of the transformer, in [57] an internal phase shift is introduced between the legs of switches in one side of the transformer. Adding the internal phase shift will result in expanding regulation range of transmission power. This will also result in reduced current stress of the switches and thus reduced switching losses. In [60] double phase shift control method is introduced where equal internal phase shift takes place on both sides of the transformer, and in [61] a universal phase shift control has been proposed where internal phase shift could be different from each other. This results in operating points with more reduced current stress while delivering same power.

Despite of the role of amplitude ratio index, there is no study that has investigated the effect of combined amplitude ratio index and phase-shift control on current stress of IMMDC converter. Although claimed in the literature that large modulation index results in low-magnitude currents, this work indeed investigates the amplitude ratio index as an extra degree of freedom for

controlling the converter. Therefore, in this work the primary side of the transformer is considered as the reference; i.e. phase angle is zero and the amplitude ratio index is one. However, for the secondary side, the generated voltage has a phase shift and an amplitude ratio index. Chapter III primarily analyzes the effect of combined amplitude ratio index and phase shift control on current stress of the components.

Chapter II: New MMC-Based Multilevel Converter

2.1. Conventional MMC

Fig. 9 illustrates power circuit of a two-level VSC and conventional MMC. The MMC is comprised of the upper arm and the lower arm, two buffer inductors in each leg, and two DC sources. Each arm includes SMs or cells. The usual employed SM type is half-bridge as shown in Fig. 9. Each half-bridge SM consists of a floating DC capacitor and two high-frequency complementary insulated gate bipolar transistors (IGBT) switches. When a SM is in the ON state by turning on switch S, then the SM is inserted into the circuit and the capacitor voltage will vary regarding arm current. If the arm current $i_{u,l}$ is positive, then the voltage of the floating capacitor will increase, and if it is negative the voltage of the capacitor will decrease. If the switch S is turned off, the SM is in the OFF state and bypassed from the circuit. In this case the voltage of the capacitor will remain unchanged. Capacitor voltage balancing in MMC is the main goal of the control system which assures stable operation of the converter [8]. Using $4N$ (N is equal to 2 in MMC of Fig. 9(b)) SMs per arm, and employing a common modulation method such as phase-disposition level shifted Pulse Width Modulation (PWM), the MMC can generate output voltages with $8N$+1 (equal to 17 in MMC of Fig. 9(b)) levels with maximum peak to peak value of $2E$ (E represents the DC source voltage in Fig. 9(b)).

With respect to Fig. 9(b), the output current can be written as

$$i_{out} = i_u - i_l \tag{1}$$

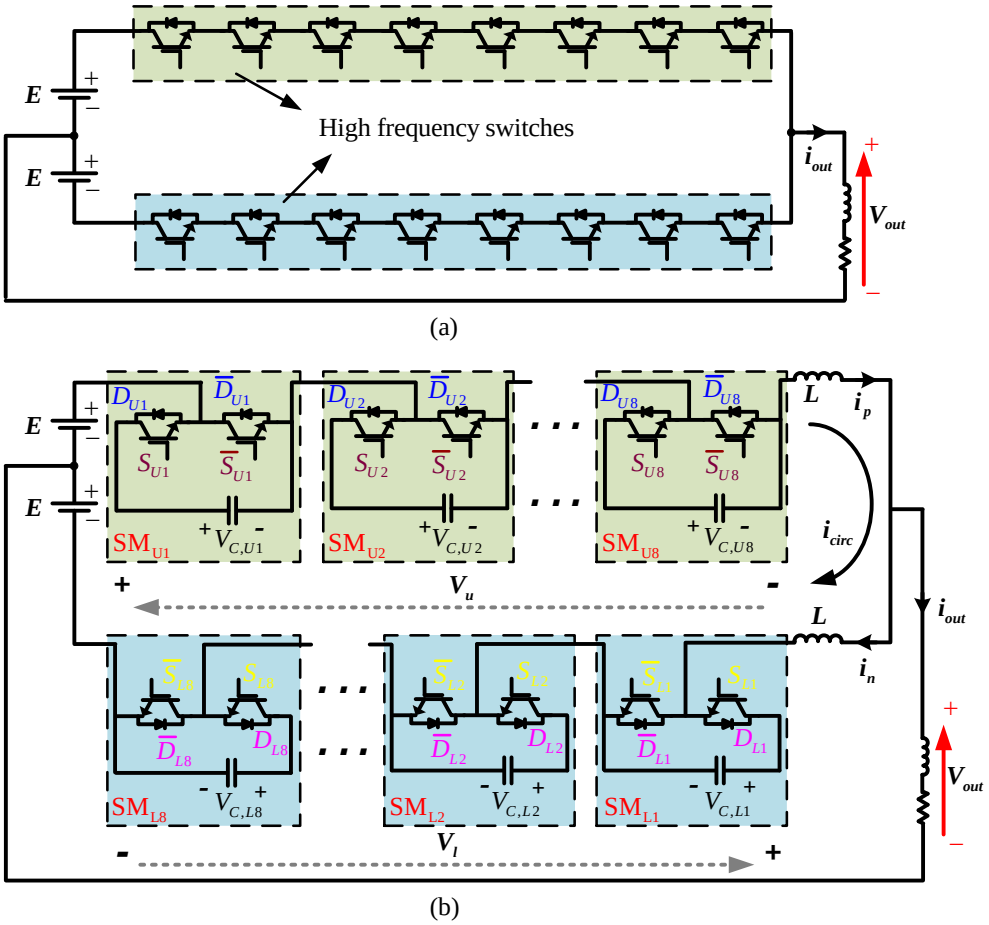


Fig. 9. Power circuit of a) Two-level VSC (b) Conventional MMC, with 8 SMs per arm that results in 17-level V_{out} controlled by phase disposition level-shifted PWM..

where i_u and i_l are the upper arm and lower arm currents; respectively. The upper arm voltage V_u, and the lower arm voltag, V_l, can be written as

$$V_u = E - L_{arm}\frac{di_u}{dt} - V_{out} \tag{2}$$

$$V_l = E - L_{arm}\frac{di_l}{dt} + V_{out} \tag{3}$$

where V_{out} is the output voltage, and L_{arm} is the arm inductor.

By subtracting (3) from (2), we can write

$$V_{out} = \frac{1}{2}\left(V_l - V_u - L_{arm} \frac{di_{out}}{dt} \right) \tag{4}$$

Also by adding (2) and (3) we can write

$$\frac{di_{circ}}{dt} = \frac{1}{2L_{arm}} \left(2E - \left(V_u + V_l \right) \right) \tag{5}$$

where

$$i_{circ} = \frac{i_u + i_l}{2} \tag{6}$$

2.2. Power Circuit Topology of Proposed Two-And-One MMC (TOMMC)

Fig. 9(b) and Fig. 10 illustrate conventional MMC and proposed two-and-one set of arms MMC. The employed SM type is half-bridge. Each half-bridge SM consists of a floating DC capacitor and two high-frequency complementary IGBTs switches. When SM is inserted to the circuit, the SM capacitor voltage varies according to the arm current value and direction. When the SM is bypassed, the SM capacitor voltage remains unchanged. The conventional MMC is comprised of the upper arm and the lower arm, two buffer inductors in each leg, and two DC sources. The one side of the load is connected to the mid-point of the upper and lower arm, and the other side of the load is connected to mid-point of the two DC-sources. As seen in Fig. 9(b) and Fig. 10, V_{out} is the output voltage across the load, i_u and i_l are the upper and lower arm currents, respectively; E is the source voltage of the TOMMC, L is the arm buffer inductor, i_{circ} is the circulating current, $V_{C,Ui}$ and $V_{C,Li}$ represent ith capacitor voltage in the upper and lower arm,

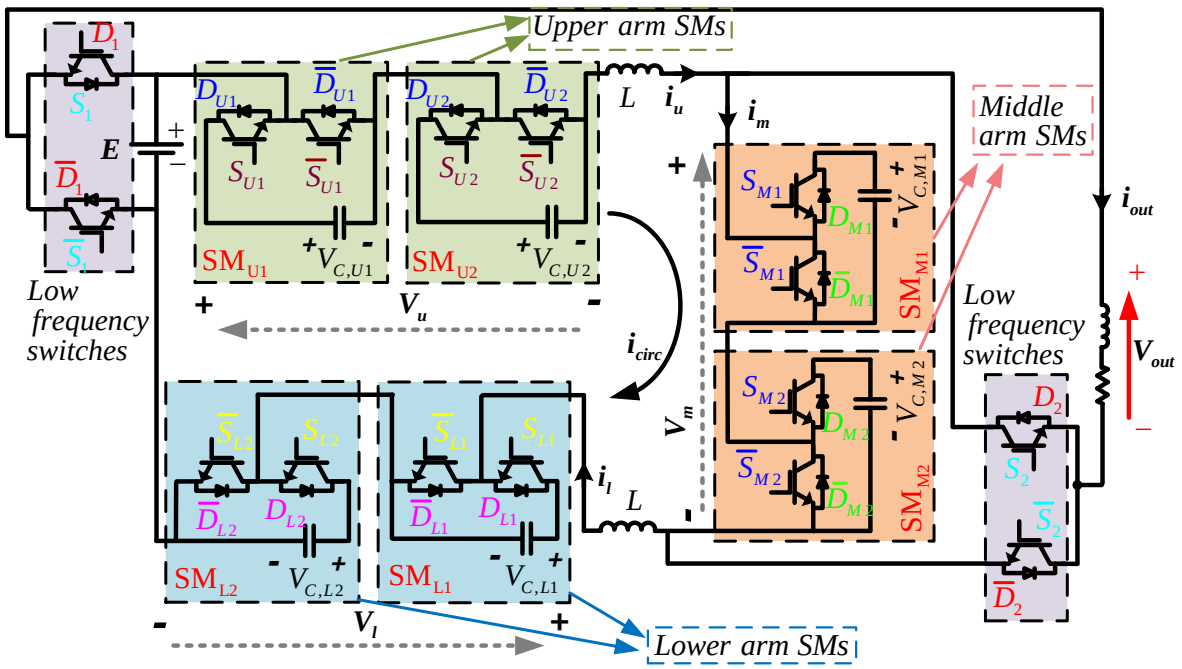


Fig. 10. Proposed TOMMC with two-and-one set of arms, with 2 SMs per arm that results in 17-level V_{out} controlled by phase disposition level-shifted PWM

respectively, and S_{Ui} and S_{Li} are the gating signal of the upper switch in the *i*th SM of the upper and lower arm, respectively.

As mentioned earlier, using *4N* (*N* is equal to 2 in MMC of Fig. 9(b)) SMs per arm, and employing a common modulation method such as phase-disposition level shifted pulse width modulation (PWM), the conventional MMC can generate output voltages with 8*N*+1 (equal to 17 in MMC of Fig. 9(b)) levels with maximum peak to peak value of 2*E* (*E* represents the DC source voltage in Fig. Fig. 9(b)). One major drawback of conventional MMC-based multilevel topologies is the large ratio of number of required SMs to the number of realizable voltage levels. In general, conventional MMC-based topologies require half of the SMs of the leg any time instant to be inserted at into the circuit for generating any voltage level, while the other remaining half is

bypassed. For example, assuming there are 2*W* SMs per leg, if *X* SMs in the lower arm are inserted into the circuit for a specific voltage level, then there is need for *W-X* SMs of the upper arm to be inserted in the circuit to compensate the deficit between the DC link voltage and voltage of the inserted SMs in lower arm. In other words, at any instance during the operation, half of the SM capacitors in a conventional MMC are not engaged in the power conversion process. This work addresses this issue by introducing a new MMC topology that makes better use of the SMs at any time by introducing a middle arm than can be added to the upper/lower arm.

The proposed TOMMC, shown in Fig. 10, utilizes a middle arm with *N* SMs (SM_{M1} to SM_{M2} in Fig. 10), in addition to the conventional MMC's upper and lower arms. This arrangement is denoted as the "two-and-one" set of arms, hereinafter. The proposed TOMMC converter can generate the same *2E* peak to peak output voltage with the same *8N+1* (=17 in Fig. 10) number of voltage levels as a conventional MMC, but with using only *N* SMs in each arm and only one DC source for the converter. All SMs in the proposed topology utilize a half-bridge structure similar to the conventional MMC. The number of SMs in proposed TOMMC then amounts to a total of *3N* (=6 in Fig. 10) in each phase which is significantly less than the *8N* (=16 in Fig. 9(b)) SMs that the conventional MMC uses. This is achieved since four new low-frequency high-power switches (S_1 to $\overline{S_2}$ in Fig. 10) are introduced in proposed TOMMC. Switches $\overline{S_1}$ and $\overline{S_2}$ act complimentary to switches S_1 and S_2. The switch S_1 is required to turn ON and OFF only once at each complete cycle of the fundamental frequency of the output voltage. Due to fundamental switching frequency of switches S_1 and $\overline{S_1}$, it is feasible to employ gate turn-off (GTO) thyristor instead of IGBTs. The switch S_2 is required to turn ON and OFF three times at each complete cycle of the fundamental frequency of the output voltage.

TABLE I
Different switching states and associated ancillary and auxiliary SMs.

	S_1	S_2	Ancillary SMs	V_{anc}	Auxiliary SMs	V_{aux}	V_{out}
state 1	ON	ON	upper arm	V_u	middle and lower arm	V_m+V_l	V_u
state 2	ON	OFF	upper and middle arm	V_u+V_m	lower arm	V_l	V_u+V_m
state 3	OFF	ON	lower arm	V_l	upper and middle arm	V_u+V_m	$-V_l$
state 4	OFF	OFF	middle and lower arm	V_m+V_l	upper arm	V_u	$-V_m-V_l$

2.3. Circuit Equations of TOMMC

Four fundamental states are defined for the TOMMC in TABLE I based on the switching states of the low frequency switches during operation. TABLE I uses the notion of *ancillary* and *auxiliary* for the SMs in each fundamental state. For each fundamental state, we define ancillary SMs as the ones responsible for generating the output voltage, and the *auxiliary SMs* as the ones responsible for compensating the voltage deficit between the dc source and the output voltage. For instance, when S_1 and S_2 are ON (fundamental state 1), the output current will flow through the load and the upper arm. In this state the upper arm provides the output voltage (thus it contains the ancillary SMs), while the middle and lower arm compensate the voltage deficit between the dc source and output voltage (thus they contain the auxiliary SMs).

TABLE I also illustrates the voltage of ancillary and auxiliary SMs (V_{anc} and V_{aux} respectively), and the output voltage (V_{out}), based on the voltages of the upper, middle, and lower arms (V_u, V_m , V_l respectively). TABLE II illustrates the switching states for generating different

voltage levels of 17-level TOMMC when output voltage is positive. It shows the redundant switching states for generating different voltage levels. The redundant switching states will be used in voltage balancing of the capacitors. Similarly, TABLE III illustrates the switching states for generating different voltage levels when output voltage is negative.

TABLE II

Switching states of 17-level TOMMC for different positive voltage levels

S_{U1}	S_{U2}	S_{M1}	S_{M2}	S_{L1}	S_{L2}	S_1	S_2	V_{out}
ON	ON	ON	ON	OFF	OFF	ON	OFF	$+E$
OFF	ON	ON	ON	OFF	OFF	ON	OFF	$+7E/8$
ON	OFF	ON	ON	OFF	OFF	ON	OFF	
ON	ON	OFF	ON	OFF	OFF	ON	OFF	
ON	ON	ON	OFF	OFF	OFF	ON	OFF	
ON	ON	ON	ON	ON	OFF	ON	OFF	
ON	ON	ON	ON	OFF	ON	ON	OFF	
ON	ON	ON	OFF	ON	OFF	ON	OFF	$+6E/8$
ON	ON	ON	OFF	OFF	ON	ON	OFF	
ON	ON	OFF	ON	ON	OFF	ON	OFF	
ON	ON	OFF	ON	OFF	ON	ON	OFF	
ON	OFF	ON	ON	ON	OFF	ON	OFF	
ON	OFF	ON	ON	OFF	ON	ON	OFF	
OFF	ON	ON	ON	ON	OFF	ON	OFF	
OFF	ON	ON	ON	OFF	ON	ON	OFF	
ON	ON	OFF	OFF	ON	OFF	ON	OFF	$+5E/8$
ON	ON	OFF	OFF	OFF	ON	ON	OFF	
ON	OFF	ON	OFF	ON	OFF	ON	OFF	
ON	OFF	ON	OFF	OFF	ON	ON	OFF	
ON	OFF	OFF	ON	ON	OFF	ON	OFF	
ON	OFF	OFF	ON	OFF	ON	ON	OFF	
OFF	ON	ON	OFF	ON	OFF	ON	OFF	
OFF	ON	ON	OFF	OFF	ON	ON	OFF	
OFF	ON	OFF	ON	ON	OFF	ON	OFF	
OFF	ON	OFF	ON	OFF	ON	ON	OFF	
OFF	OFF	ON	ON	ON	OFF	ON	OFF	
OFF	OFF	ON	ON	OFF	ON	ON	OFF	
ON	ON	ON	OFF	ON	ON	ON	OFF	
ON	ON	OFF	ON	ON	ON	ON	OFF	
ON	OFF	ON	ON	ON	ON	ON	OFF	
OFF	ON	ON	ON	ON	ON	ON	OFF	
ON	ON	OFF	OFF	ON	ON	ON	OFF	$+4E/8$
ON	OFF	ON	OFF	ON	ON	ON	OFF	
ON	OFF	OFF	ON	ON	ON	ON	OFF	
OFF	ON	ON	OFF	ON	ON	ON	OFF	
OFF	ON	OFF	ON	ON	ON	ON	OFF	
OFF	OFF	ON	ON	ON	ON	ON	OFF	

ON	ON	ON	ON	OFF	OFF	ON	ON	
ON	ON	ON	OFF	ON	OFF	ON	ON	
ON	ON	ON	OFF	OFF	ON	ON	ON	
ON	ON	OFF	ON	ON	OFF	ON	ON	
ON	ON	OFF	ON	OFF	ON	ON	ON	
ON	ON	OFF	OFF	ON	ON	ON	ON	
ON	ON	ON	ON	ON	OFF	ON	ON	+3*E*/8
ON	ON	ON	ON	OFF	ON	ON	ON	
ON	ON	ON	OFF	ON	ON	ON	ON	
ON	ON	OFF	ON	ON	ON	ON	ON	
ON	OFF	ON	ON	OFF	OFF	ON	ON	
ON	OFF	ON	OFF	ON	OFF	ON	ON	
ON	OFF	ON	OFF	OFF	ON	ON	ON	
ON	OFF	OFF	ON	ON	OFF	ON	ON	
ON	OFF	OFF	ON	OFF	ON	ON	ON	
ON	OFF	OFF	OFF	ON	ON	ON	ON	
OFF	ON	ON	ON	OFF	OFF	ON	ON	
OFF	ON	ON	OFF	ON	OFF	ON	ON	
OFF	ON	ON	OFF	OFF	ON	ON	ON	
OFF	ON	OFF	ON	ON	OFF	ON	ON	
OFF	ON	OFF	ON	OFF	ON	ON	ON	
OFF	ON	OFF	OFF	ON	ON	ON	ON	
ON	OFF	ON	ON	ON	OFF	ON	ON	+2*E*/8
ON	OFF	ON	ON	OFF	ON	ON	ON	
ON	OFF	ON	OFF	ON	ON	ON	ON	
ON	OFF	OFF	ON	ON	ON	ON	ON	
OFF	ON	ON	ON	ON	OFF	ON	ON	
OFF	ON	ON	ON	OFF	ON	ON	ON	
OFF	ON	ON	OFF	ON	ON	ON	ON	
OFF	ON	OFF	ON	ON	ON	ON	ON	
ON	OFF	ON	ON	ON	ON	ON	ON	+1*E*/8
OFF	ON	ON	ON	ON	ON	ON	ON	
OFF	OFF	ON	ON	ON	OFF	ON	ON	
OFF	OFF	ON	ON	OFF	ON	ON	ON	
OFF	OFF	ON	OFF	ON	ON	ON	ON	
OFF	OFF	OFF	ON	ON	ON	ON	ON	
OFF	OFF	ON	ON	ON	ON	ON	ON	0

TABLE III

Switching states of 17-level TOMMC for different negative voltage levels

S_{U1}	S_{U2}	S_{M1}	S_{M2}	S_{L1}	S_{L2}	S_1	S_2	V_{out}
OFF	OFF	ON	ON	ON	ON	OFF	ON	-1*E*
OFF	OFF	OFF	ON	ON	ON	OFF	ON	-7*E*/8
OFF	OFF	ON	OFF	ON	ON	OFF	ON	
OFF	OFF	ON	ON	OFF	ON	OFF	ON	
OFF	OFF	ON	ON	ON	OFF	OFF	ON	
ON	OFF	ON	ON	ON	ON	OFF	ON	
OFF	ON	ON	ON	ON	ON	OFF	ON	
ON	OFF	ON	ON	ON	OFF	OFF	ON	-6*E*/8
ON	OFF	ON	ON	OFF	ON	OFF	ON	
ON	OFF	ON	OFF	ON	ON	OFF	ON	
ON	OFF	OFF	ON	ON	ON	OFF	ON	
OFF	ON	ON	ON	ON	OFF	OFF	ON	
OFF	ON	ON	ON	OFF	ON	OFF	ON	
OFF	ON	ON	OFF	ON	ON	OFF	ON	
OFF	ON	OFF	ON	ON	ON	OFF	ON	
ON	OFF	ON	ON	OFF	OFF	OFF	ON	-5*E*/8
ON	OFF	ON	OFF	ON	OFF	OFF	ON	
ON	OFF	ON	OFF	OFF	ON	OFF	ON	
ON	OFF	OFF	ON	ON	OFF	OFF	ON	
ON	OFF	OFF	ON	OFF	ON	OFF	ON	
ON	OFF	OFF	OFF	ON	ON	OFF	ON	
OFF	ON	ON	ON	OFF	OFF	OFF	ON	
OFF	ON	ON	OFF	ON	OFF	OFF	ON	
OFF	ON	ON	OFF	OFF	ON	OFF	ON	
OFF	ON	OFF	ON	ON	OFF	OFF	ON	
OFF	ON	OFF	ON	OFF	ON	OFF	ON	
OFF	ON	OFF	OFF	ON	ON	OFF	ON	
ON	ON	ON	ON	ON	OFF	OFF	ON	
ON	ON	ON	ON	OFF	ON	OFF	ON	
ON	ON	ON	OFF	ON	ON	OFF	ON	
ON	ON	OFF	ON	ON	ON	OFF	ON	
ON	ON	ON	ON	OFF	OFF	OFF	ON	-4*E*/8
ON	ON	ON	OFF	ON	OFF	OFF	ON	
ON	ON	ON	OFF	OFF	ON	OFF	ON	
ON	ON	OFF	ON	ON	OFF	OFF	ON	
ON	ON	OFF	ON	OFF	ON	OFF	ON	
ON	ON	OFF	OFF	ON	ON	OFF	ON	

ON	ON	OFF	OFF	ON	ON	OFF	OFF	
ON	OFF	ON	OFF	ON	ON	OFF	OFF	
ON	OFF	OFF	ON	ON	ON	OFF	OFF	
OFF	ON	ON	OFF	ON	ON	OFF	OFF	
OFF	ON	OFF	ON	ON	ON	OFF	OFF	
OFF	OFF	ON	ON	ON	ON	OFF	OFF	
ON	ON	OFF	OFF	ON	OFF	OFF	OFF	
ON	OFF	ON	OFF	ON	OFF	OFF	OFF	
ON	OFF	OFF	ON	ON	OFF	OFF	OFF	
OFF	ON	ON	OFF	ON	OFF	OFF	OFF	
OFF	ON	OFF	ON	ON	OFF	OFF	OFF	
OFF	OFF	ON	ON	ON	OFF	OFF	OFF	
ON	ON	OFF	OFF	OFF	ON	OFF	OFF	
ON	OFF	ON	OFF	OFF	ON	OFF	OFF	-3*E*/8
ON	OFF	OFF	ON	OFF	ON	OFF	OFF	
OFF	ON	ON	OFF	OFF	ON	OFF	OFF	
OFF	ON	OFF	ON	OFF	ON	OFF	OFF	
OFF	OFF	ON	ON	OFF	ON	OFF	OFF	
ON	ON	ON	OFF	ON	ON	OFF	OFF	
ON	ON	OFF	ON	ON	ON	OFF	OFF	
ON	OFF	ON	ON	ON	ON	OFF	OFF	
OFF	ON	ON	ON	ON	ON	OFF	OFF	
ON	ON	ON	OFF	ON	OFF	OFF	OFF	
ON	ON	OFF	ON	ON	OFF	OFF	OFF	
ON	OFF	ON	ON	ON	OFF	OFF	OFF	
OFF	ON	ON	ON	ON	OFF	OFF	OFF	-2*E*/8
ON	ON	ON	OFF	OFF	ON	OFF	OFF	
ON	ON	OFF	ON	OFF	ON	OFF	OFF	
ON	OFF	ON	ON	OFF	ON	OFF	OFF	
OFF	ON	ON	ON	OFF	ON	OFF	OFF	
ON	ON	ON	OFF	OFF	OFF	OFF	OFF	
ON	ON	OFF	ON	OFF	OFF	OFF	OFF	
ON	OFF	ON	ON	OFF	OFF	OFF	OFF	
OFF	ON	ON	ON	OFF	OFF	OFF	OFF	-1*E*/8
ON	ON	ON	ON	ON	OFF	OFF	OFF	
ON	ON	ON	ON	OFF	ON	OFF	OFF	
ON	ON	ON	ON	OFF	OFF	OFF	OFF	0

The output voltage reference is defined as,

$$V_{out}^{*} = M\ \sin\left(\omega t + \alpha\right) \tag{7}$$

where M is the modulation index ($0 \le M \le 1$) and α is the output voltage phase angle. When generating positive output voltage reference $V_{out}^{*} \ge 0$, switch S_1 is turned ON and switch $\overline{S_1}$ is turned OFF. When generating negative output voltage reference $V_{out}^{*} < 0$, switch S_1 is turned OFF and switch $\overline{S_1}$ is turned ON. It must be noted for the conventional MMC in Fig. 9(b), maximum available value of output voltage is half of DC-link,(equal to $(2E)/2=E$ in Fig. 9(b)), whereas in the proposed TOMMC full utilization of DC-link (equal to E in Fig. 10) can be achieved by using switches S_1 and $\overline{S_1}$.

When switches S_1 and S_2 are turned ON, the output current will flow through the load and the upper arm. In this state, the upper arm provides the output voltage, while the middle and lower arm compensate the voltage deficit between the DC source and output voltage. As mentioned earlier, we define ancillary SMs as the SMs of the arms that are responsible for generating the output voltage, and the auxiliary SMs as the SMs of the arms that are responsible for compensating the voltage deficit between the DC source and output voltage. Regarding this definition, the ancillary and auxiliary SMs' voltage reference of the proposed TOMMC is defined as [62]

$$\begin{cases} V_{anc}^{*} = V_{out}^{*} & -\alpha < wt \le \pi - \alpha \\ V_{aux}^{*} = 1 - V_{out}^{*} & -\alpha < wt \le \pi - \alpha \\ V_{anc}^{*} = -V_{out}^{*} & \pi - \alpha < wt \le 2\pi - \alpha \\ V_{aux}^{*} = 1 + V_{out}^{*} & \pi - \alpha < wt \le 2\pi - \alpha \end{cases} \tag{8}$$

The middle arm is included in the ancillary SMs circuit either when the positive output voltage reference is less than half or when the negative output voltage reference is less than minus

half. In this state, switch S_2 is turned OFF and switch $\overline{S_2}$ is turned ON. Either when the positive output voltage reference is greater than half or when the negative output voltage reference is greater than minus half, switch S_2 is turned ON and switch $\overline{S_2}$ is turned OFF. The four different states of operation of the proposed converter, already mentioned in TABLE I is provided in Fig. 11 for better understanding.

State 1 in Fig. 11 is defined for $0 < V_{out}^{*} < 0.5$. In this state switches S_1 and S_2 are turned ON. The ancillary SMs will include SMs of the upper arm, while the auxiliary SMs will include the SMs of the middle arm and the lower arm. Accordingly, the voltage of ancillary and auxiliary SMs can be formulated as $V_{anc} = V_u$, and $V_{aux} = V_m + V_l$ respectively, where V_u, V_m, V_l are the voltages of the upper, middle, and lower arms correspondingly, as shown in Fig. 10. State 2 is defined for $0.5 < V_{out}^{*} < 1$. In this state switches S_1 is turned ON while switch S_2 is turned OFF. The ancillary SMs will include SMs of the upper arm and middle arm, and the auxiliary SMs will be the SMs of the lower arm. The voltage of ancillary and auxiliary SMs in this state can be formulated as $V_{anc} = V_u + V_m$, and $V_{aux} = V_l$ respectively. State 3 is defined for $-0.5 < V_{out}^{*} < 0$. In this state switches S_1 and S_2 are turned OFF. The ancillary SMs will include SMs of lower arm, while the auxiliary SMs will include the SMs of the upper arm and the middle arm. The voltage of ancillary and auxiliary SMs in this state can be formulated as $V_{anc} = V_l$, and $V_{aux} = V_m + V_l$ respectively. State 4 is defined for $-1 < V_{out}^{*} < -0.5$. In this state switch S_1 is turned OFF and switch S_2 is turned ON. The ancillary SMs will include SMs of the middle arm and the lower arm, while the auxiliary SMs will include the

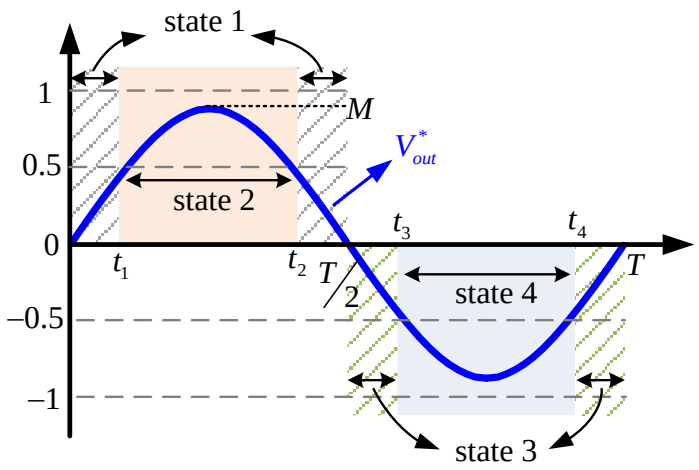


Fig. 11. 4 different operation states of the proposed converter

SMs of the upper arm. The voltage of ancillary and auxiliary SMs in this state can be formulated as $V_{anc} = V_m + V_l$, and $V_{aux} = V_u$ respectively.

The positive output voltage, i.e. when switch S_1 is turned ON, can be written as

$$V_{anc} = V_{out} - L\, di_u / dt \tag{9}$$

$$V_{aux} = E - V_{out} - L\, di_l / dt \tag{10}$$

Subtracting (9) from (10) yields,

$$V_{out} = \frac{1}{2}\left(E + V_{anc} - V_{aux}\right) - \frac{L}{2}\frac{di_{out}}{dt} \tag{11}$$

where

$$i_{out} = i_l - i_u \tag{12}$$

It can be seen from (11) that output voltage has extra term of $E/2$ compared to the case in conventional MMC. This results in full utilization of the link voltage when generating positive

output voltage. Summing (9) and (10) yields,

$$\frac{di_{circ}}{dt} = \frac{1}{2L}\left[E - \left(V_{anc} + V_{aux}\right)\right] \tag{13}$$

where

$$i_{circ} = \frac{i_l + i_u}{2} \tag{14}$$

The positive output voltage, i.e. when switch S_1 is turned ON, can be written as

$$V_{anc} = -V_{out} - L\, di_l / dt \tag{15}$$

$$V_{aux} = E + V_{out} - L\, di_u / dt \tag{16}$$

Subtracting (15) from (16) yields,

$$V_{out} = -\frac{1}{2}\left(E + V_{anc} - V_{aux}\right) - \frac{L}{2}\frac{di_{out}}{dt} \tag{17}$$

It can be seen from (17) that output voltage has extra term of $-E/2$ compared to the case in conventional MMC that results in full utilization of the link voltage when generating negative output voltage. Summing (15) and (16) yields the same equation as in (13). Hence, the dynamic equation for circulating current in proposed TOMMC is the same as of conventional MMC. Therefore, several previously developed control methods for voltage balancing and circulating current suppression in the literature for conventional MMCs are applicable to the proposed TOMMC with minimal effort. This is another advantage of the proposed topology. To control the voltage of SM capacitors, averaging control is employed for this converter. The details and implementation of this control scheme is similar to the scheme provided in [8]. The i_{circ} terms that represent the circulating current are comprised of DC-component and even order harmonics of the

arm currents. The second order harmonic is the main harmonic component and is suppressed using proportional-resonant type minor loop circulating suppression method in [63].

2.4. Modulation of proposed TOMMC

For the conventional MMC with half-bridge SMs, the upper and lower arm voltage references is defined as [64]

$$\begin{cases} V_l^* = \frac{1}{2}\left(E + V_{out}^*\right) \\ V_u^* = \frac{1}{2}\left(E - V_{out}^*\right) \end{cases} \tag{18}$$

where V_{out}^* is defined in (7). Although the SMs of each arm could provide maximum voltage of DC-link voltage, but the maximum achievable output voltage is half of DC-link voltage. In the proposed TOMMC, the voltage references are considered for ancillary and auxiliary SMs rather than lower and upper arm SMs as defined in (8). The ancillary and auxiliary SMs' voltage reference of the proposed TOMMC is accordingly shown in Fig. 12 where phase-disposition level-shifted PWM is used to synthesis the output voltage. The $3N$ carrier signals are provided for $N = 2$ SMs per arm. It must be noted that the carrier 1 and carrier 2 signals are broken apart and shown separately for better understanding of the proposed TOMMC operation. The gating signals for low-frequency switches as well as gating signals for upper, lower and middle arm SMs are also shown in Fig. 12. As mentioned earlier, switch S_1 is required to turn ON and OFF only once at each complete cycle of the fundamental frequency of the output voltage. The switch S_2 is required to turn ON and OFF three times at each complete cycle of the fundamental frequency of the output voltage. It can be seen that V_{anc} and V_{aux} have $2N+1$ (=5 in Fig. 12) voltage levels varying from 0

to E with steps of $E/4$. Considering (13), the voltage drop on the arm inductor is shown as in Fig. 12, with maximum value of $E/4N$ and minimum value of $-E/4N$. Due to asymmetry of phase disposition level-shifted PWM at synthesizing the V_{anc} and V_{aux} signals, the summation of voltage of ancillary SMs voltage and auxiliary SMs voltage will be always equal to DC-link voltage. Hence, a voltage drop of $\pm E/4N$ will appear on the arm inductors. Since the output voltage depends also on the voltage drop on the arm inductor according to (9)-(10) and (15)-(16), there will be intermediate voltage levels created by phase disposition level shifted PWM, resulting in lower harmonic distortion of the output voltage. It can be seen in Fig. 12 that output voltage of TOMMC with two SMs per arm has $8N+1$ (=17 in Fig. 12) voltage levels.

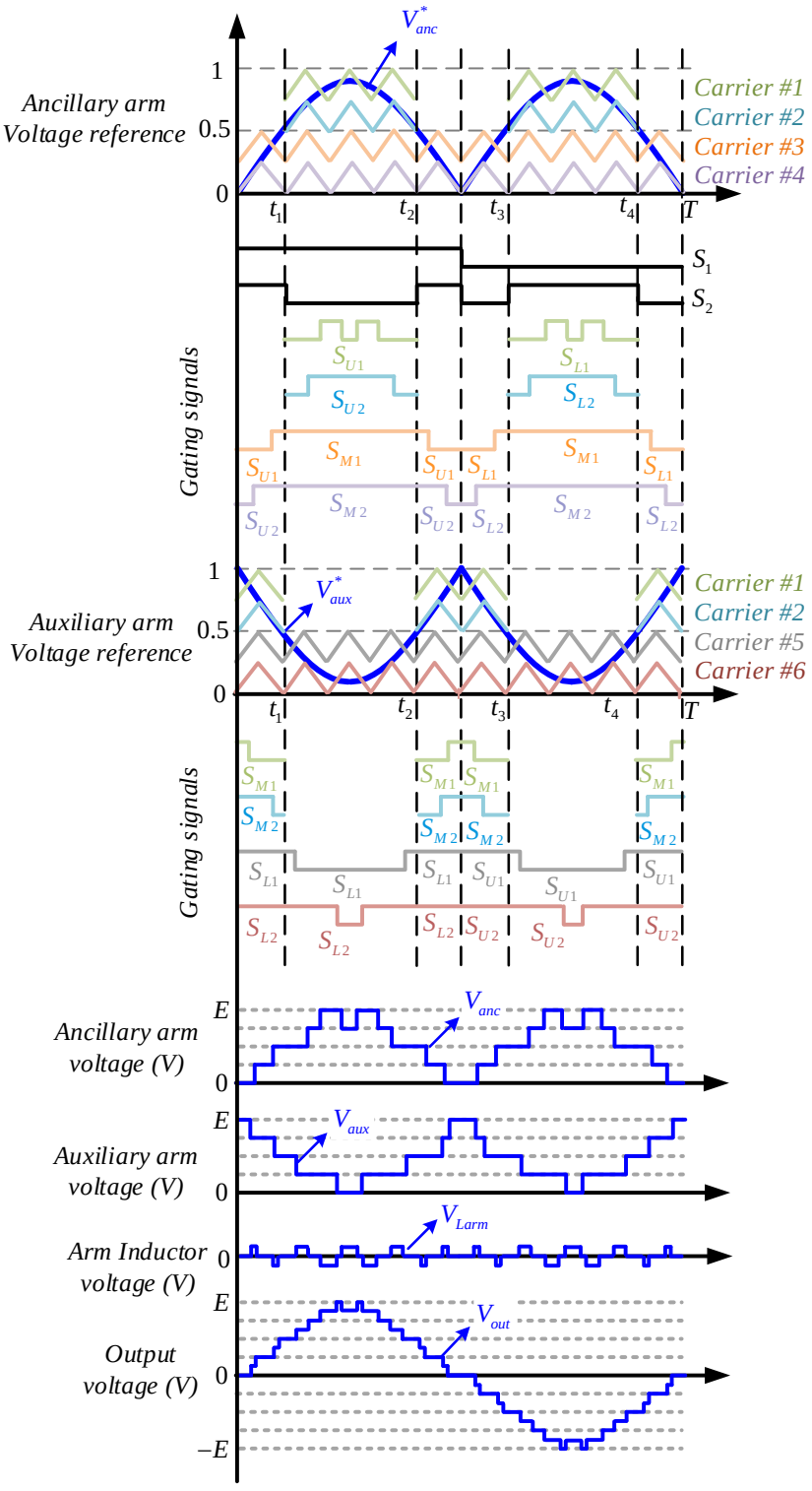


Fig. 12. PDLSPWM scheme for gating signals of the proposed TOMMC

2.5. New Voltage Balancing Technique Based on Carrier-Disposition PWM for MMC

As mentioned in Chapter I Section 1.3, the proposed method does not need the number of inserted SMs and can be employed for any of three carrier deposition PWM without any modification. The proposed voltage balancing method will result in even distribution of voltage ripple along the capacitors of different SMs in each arm. Also, the unequal DCPs of the carrier disposition techniques will be avoided which results in uniform power and heat distribution in each arm of the MMC. In the proposed method, for each carrier which is assigned to a particular SM, one control signal will be obtained and compared with the carrier. The proposed method is explained as follows for lower arm of MMC. Same discussion is true for the upper arm.

The capacitor voltages and current of each arm of MMC are measured to sort the capacitor voltages. The vector of the output of the voltage balancing algorithm is defined as,

$$Y = \left\{0,\ \frac{1}{N},\ \frac{2}{N},\ ...,\ \frac{N-1}{N}\right\} \tag{19}$$

where N is the number of SMs per arm. The corresponding output of the voltage balancing algorithm for each SM ($y_{l,i}$) will take one of the values in vector Y. The $y_{l,i}$ is determined with respect to arm current and capacitor voltages. If the arm current is positive, the SM with the highest capacitor voltage will be assigned a value of $(N-1)/N$, the SM with the second highest capacitor voltage will be assigned a value of $(N-2)/N$, continuing accordingly until reaching the SM with the lowest capacitor voltage which will be assigned a value of 0. If the arm current is negative, the SM with highest capacitor voltage will be assigned a value of 0, the SM with second highest capacitor voltage will be assigned a value of $1/N$, and it will continue until the SM with lowest

capacitor voltage will be assigned a value of $(N-1)/N$. For example, if the arm current is negative and assuming the lower arm capacitor voltages for SMs are [400, 380, 410, and 390] respectively (4 cells per arm N=4), then the output of the voltage balancing algorithm will be Y = {1/4, 3/4, 0, 2/4}. Meaning that the SM with lowest capacitor voltage (SM2) is assigned the highest value of 3/4, and the SM with highest capacitor voltage (SM3) is assigned the lowest value of 0. For positive arm currents and for the same mentioned capacitor voltages, the output of the voltage balancing algorithm will be Y = {2/4, 0, 3/4, 1/4}. The reference voltage of the lower arm which could be a sinusoidal waveform is normalized between 0 and 1 and is denoted by $V_{ref\_l} = \frac{1}{2}\left(1 + M\sin wt\right) + \frac{V_{avg}}{V_{DC}}$. M is the modulation index, V_{avg} is the averaging control term defined in [8], and V_{DC} is the total DC-link voltage. Since each output of the voltage balancing algorithm ($y_{l,i}$) is unique, therefore N different control signals will be obtained by subtracting the V_{ref_l} from each $y_{l,i}$ as shown in Fig. 13,

$$V_{ref\_l,i} = V_{ref\_l} - y_{l,i} \tag{20}$$

The N different control signals cannot have negative values, and cannot be larger than $1/N$ as they will be compared with carriers with maximum value of $1/N$. $V_{ref\_l,i}$ is the reference of i^{th} SM in the lower arm. Then each SM reference is compared with the carrier as shown in Fig. 13. All level-shifted carriers have a maximum value of $1/N$. Similar process can be employed for the upper arm, where $V_{ref\_u} = \frac{1}{2}\left(1 - M\sin wt\right) + \frac{V_{avg}}{V_{DC}}$ is the reference voltage of the upper arm.

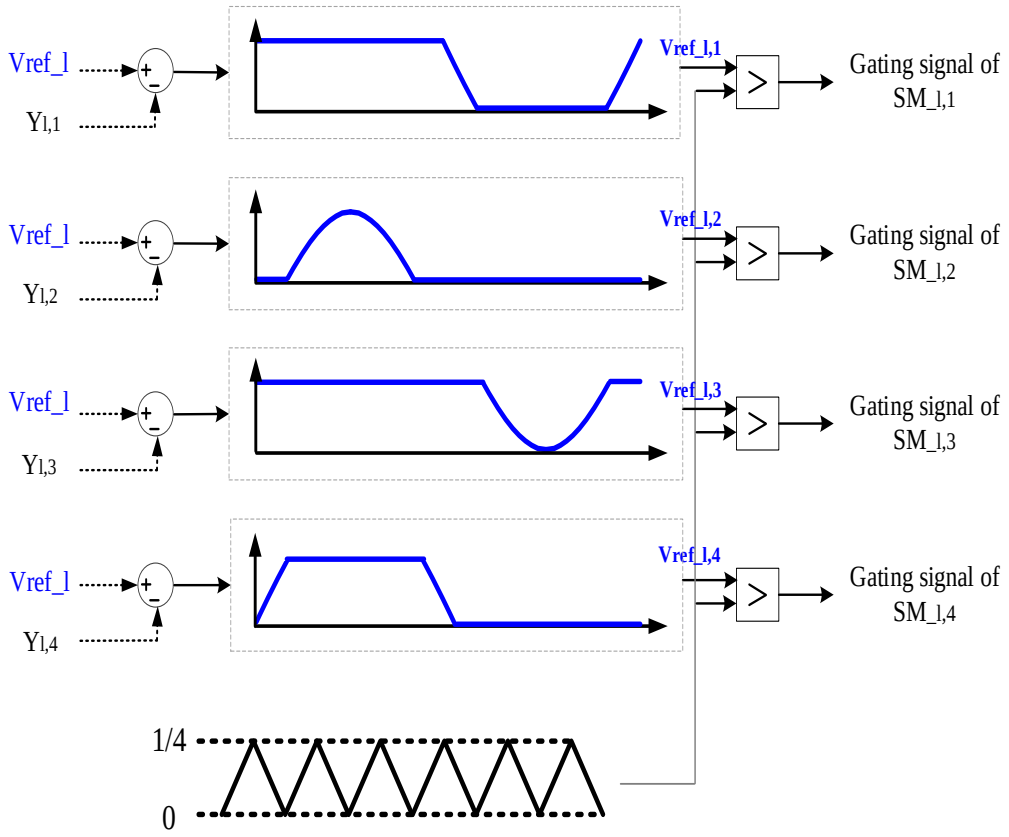
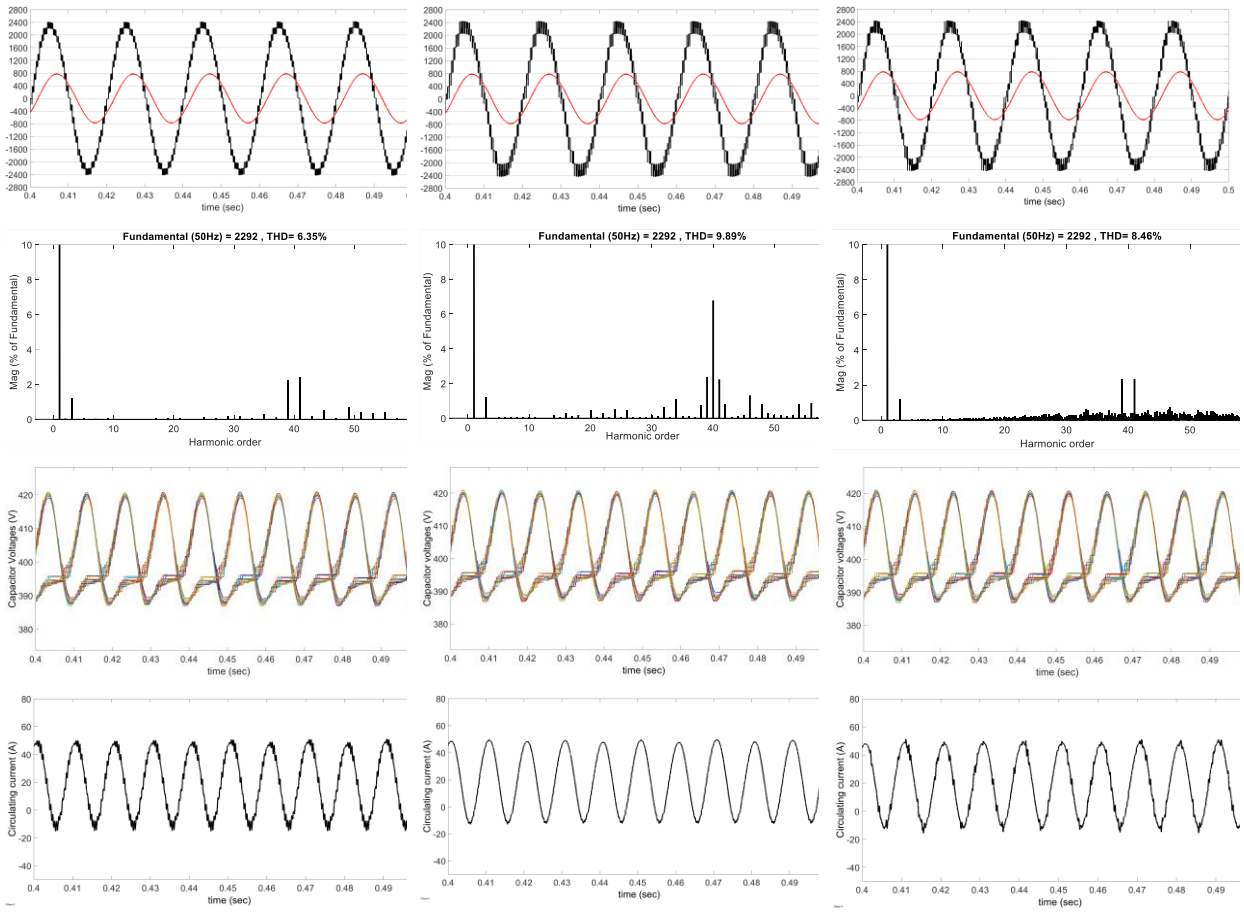


Fig. 13. Employing proposed method for PD carrier-disposition PWM with N=4

The proposed modified voltage balancing method with PD, POD, and APOD carrier disposition PWM method has been implemented on a MMC with 12 SMs per arm (N=12). The THD of output ac voltage is compared between three modulation schemes.

Circulating current suppression is not employed in order to investigate the effect of the modulation schemes on the magnitude of circulating current. Simulations of the single-phase MMC feeding an R-L load is carried out in MATLAB/Simulink. Switching frequency of 2 kHz is employed, and the total DC-link voltage is equal to 4.8 kV. For M=0.95, the peak to peak output voltage of 4.8 kV is obtained as shown in Fig. 14 (top row). As pictured, for N=12 the PD PWM can generate output voltages with $2N$+1 levels and subsequently has lowest THD (6.35%), while



(a) PD (b) POD (c) APOD

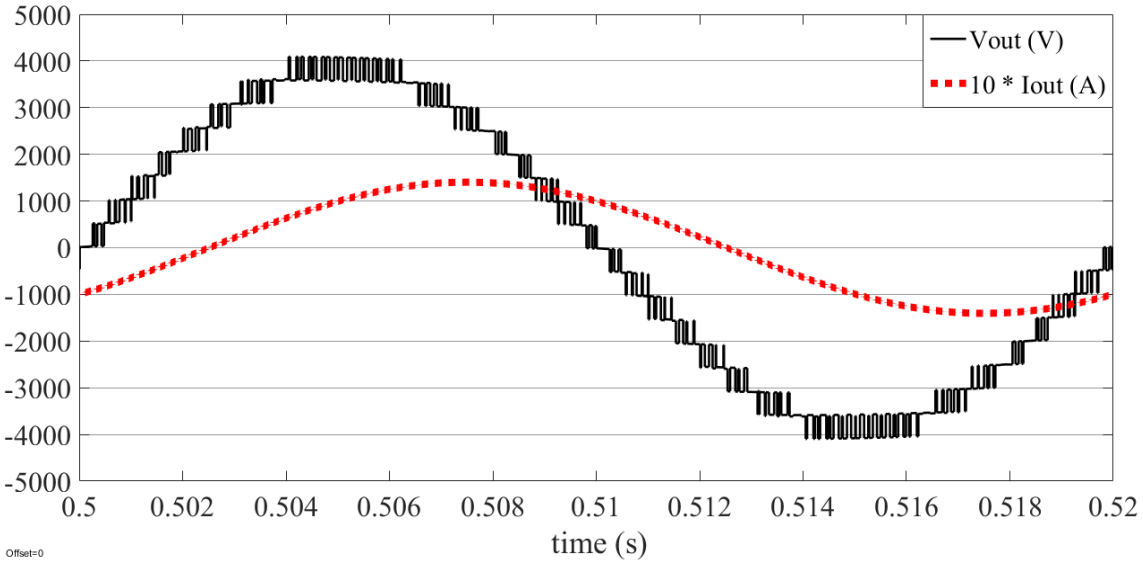
Fig. 14. Output voltage (Vac) and output current (8*Iac); Output voltage THD; Capacitor Voltages; and circulating current for (a) PD carrier-disposition PWM (b) POD carrier-disposition PWM (c) APOD carrier-disposition PWM

POD can generate N+1 levels and has the highest THD (9.89%) among the three, and APOD has an average performance with THD of 8.46%. All capacitor voltages follow the reference value of 400 V (V_{DC}/N). By comparing the circulating currents in Fig. 14, it can be seen that POD has better performance. It has mainly 2nd order harmonics in circulating current, and hence adding a single proportional-resonant (PR) controller tuned at 2nd order harmonic will suppress the circulating current. However, in addition to 2nd order harmonic, PD PWM will generate other higher order harmonics and hence there would be need to use other PRs, which would add to complexity of the controller.

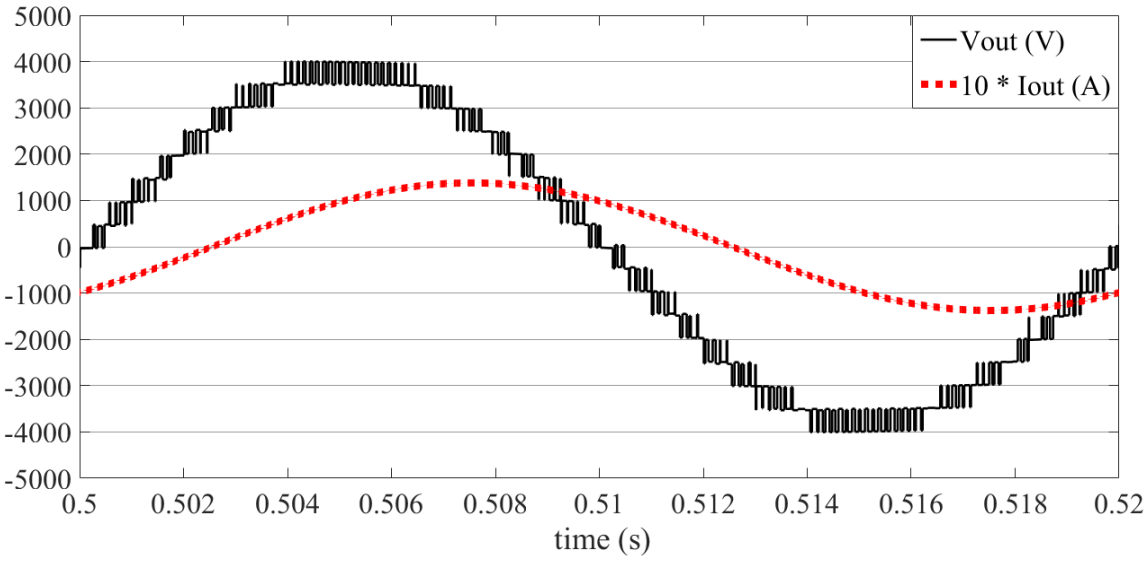
2.6. Simulation Result of 17-Level Output Voltage of Proposed TOMMC

To control the voltage of SM capacitors, the proposed averaging control in Section 2.5 is employed for this converter.

The simulation result of the conventional MMC with two DC-sources of 4 kV and 8 SMs per arm (total of 16 SMs) feeding an R-L load of 20 Ω-60 mH is shown in Fig. 15(a), while simulation result of the two-and-one MMC with one DC-source of 4 kV and 2 SMs per arm (total of 6 SMs) feeding the same load is shown in Fig. 15(b). The modulation index is set at $M = 0.95$, SM capacitor is 3 mF, and arm inductor is 2.5 mH in both cases. It can be seen that both converters can provide output voltage from -4 kV to 4 kV with 17 voltage levels, while proposed converter has less SM capacitors. The simulation results confirm the developed theoretical outcomes.



(a)



(b)

Fig. 15. 17-level output voltage V_{out} of (a) conventional MMC (b) proposed TOMMC

2.7. Current Stress Analysis of High-Frequency Switches

The current stress of high frequency switches of the conventional MMC and proposed TOMMC are compared in this section. By ignoring the even order harmonics, the circulating current can be approximated by its DC-term. The current stress for the high-frequency switches of conventional and proposed TOMMC can be written as

$$i_{\max}^{Conv} = \max\left(i_{circ,dc}^{Conv} + \frac{i_{out}}{2} \right) \tag{21}$$

$$i_{\max}^{Prop} = \max\left(i_{circ,dc}^{Prop} + \frac{i_{out}}{2} \right) \tag{22}$$

Assuming the output current i_{out} is purely sinusoidal [18], it can be written as,

$$i_{out} = i_{out} \cos\left(\omega t + \alpha + \phi\right) \tag{23}$$

where i_{out} is peak value of the output current, and is the angular displacement with respect to the voltage reference in (7). i_{out} can be approximated as,

$$i_{out} = \frac{ME}{Z_{load}} \tag{24}$$

where Z_{load} is the load amplitude. It should be noted to be fair, comparison is done for generating same output voltage V_{out} and feeding same R-L load. That will result in the same output current i_{out} . Hence, the current stress comparison will depend on DC-term of the circulating currents. The circulating DC-term in conventional MMC is obtained as [18]

$$i_{circ,dc}^{Conv} = \frac{M i_{out} \cos\phi}{4} \tag{25}$$

The DC-term of the circulating current of the proposed converter can be obtained by equating the input power and active power consumed by the load. The input power from the DC-source can be written as

$$\begin{aligned} P_{dc} &= \frac{1}{T}\left(\int_0^{0.5T} E i_l dt + \int_{0.5T}^{T} E i_u dt\right) \\ &= \frac{E}{T}\left(\int_0^{0.5T}\left(i_{circ,dc}^{Prop} + \frac{i_{out}}{2}\right)dt + \int_{0.5T}^{T}\left(i_{circ,dc}^{Prop} - \frac{i_{out}}{2}\right)dt\right) \end{aligned} \tag{26}$$

Without losing generality, the output voltage phase angle α is set to zero for simpler calculations. By substituting (23) into (26), input power from the DC-source is obtained as,

$$P_{dc} = E\left(i_{circ,dc}^{Prop} + i_{out}\frac{\cos\phi}{\pi}\right) \tag{27}$$

On the other hand the active power consumed by the output load cab be written as

$$P_{out} = \frac{1}{T}\int_0^T \left(V_{out} i_{out} dt\right) \tag{28}$$

which by substituting (7) and (23) into (28) will be simplified to,

$$P_{out} = \frac{ME i_{out}}{4}\cos\phi \tag{29}$$

By neglecting the loss of the power switches, equating (27) and (29) will result in,

$$i_{circ,dc}^{Prop} = \frac{\left(M\pi - 2\right) i_{out}\cos\phi}{2\pi} \tag{30}$$

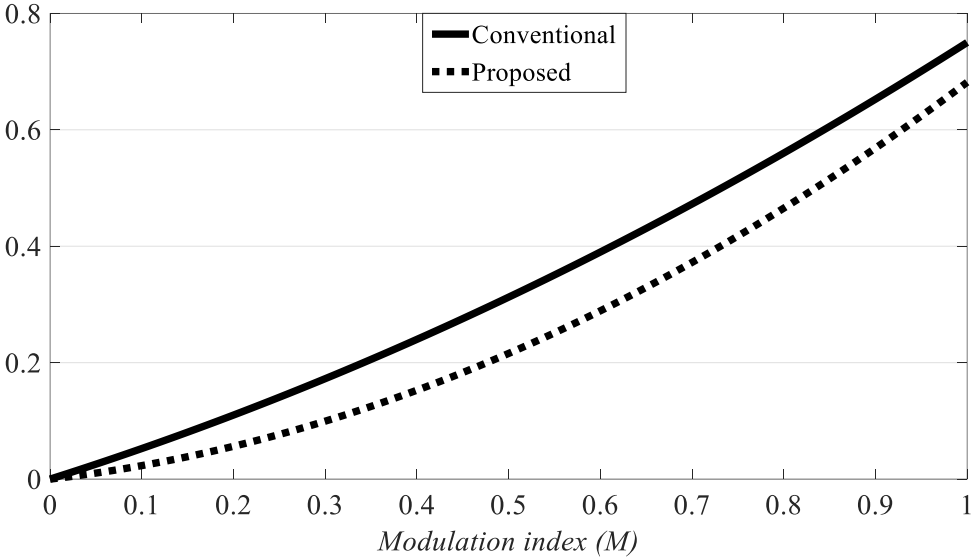


Fig. 16. Current stress comparison of $i_{\max}^{Conv}$ and $i_{\max}^{Prop}$ for $E = 1$ p.u. and $Z_{load} = 1$

For the case studied in Fig. 15 with E=4 kV, $M = 0.95$, and R-L load of 20 Ω-60 mH, $i_{circ,dc}^{Conv}$ and $i_{circ,dc}^{Prop}$ are obtained as 24.9 A and 16.8 A in simulation. Using (25) and (30), $i_{circ,dc}^{Conv}$ and $i_{circ,dc}^{Prop}$ are obtained as 24.19 A and 16.0 A.

Plugging (25) and (30) in (21) and (22), current stresses can be obtained as,

$$i_{\max}^{Conv} = \frac{ME}{Z_{load}}\left(\frac{1}{2} + \frac{M\cos\phi}{4}\right) \tag{31}$$

$$i_{\max}^{Prop} = \frac{ME}{Z_{load}}\left(\frac{1}{2} + \frac{(M\pi - 2)\cos\phi}{2\pi}\right) \tag{32}$$

For $i_{\max}^{Prop}$ to be less than $i_{\max}^{Conv}$, following equation should hold true,

$$\frac{(M\pi - 2)}{2\pi} < \frac{M}{4} \tag{33}$$

which always holds true for $0 \le M \le 1$. Hence, under same output voltage and same load, the current stress of the high frequency switches of the proposed TOMMC is less than conventional MMC. Fig. 16 show the $i_{\max}^{Prop}$ and $i_{\max}^{Conv}$ with respect to M or $E = 1$ p.u. and $Z_{load} = 1$. Higher current stress for high frequency power switches will shorten the lifetime of high-frequency switches.

2.8. Loss Analysis of Proposed TOMMC

The loss investigation is indispensable for performance evaluation of the proposed TOMMC, and for comprehensive comparison with the conventional MMC. The conduction power loss of an IGBT can be derived as

$$P_{IGBT}^{Cond} = \frac{1}{2\pi}\int_0^{2\pi} \left(v_{CE}.i_C\right) d\left(wt\right) \tag{34}$$

where v_{CE} is the IGBT voltage drop across collector-emitter when conducting, and i_C is the current flowing through IGBT. The same expression can be obtained for anti-parallel diode conduction losses as

$$P_{Diode}^{Cond} = \frac{1}{2\pi}\int_0^{2\pi} \left(v_F.i_F\right) d\left(wt\right) \tag{35}$$

where v_F is the forward voltage drop of the anti-parallel diode, and i_F is the forward current. The curves for voltage drop and current are given in datasheet.

Switching loss in IGBT or diode is generated due to inherent switching delays which exists in semiconductor devices. Turn-on energy loss E_{on} and turn-off energy loss E_{off} are considered for IGBT, and energy recovery loss E_{rec} is considered for diode as turn-on loss of diode is usually less than 1% of the recovery loss [65] and is not usually even provided in datasheet of the module. The current-dependent curves of energy loss of IGBTs and diodes for a fixed blocking voltage are

given in datasheet. As the blocking voltage of switches V_{CE} in proposed TOMMC is different from the reference blocking voltage $V_{CE,ref}$ provided in data sheet, the obtained loss energy must be multiplied by the adjustment coefficient defined as [65]

$$k\left(V_{CE}\right)=\frac{V_{CE}}{V_{CE-ref}} \tag{36}$$

The total conduction losses and switching losses in a 2.4 MVA, 8.5 kV twenty-five-level conventional and proposed TOMMC are investigated through simulation results. The study is carried out for conventional and proposed TOMMC feeding an R-L load with power factor of 0.7 (20 Ω-68 mH). The maximum achievable peak-to-peak output voltage is considered to be 24 kV, and voltage reference of each SM capacitor is set as 2 kV. The conventional MMC requires two 12 kV DC-source and 12 SMs per arm. Since the medium-voltage switches are usually operated at around 50% to 60% of the blocking voltage rating, 3.3 kV 400 IGBT module from Infineon Technologies are considered for high-frequency power switches of SMs. This would count to 48 of these 3.3 kV modules to be used in conventional MMC. The proposed TOMMC requires only one 12 kV DC-source and 3 SMs per arm. 18 number of the same IGBT module of conventional MMC are considered for high-frequency power switches of SMs in proposed TOMMC. Since the voltage rating of the low-frequency switches of proposed TOMMC are higher than the voltage rating of SM power switches , three of 6.5 kV 400 A IGBT module from Infineon Technologies are used to realize power switches $S_1 / \overline{S_1}$, while two of those 6.5 kV IGBT modules are used to realize switches $S_2 / \overline{S_2}$. The conventional and proposed TOMMC have same arm inductance of 2.5 mH and SM capacitance of 3 mF. For *M*=0.95, the switching loss, conduction loss and total loss of the conventional MMC is 27.5 kW, 7.0 kW, and 34.5 kW; respectively, while it is equal to

15.5 kW,

Table IV
Loss comparison of conventional and proposed TOMMC for PF 0.9

R-L load	27 Ω - 41.6 mH					
M	0.95		0.8		0.65	
Loss (kW)	P_{sw}	P_{cond}	P_{sw}	P_{cond}	P_{sw}	P_{cond}
Conv.	27.1	7.6	27.8	5.6	26.5	3.9
Prop.	15.7	6.0	15.6	4.6	12.5	3.4

Table V
Loss comparison of conventional and proposed TOMMC for PF 0.7

R-L load	20 Ω - 68 mH					
M	0.95		0.8		0.65	
Loss (kW)	P_{sw}	P_{cond}	P_{sw}	P_{cond}	P_{sw}	P_{cond}
Conv.	27.5	7.0	28.6	5.2	29.7	3.7
Prop.	15.5	5.8	14.8	4.5	13.6	3.3

Table VI
Loss comparison of conventional and proposed TOMMC for PF 0.5

R-L load	15 Ω - 82.6 mH					
M	0.95		0.8		0.65	
Loss (kW)	P_{sw}	P_{cond}	P_{sw}	P_{cond}	P_{sw}	P_{cond}
Conv.	30.0	6.5	30.3	5.0	30.2	3.6
Prop.	15.7	5.8	15.4	4.4	13.3	3.2

5.8 kW, and 21.4 kW for the proposed TOMMC. In this case, the total loss power of the proposed TOMMC is around 62% of the conventional MMC. Table IV to Table VI show the switching loss and conduction loss comparison of the two converters under different power factors (*PF*) and

modulation indexes (*M*). The load impedance magnitude is kept constant to avoid overcurrent of power switches. It can be seen that in both cases the switching loss is the major component of total loss of the converter. While the conduction loss is reduced by around 10% to 20% in the proposed TOMMC compared to conventional MMC, the switching loss has been reduced by around 40% to 50%. It can be seen from Table IV to Table VI that proposed TOMMC has lower total loss under different studied *PF* and *M*.

Fig. 17 to Fig. 19 show the detailed conduction loss of each single power cell in a 2.4 MVA, 8.5 kV twenty-five level considering constant load impedance magnitude with PFs of 0.9, 0.7 and 0.5. Since the loss in each of SMs of upper arm and lower arm are the same, only conduction loss of power switches in SM_{U1} ($P_{S_{U1}}^{Cond}$, $P_{D_{U1}}^{Cond}$, $P_{\overline{S_{U1}}}^{Cond}$, $P_{\overline{D_{U1}}}^{Cond}$) is shown in Fig. 17 to Fig. 19. In addition, all the SM of middle arm have the same power loss. Hence, only the conduction loss for SM_{M1} ($P_{S_{M1}}^{Cond}$, $P_{D_{M1}}^{Cond}$, $P_{\overline{S_{M1}}}^{Cond}$, $P_{\overline{D_{M1}}}^{Cond}$) is provided. Due to symmetrical operation, $P_{S_1}^{Cond} = P_{\overline{S_1}}^{Cond}$, $P_{D_1}^{Cond} = P_{\overline{D_1}}^{Cond}$, $P_{S_2}^{Cond} = P_{\overline{S_2}}^{Cond}$, and $P_{D_2}^{Cond} = P_{\overline{D_2}}^{Cond}$. It can be seen in Fig. 17 to Fig. 19 that as PF decreases from 0.9 to 0.5, the conduction loss of IGBTs S_1 decreases while conduction loss of its anti-parallel diodes D_1 increases. This can be explained by considering the gating signal of IGBT S_1 in Fig. 12, where it is ON for positive V_{out}^* during $0 \le t \le T/2$. If the load would be pure resistive, then the output current was also positive during this time interval and pass through the IGBT. Therefore, diode D_1 would not conduct during time interval $0 \le t \le T/2$. By introducing a more inductive load and with decreasing the PF, the phase shift between output voltage and current increases, and would result in longer portion of time that current passes through diode D_1 .

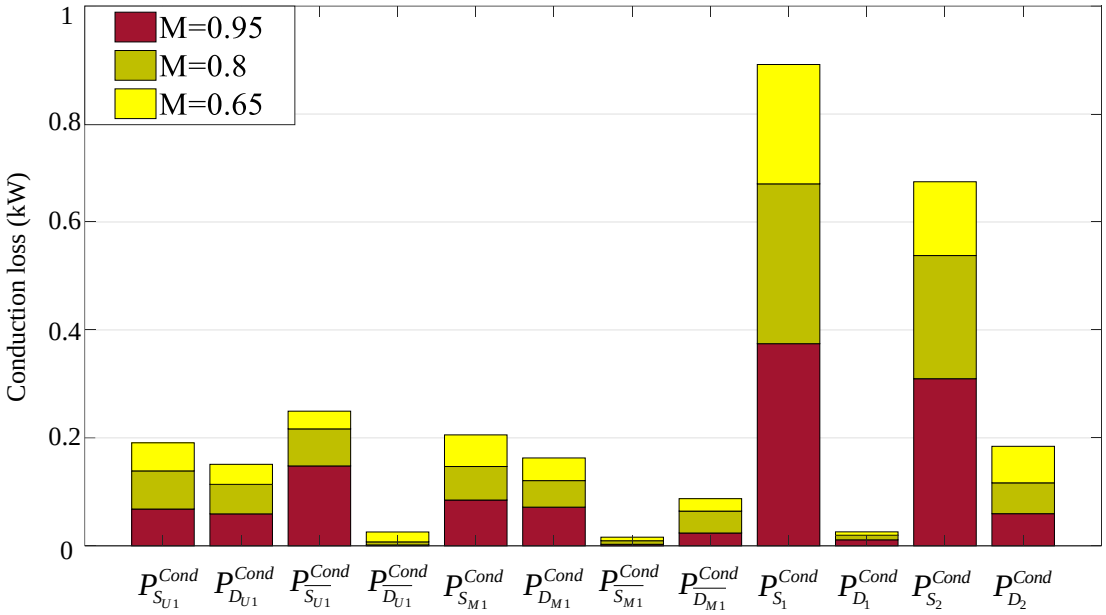


Fig. 17. Conduction loss of each single power cell in a 2.4 MVA, 8.5 kV twenty-five level considering constant load impedance magnitude with PF of 0.9

Fig. 20 to Fig. 22 shows the detailed switching loss of each single power cell in a 2.4 MVA, 8.5 kV twenty-five level considering constant load impedance magnitude with PFs of 0.9, 0.7 and 0.5. It can be seen that the switching losses of IGBT/anti-parallel diode of S_1 / D_1 are very low due to their fundamental switching frequency. In addition, switching loss of IGBT/anti-parallel diode of S_2 / D_2 are relatively low compared to the switching losses of power switches in the arm SMs.

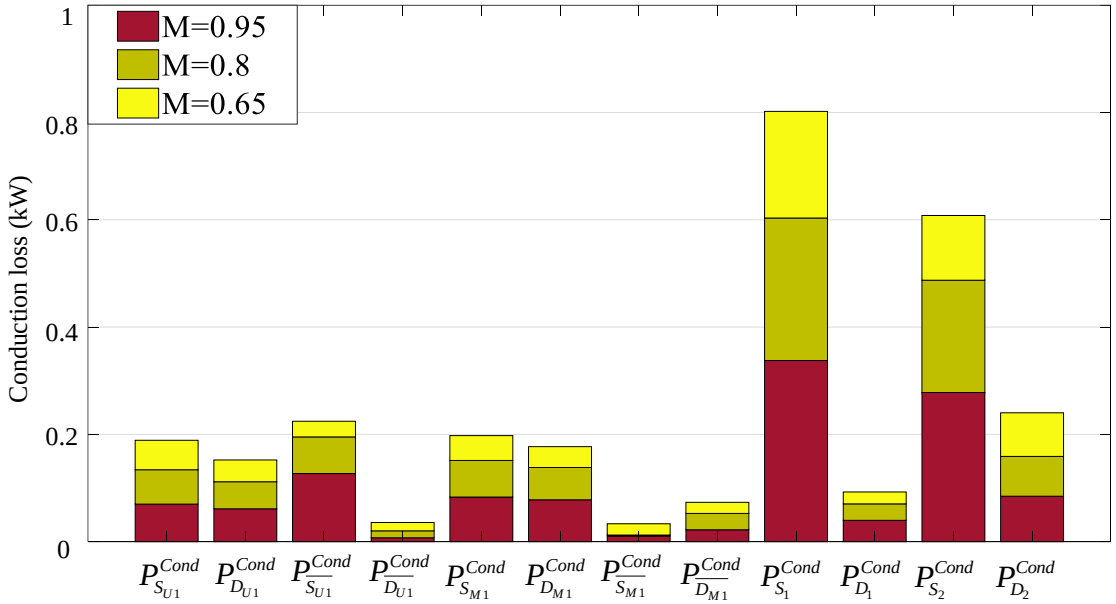


Fig. 18. Conduction loss of each single power cell in a 2.4 MVA, 8.5 kV twenty-five level considering constant load impedance magnitude with PF of 0.7

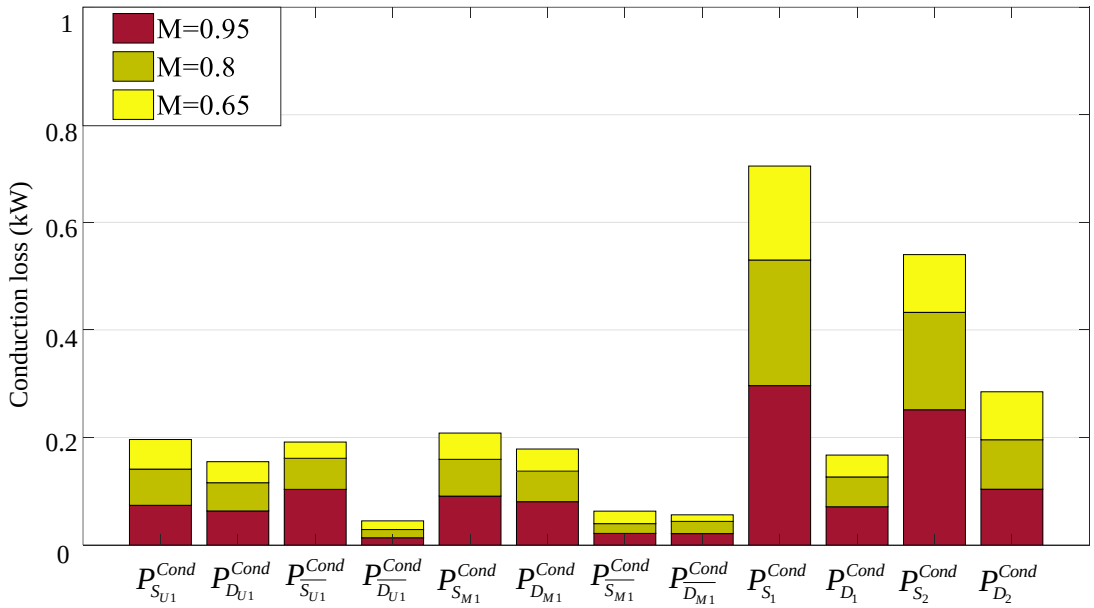


Fig. 19. Conduction loss of each single power cell in a 2.4 MVA, 8.5 kV twenty-five level considering constant load impedance magnitude with PF of 0.5

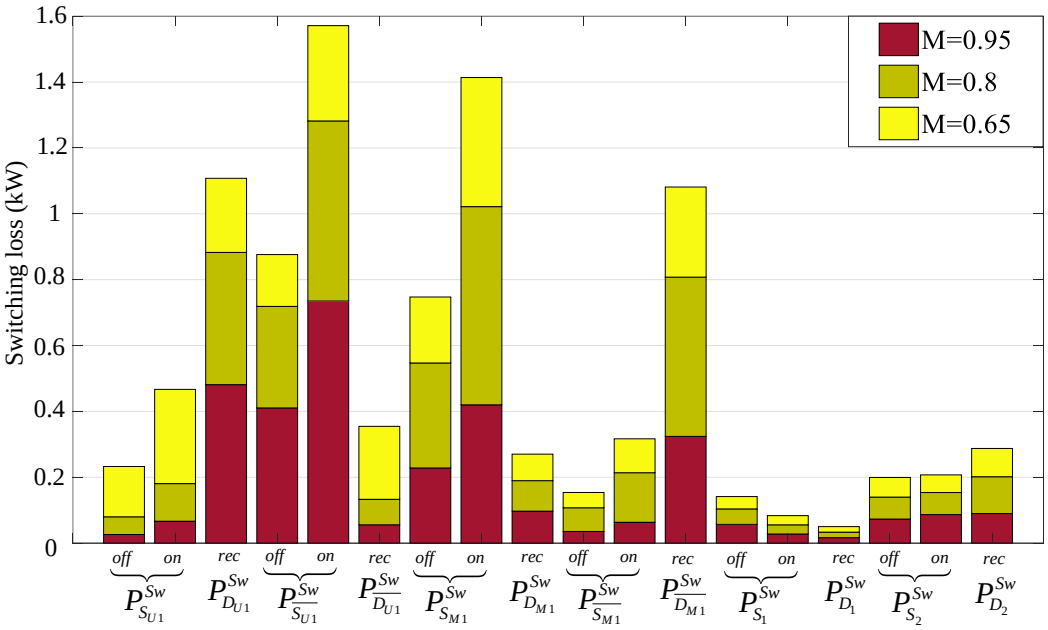


Fig. 20. Switching loss of each single power cell in a 2.4 MVA, 8.5 kV twenty-five level considering constant load impedance magnitude with PF of 0.9

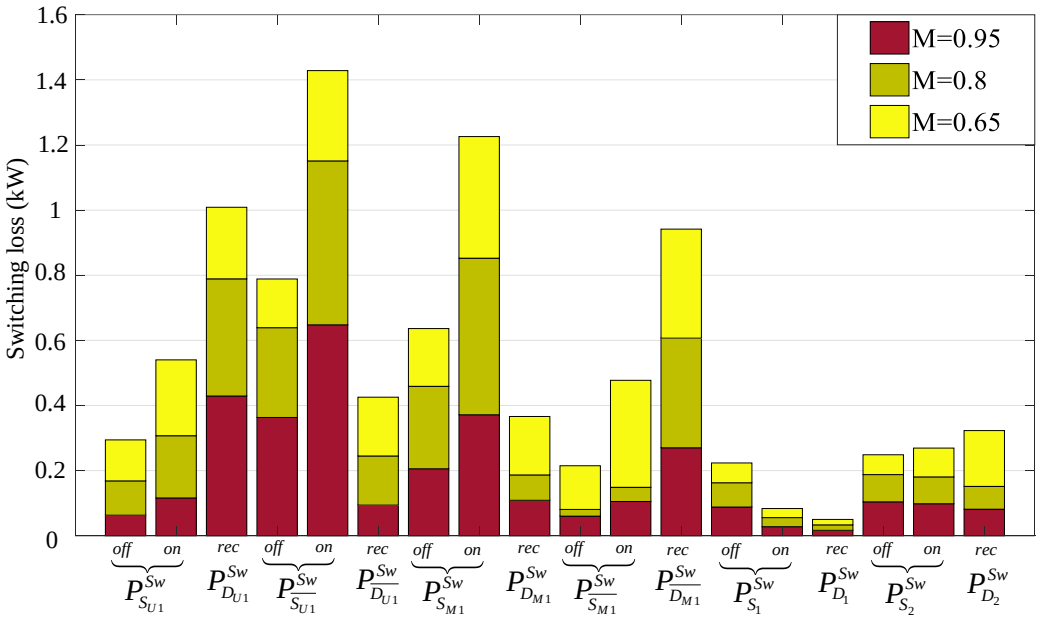


Fig. 21. Switching loss of each single power cell in a 2.4 MVA, 8.5 kV twenty-five level considering constant load impedance magnitude with PF of 0.7

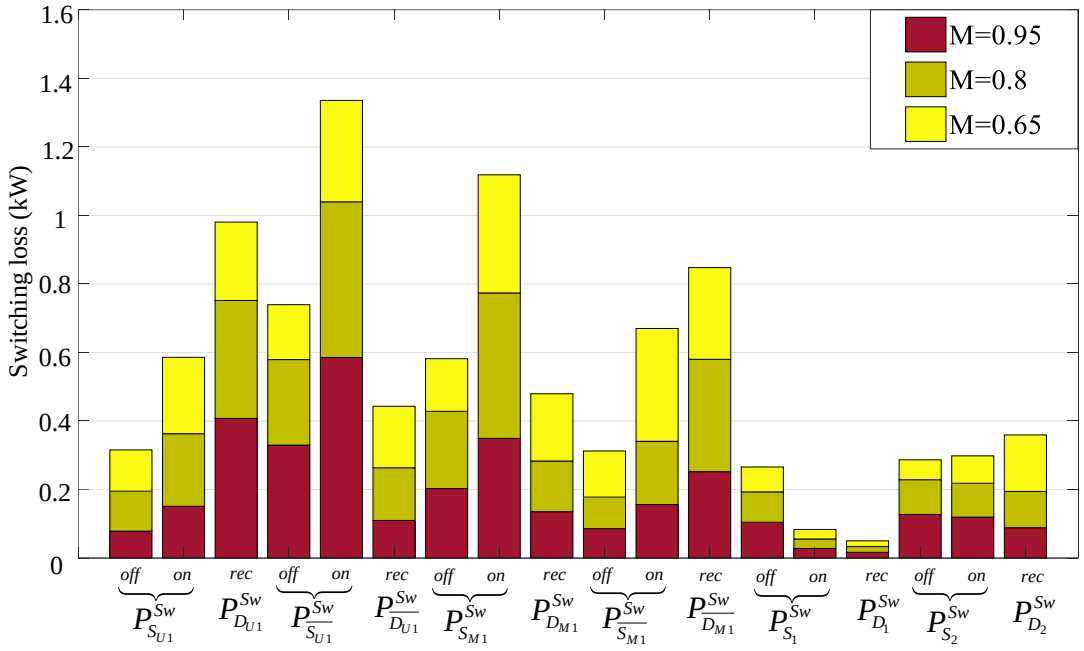


Fig. 22. Switching loss of each single power cell in a 2.4 MVA, 8.5 kV twenty-five level considering constant load impedance magnitude with PF of 0.5

2.9. Hardware-in-the-loop Experimental Results

The operation of the proposed TOMMC based on TI TMS320F28377S is investigated to verify the effectiveness of the modulation and control method mentioned earlier. To do so, study of the proposed TOMMC feeding an R-L load is carried out in hardware-in-the-loop (HIL) system. Proposed level-shifted PWM with switching frequency of 4 kHz is employed. The detailed output voltage of the proposed TOMMC is shown in Fig. 23. As pictured, the proposed TOMMC uses a single 12 kV DC source to generate output voltages with maximum and minimum amplitude of +12 kV and -12 kV with voltage steps dictated by the value of voltages of SM capacitors. In our case, the reference for voltage of SM capacitors is set to 2000 V $\left({}^{V_{DC}}/_{2N}\right)$. To generate the same voltages, the conventional MMC requires 24 cells per phase and two DC sources, while the proposed TOMMC uses only 9 cells per phase and one DC source. The output current lags the

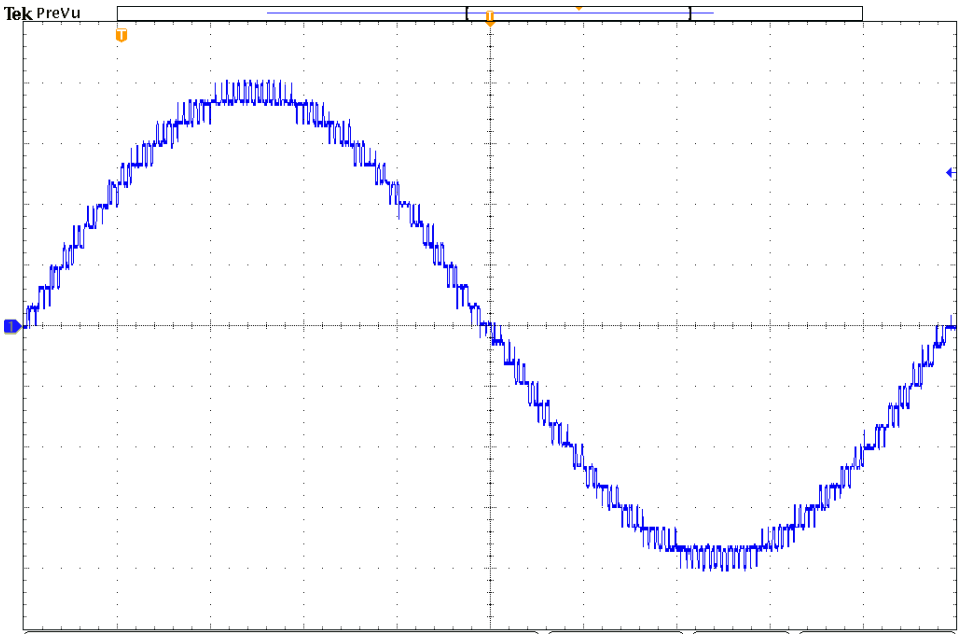


Fig. 23. Detailed twenty-five levels of output voltage V_{out} (3 kV/div) of proposed TOMMC with 3 SMs per arm.

output voltage due to inductive load as shown in Fig. 24. The ancillary voltage and auxiliary voltages are shown in Fig. 25 and Fig. 26; respectively. It can be seen that are following similar waveforms presented in Fig. 12.The capacitor voltages follow the reference value of 2000 V as shown in Fig. 27 under proposed voltage balancing method.

A step change in M has been carried out to verify the effectiveness of the developed controller for the proposed TOMMC. The results are shown in Fig. 28(a) and Fig. 28(b) where M is reduced from 0.95 to 0.5, and increased from 0.5 to 0.8; respectively.

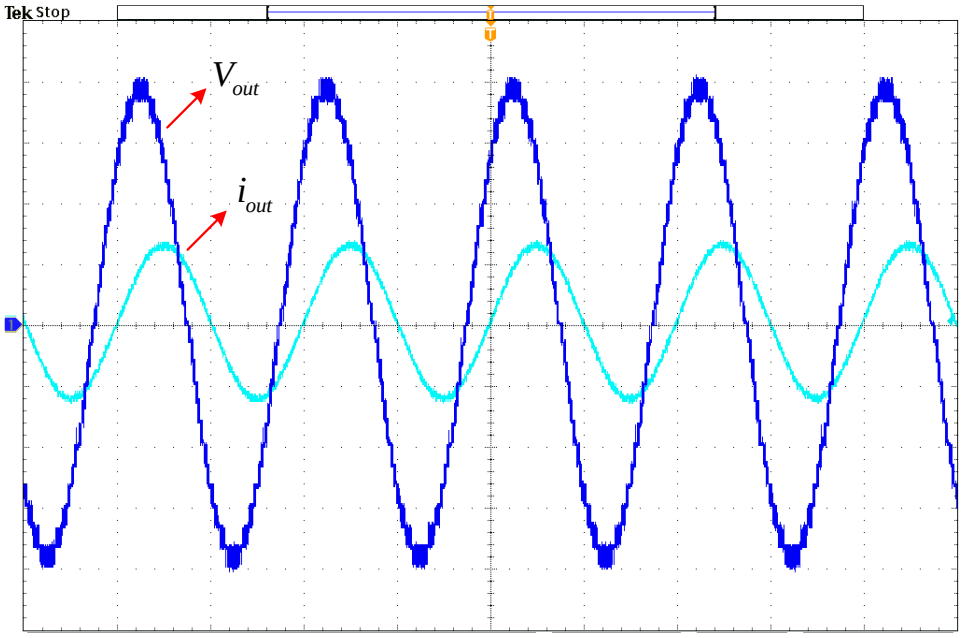


Fig. 24. Experimental HIL result of the V_{out} (3 kV/div) and $10 \times i_{out}$ (3 kA/div)

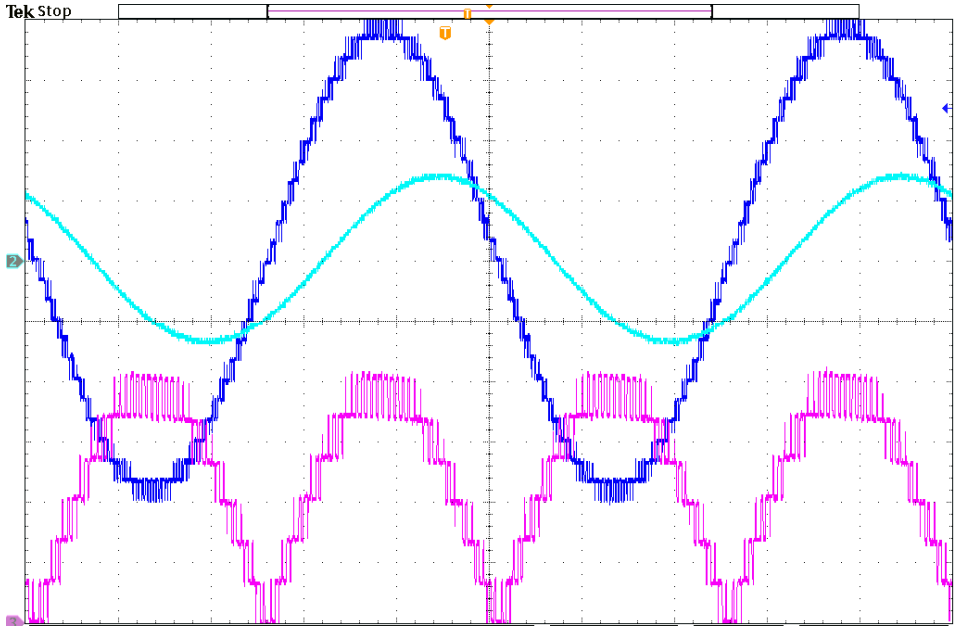


Fig. 25. Ancillary voltage V_{anc} (3kV V/div) shown with output voltage and current

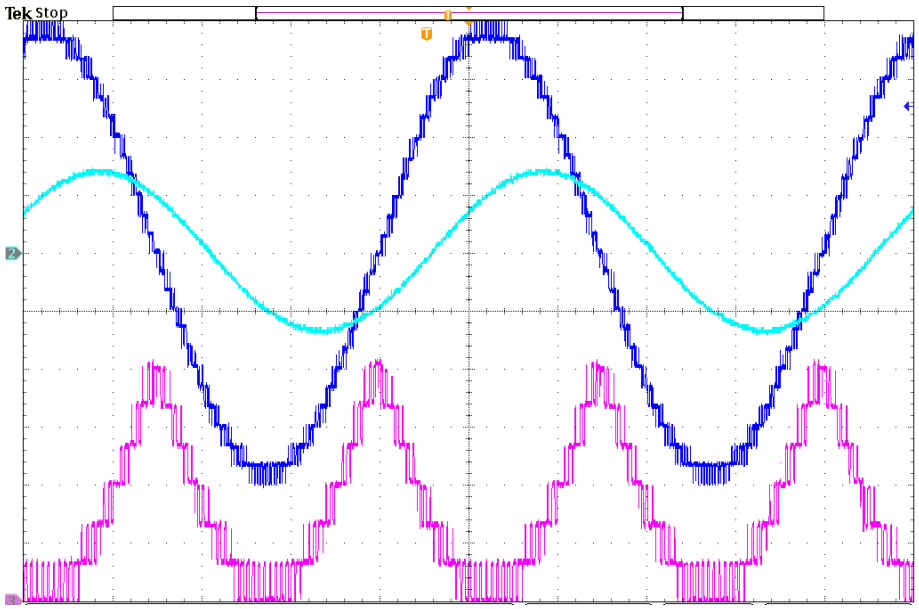


Fig. 26. Auxiliary voltage V_{aux} (3kV V/div) shown with output voltage and current

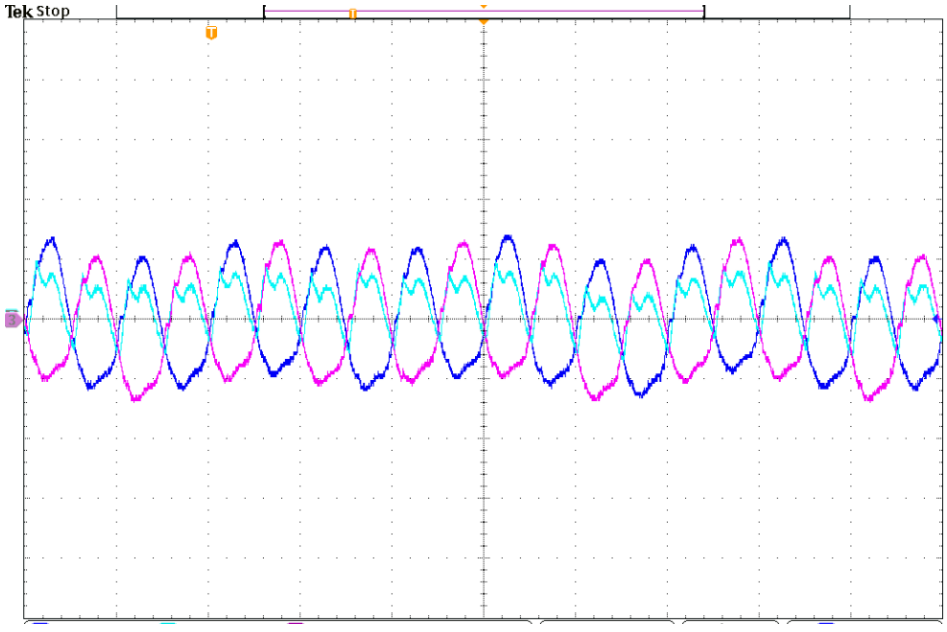
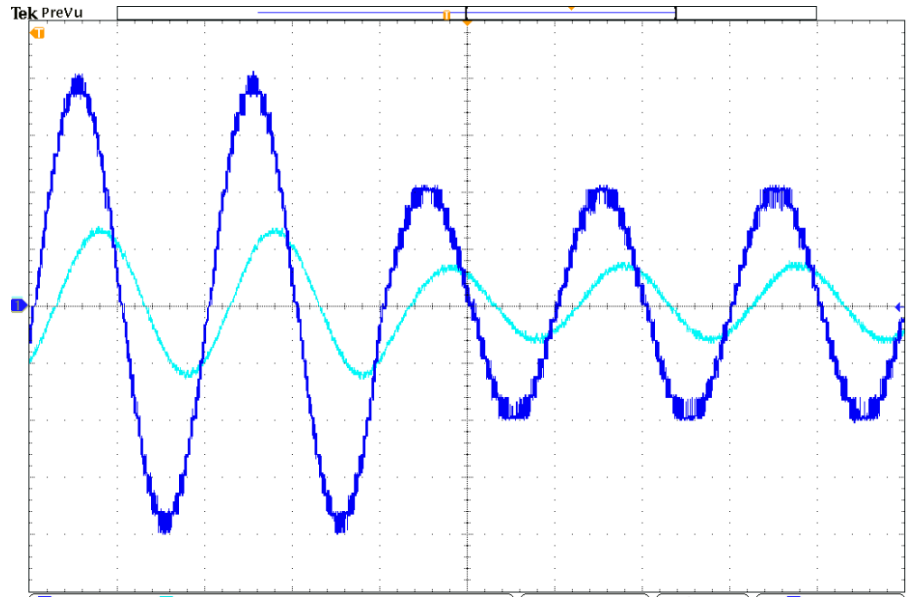
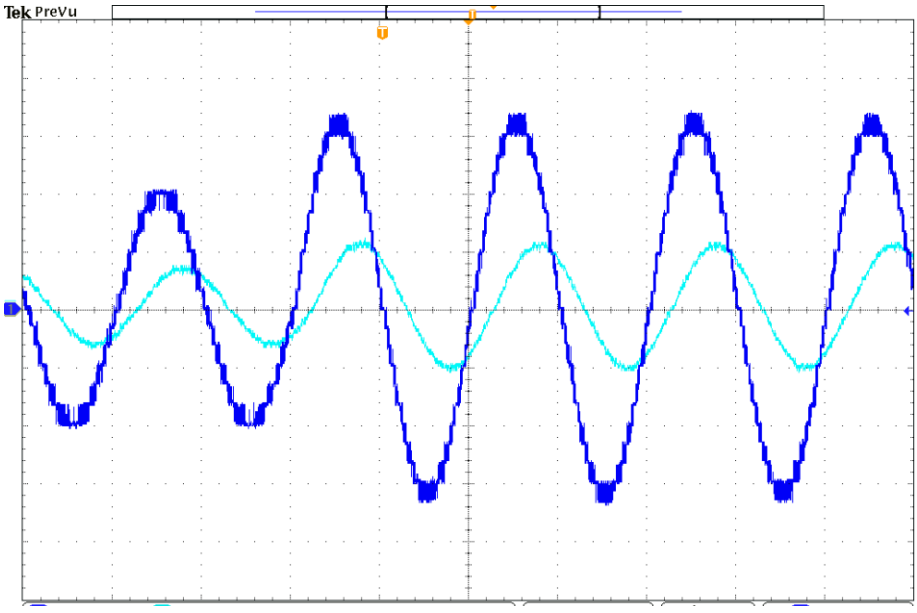


Fig. 27. Capacitor voltage of three arms (50 V/div. The curser is set at 2 kV)



(a)



(b)

Fig. 28. V_{out} (3 kV/div) and $10 \times i_{out}$ (3 kA/div) under step change in *M* (a) from 0.95 to 0.5 (b) from 0.5 to 0.8

Chapter III: PSAR Control of Isolated MMC-Based DC-DC Converters

In this chapter the PSAR control for IMMDC converter will be presented. To do so, first the equivalent circuit model of IMMDC is developed. Then the proposed PSAR control for IMMDC is presented. The current stress in PSAR will be analyzed with respect to different operating points, and will be compared to SPS control. The hardware-in-the-loop experimental results are provided to verify the theoretical outcomes.

3.1. The Equivalent Circuit model of IMMDC Converter

An equivalent circuit model of the two-arrangement IMMDC converter is derived in this section to be leveraged for the reminder of the analysis. The IMMDC converter is shown in Fig. 29. As pictured, the primary and secondary sides of this converter are comprised of two legs, referred to as the primary left leg, primary right leg, secondary left leg, and secondary right leg, hereinafter. Furthermore, each leg is comprised of an upper arm and a lower arm.

Each arm of the primary side legs has the same arm inductance of L_{arm^P}. Therefore, the transformer primary current (i_P) will be evenly distributed between the two arms in primary side legs of the converter. Hence, similar to conventional MMC, the arm currents of the primary side can be formulated as,

$$i_{up^{P,L}} = \frac{i_{dc_1}}{2} + i_{circ^{P,L}} + \frac{i_P}{2} \tag{37}$$

$$i_{low^{P,L}} = \frac{i_{dc_1}}{2} + i_{circ^{P,L}} - \frac{i_P}{2} \tag{38}$$

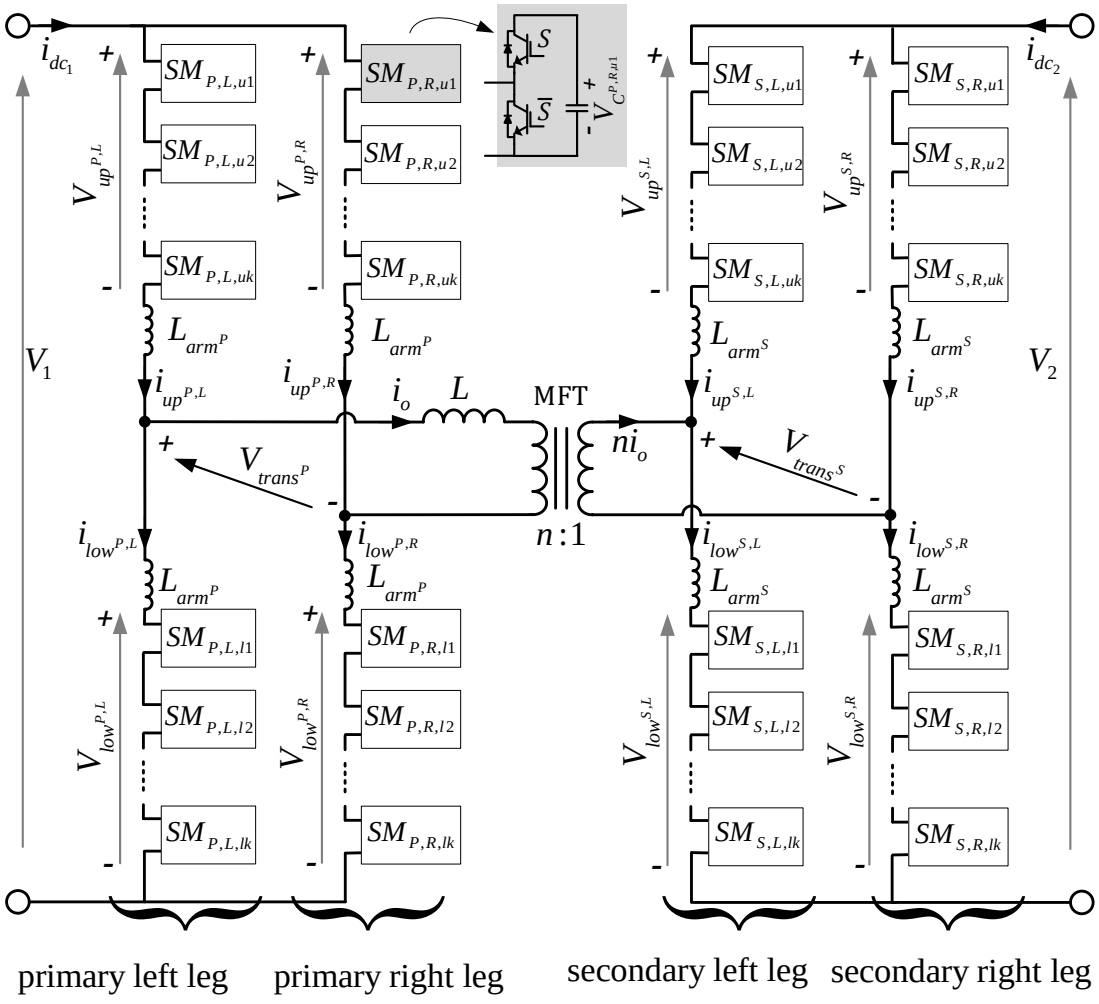


Fig. 29. Two-arrangement IMMDC converter

$$i_{up^{P,R}} = \frac{i_{dc_1}}{2} + i_{circ^{P,R}} - \frac{i_P}{2} \tag{39}$$

$$i_{low^{P,R}} = \frac{i_{dc_1}}{2} + i_{circ^{P,R}} + \frac{i_P}{2} \tag{40}$$

where $i_{up^{P,L}}$, $i_{low^{P,L}}$ are the upper arm and lower arm currents of the primary left leg, and $i_{up^{P,R}}$, and $i_{low^{P,R}}$ are the upper arm and lower arm currents of the primary right leg, respectively.

The i_{circ} terms that represent the circulating current of each leg are comprised of even order harmonics of the arm currents and can be suppressed using circulating suppression method in [63]. Therefore, they will be neglected in the reminder of this analysis. The arm voltage references for the primary left leg can be formulated as,

$$V_{up^{P,L}} = V_{low^{P,R}} = \frac{V_1}{2} + K_1 \frac{V_1}{2} \mathrm{sq}(\mathrm{t}) \tag{41}$$

$$V_{low^{P,L}} = V_{up^{P,R}} = \frac{V_1}{2} - K_1 \frac{V_1}{2} \mathrm{sq}(\mathrm{t}) \tag{42}$$

where K_1 represents the amplitude ratio index of the primary side and is considered to be 1, and $\mathrm{sq(t)}$ represents a square function defined as,

$$\mathrm{sq}(\mathrm{t}) = \begin{cases} +1 \quad if \quad hT_s \le t < (2h+1)\dfrac{T_s}{2} \\ -1 \quad if \quad (2h+1)\dfrac{T_s}{2} \le t < (h+1)T_s \end{cases} \tag{43}$$

where $2T_s\,(=1/\,f\,)$ is the fundamental period of transformer voltages, f is the frequency of transformer voltages, and h is an integer value.

Using this terminology, the voltage on the primary side of the transformer then can be formulated using Kirchhoff's Voltage Law (KVL) as,

$$V_{trans^P} = V_{low^{P,L}} + L_{arm^P} \frac{di_{low^{P,L}}}{dt} - \left(V_{low^{P,R}} + L_{arm^P} \frac{di_{low^{P,R}}}{dt} \right) \tag{44}$$

which by substituting (38), (40), and (42) into (44) will be simplified to,

$$V_{trans^P} = V_p + L_{arm^P} \frac{di_P}{dt} \tag{45}$$

where

$$V_p = K_1 V_1 \mathrm{sq}(\mathrm{t}) \tag{46}$$

In this work, the secondary side arm voltage references are defined with a phase shift with respect to the primary side voltages as,

$$V_{up^{S,L}} = V_{low^{S,R}} = \frac{V_2}{2} + K_2 \frac{V_2}{2} \mathrm{sq}\left(\mathrm{t+D}\left(\frac{\mathrm{T_s}}{2} \right) \right) \tag{47}$$

$$V_{up^{S,R}} = V_{low^{S,L}} = \frac{V_2}{2} - K_2 \frac{V_2}{2} \mathrm{sq}\left(\mathrm{t+D}\left(\frac{\mathrm{T_s}}{2} \right) \right) \tag{48}$$

where *D* is the phase shift ratio of the secondary side voltages with respect to primary side voltages.

A similar analysis as to the primary side for the secondary side circuitry will result in a similar outcome for the transformer secondary voltage,

$$V_{trans^S} = V_s + L_{arm^S} \frac{di_S}{dt} \tag{49}$$

where

$$V_s = K_2 V_2 \mathrm{sq}\left(\mathrm{t\text{-}D}\left(\frac{\mathrm{T_s}}{2} \right) \right) \tag{50}$$

and i_S is the transformer secondary current and is equal to ni_P where n is the transformer turns ratio. It must be noted that in the PSAR control, the amplitude ratio index of the secondary side K_2 can vary from zero to one.

By transferring the equivalent secondary side circuit of the converter described by (49) to the primary side, and using (47) to describe the primary side equivalent circuit, the overall equivalent circuit of the converter can be described by,

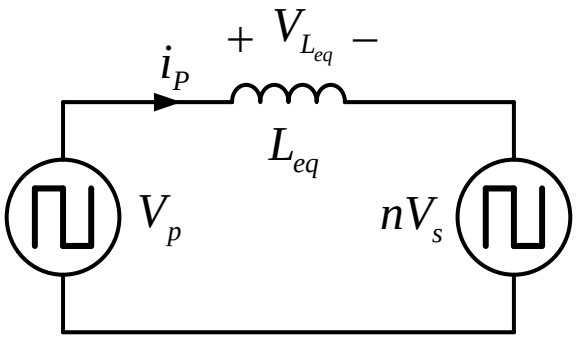


Fig. 30. Two voltage source connected by equivalent inductance

$$V_p - L_{arm^P}\frac{di_P}{dt} - \left(nV_s + n^2 L_{arm^S}\frac{ndi_P}{dt}\right) = \left(L + L_{leq}\right)\frac{di_P}{dt} \tag{51}$$

where L_{leq} is the leakage inductance of the transformer. The result can be further simplified into,

$$V_p - nV_s = L_{eq}\frac{di_P}{dt} \tag{52}$$

where

$$L_{eq} = L_{arm^P} + n^2 L_{arm^S} + L + L_{leq} \tag{53}$$

The resulting derived equivalent circuit of the converter described by (52) and (53) is shown in Fig. 30.

3.2.The Proposed Conjoined PSAR Control for IMMDC

In SPS control scheme, the phase angle of the secondary side voltage is shifted based on the desired power flow level. Theoretically, a phase shift of zero degrees results in zero active power transfer, while a phase shift of 90 degrees results in maximum power transfer. Typically, for the control of IMMDC, the amplitude ratio index for both sides is set to unity since the AC

voltage of the MMC stage can be as high as the DC bus voltage [56]. Therefore, there are very limited works in the literature investigating conjoined phase-shift and voltage amplitude for IMMDC converters. This work lays out the groundworks for implementation of the conjoined PSAR control and investigates its merits compared to conventional control techniques for IMMDC converters in terms of power transfer capability and current stress of the MFT and the power switches.

Fig. 31 illustrates IMMDC current and voltage waveforms while operating with PSAR control. According to this figure, four modes of operation for IMMDC can be defined,

1) Interval $t_0 - t_1$: As pictured, according to (41)-(42) the primary side voltages are $V_{low^{P,L}} = V_{up^{P,R}} = V_1$ and $V_{up^{P,L}} = V_{low^{P,R}} = 0$ resulting in $V_P = V_1$. While due to the PSAR's secondary side phase-shift and voltage amplitude control, the secondary side voltages are $V_{low^{S,L}} = V_{up^{S,R}} = (1-K_2)V_2/2$ and $V_{low^{S,L}} = V_{up^{S,R}} = (1+K_2)V_2/2$ resulting in $V_S = -K_2 V_2$. Therefore, in this interval the voltage over the equivalent inductance in Fig. 30 will be equal to $V_{L_{eq}} = V_1 + nK_2V_2$, which indicates that i_P will be increasing during the interval. The $i_P(t)$ during this interval can be formulated as,

$$i_P{}^{t_0-t_1}(t) = i_P(t_0) + \frac{V_1 + nK_2V_2}{L_{eq}}(t - t_0) \tag{54}$$

where $i_P(t_0)$ is the primary current at $t = t_0$.

2) Interval t_1-t_2: In this interval $V_{low^{P,L}}=V_{up^{P,R}}=V_1$, $V_{up^{P,L}}=V_{low^{P,R}}=0$ resulting in $V_P=V_1$, while $V_{low^{S,R}}=V_{up^{S,L}}=(1-K_2)V_2/2$, $V_{low^{S,L}}=V_{up^{S,R}}=(1+K_2)V_2/2$ resulting in $V_S=K_2V_2$. Therefore, the equivalent inductor voltage will be $V_{L_{eq}}=V_1-nK_2V_2$, which results the following formula for $i_P(t)$

$$i_P^{t_1-t_2}(t)=i_P(t_1)+\frac{V_1-nK_2V_2}{L_{eq}}(t-t_1) \tag{55}$$

where $i_P(t_1)$ is current at time $t=t_1$. Accordingly, based on the operating point of the IMMDC, if $V_1>nK_2V_2$, the primary current i_P would be increasing (as shown in Fig. 31), while if $V_1<nK_2V_2$, the primary current would be decreasing.

3) Interval t_2-t_3: In this interval $V_{low^{P,L}}=V_{up^{P,R}}=0$, $V_{up^{P,L}}=V_{low^{P,R}}=V_1$, resulting in $V_p=-V_1$, while $V_{low^{S,L}}=V_{up^{S,R}}=(1+K_2)V_2/2$ and $V_{low^{S,R}}=V_{up^{S,L}}=(1-K_2)V_2/2$ resulting in $V_S=+K_2V_2$. Therefore, the equivalent inductor voltage will be $V_{L_{eq}}=-V_1-nK_2V_2$, which results the following formula for $i_P(t)$,

$$i_P^{t_2-t_3}(t)=i_P(t_2)-\frac{V_1+nK_2V_2}{L_{eq}}(t-t_2) \tag{56}$$

where $i_P(t_2)$ is current at time $t=t_2$.

3) Interval t_3-t_4: In this interval $V_{low^{P,L}}=V_{up^{P,R}}=0$, $V_{up^{P,L}}=V_{low^{P,R}}=V_1$, resulting in $V_p=-V_1$, while $V_{low^{S,L}}=V_{up^{S,R}}=(1-K_2)V_2/2$ and $V_{low^{S,R}}=V_{up^{S,L}}=(1+K_2)V_2/2$ resulting in $V_S=-K_2V_2$.

Therefore, the equivalent inductor voltage will be $V_{L_{eq}} = -V_1 + nK_2V_2$, which results the following formula for $i_P(t)$

$$i_P{}^{t_3-t_4}(t) = i_P(t_3) + \frac{-V_1 + nK_2V_2}{L_{eq}}(t - t_3) \tag{57}$$

where $i_P(t_3)$ is current at time $t = t_3$.

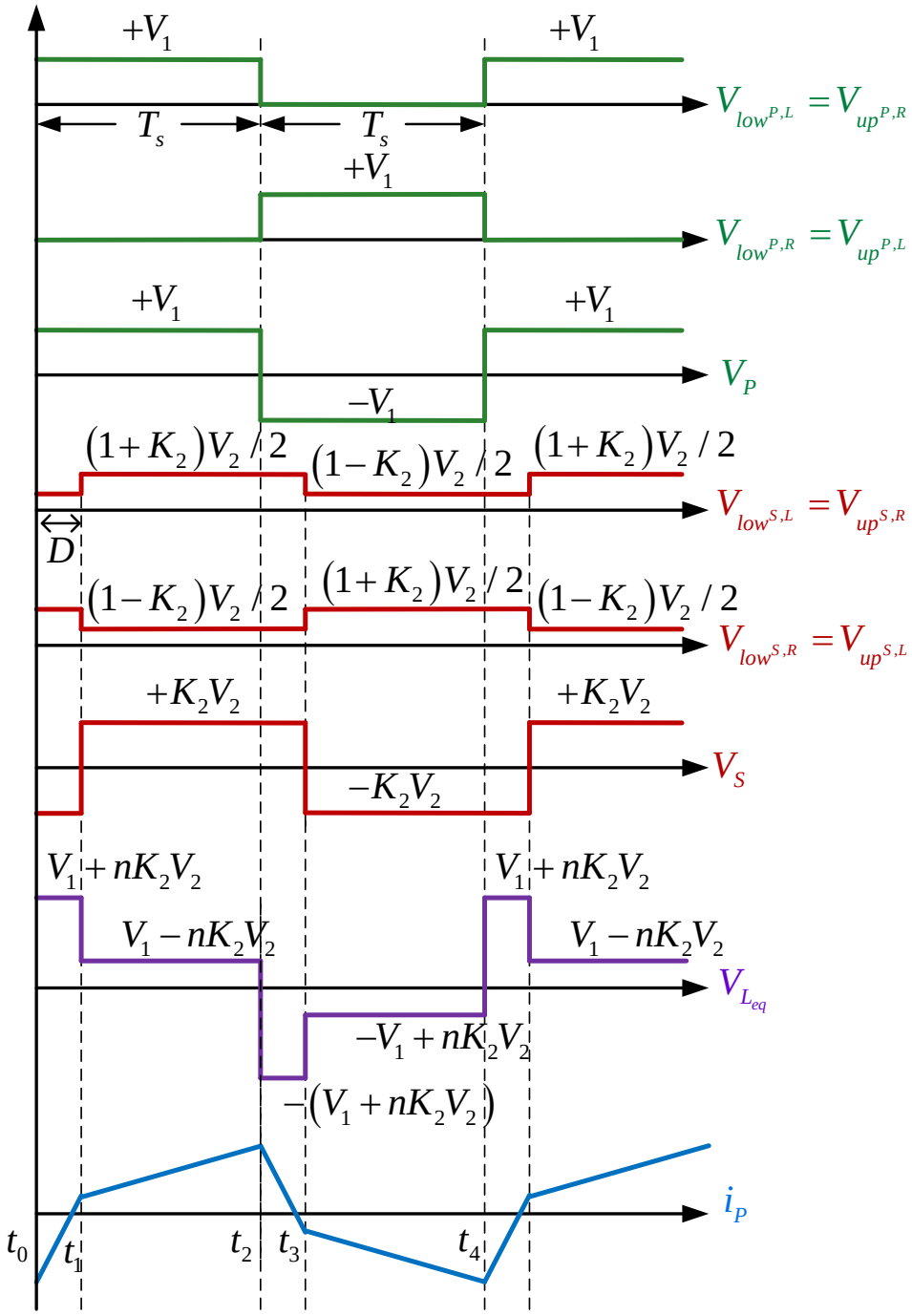


Fig. 31. Waveforms of IMMDC converters in PSAR

Using (54)-(57) the active power transmitted through equivalent inductance using PSAR control can be formulated as,

$$P = \frac{1}{T_s}\int_0^{T_s} V_P(t)\, i_P(t)\, dt = \frac{nK_2V_1V_2D(1-D)}{2L_{eq}f} \tag{58}$$

While for the SPS control, the delivered active power is [57],

$$P' = \frac{nV_1V_2D'(1-D')}{2L_{eq}f} \tag{59}$$

The power transfer capability of SPS and PSAR are compared in Fig. 32 by plotting (58)-(59) for the entire range of D', D and K_2. As pictured, the transferred power using SPS is only a function of employed phase shift (D'), while using PSAR there is more flexibility through controlling the power transfer using the amplitude ratio index (K_2). This flexibility will be leveraged in the next chapter to find IMMDC operating points while using PSAR which offer lower MFT and power switch current stresses compared to using SPS, while delivering the same amount of power.

3.3. Current Stress Comparison of SPS and PSAR for IMMDC Converter

According to inductor volt-second balance principle, the average equivalent inductor current over one period ($2T_s$) is zero in steady state condition. The symmetry of equivalent inductor voltages over a period as shown in Fig. 31 then dictates that $i_P(t=t_0) = -i_P(t=t_2=t_0+T_s)$. Therefore, in case $V_1 > nV_2$ the maximum primary side current occurs at $t=t_2$, indicating that $i_P(t=t_2) = i_p^{\max} = -i_P(t=t_0)$. This maximum value can be found by

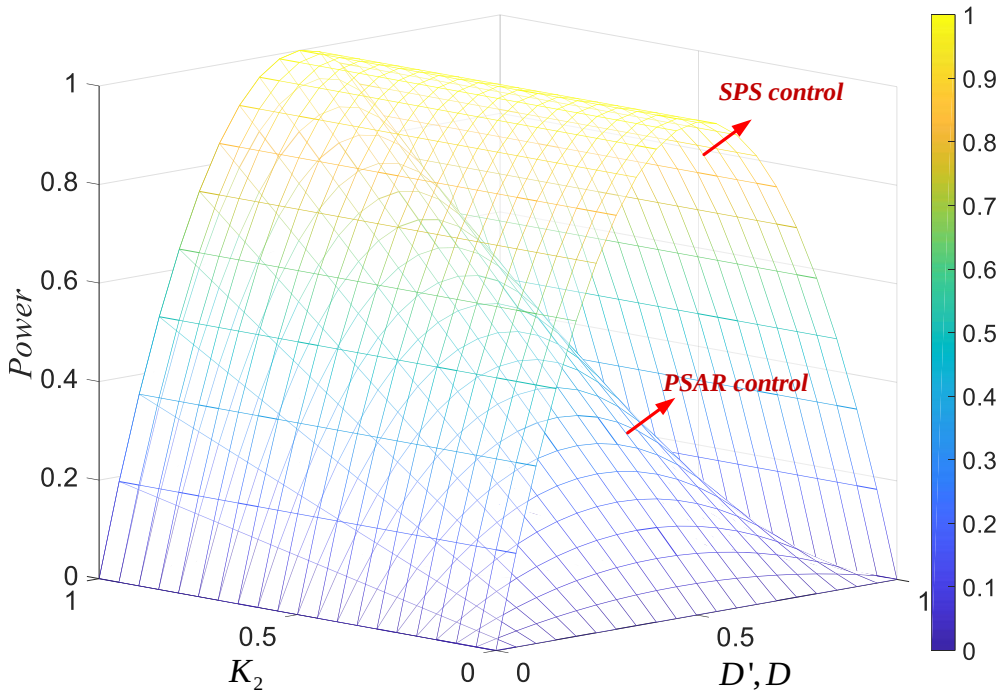


Fig. 32. IMMDC delivered power comparison using SPS vs. PSAR control. For SPS control, K_2 is conventionally equal to 1 and power is only a function of D'. For PSAR control, K_2 can vary from 0 to 1 for any D value.

calculating $i_p(t=t_1)$ using (54) in terms of $i_P(t=t_0)=-i_p^{\max}$, and in turn using this result to calculate $i_p(t=t_2)$ in terms $i_p(t=t_1)$ by employing (55). The resulting equation for $i_p(t=t_2)$ can then be simplified to find the maximum primary side current that coincides with the current stress of the MFT when using PSAR control,

$$i_P^{\max}=\frac{1}{4L_{eq}f}\left(V_1-nK_2V_2\left(1-2D\right)\right) \tag{60}$$

The case of $V_1<nV_2$ on the other hand, needs to be broken down into two instances based on the values of V_1 and nK_2V_2. If $V_1<nV_2$ and $V_1<nK_2V_2$, the maximum value of $i_P(t)$ occurs at

$t = t_1$ while if $V_1 < nV_2$ and $V_1 > nK_2V_2$, the maximum value of $i_P(t)$ occurs at $t = t_2$. The maximum primary side current for each case can be formulated similar to above using (54)-(57) as,

$$i_P^{\max} = \begin{cases} \frac{1}{4L_{eq}f}\left((2D-1)V_1 + nK_2V_2\right) & \text{if } V_1 < nK_2V_2 \\ \frac{1}{4L_{eq}f}\left(V_1 - nK_2V_2\left(1-2D\right)\right) & \text{if } V_1 \geq nK_2V_2 \end{cases} \tag{61}$$

Similarly, while using SPS the maximum primary side current can be formulated as,

$$i'^{\max}_P = \frac{1}{4L_{eq}f}\left(V_1 - nV_2\left(1-2D'\right)\right) \tag{62}$$

when $V_1 > nV_2$ and as,

$$i'^{\max}_P = \frac{1}{4L_{eq}f}\left((2D'-1)V_1 + nV_2\right) \tag{63}$$

when $V_1 < nV_2$.

As mentioned above, since $i_P(t)$ in Fig. 29 and Fig. 30 denotes the current flowing through MFT, the $i_P^{\max}$ found in (60)-(63) represents the current stress of MFT in an IMMDC. On the other hand, since the delivered power by the primary side of the IMDDC can be formulated as $P = P' = V_1 \times i_{dc_1}$ when using either SPS or PSAR, given the same V_1 for the two control methods, the i_{dc_1} will be essentially the same irrespective of the control method. Meaning that according to (37)-(40) the maximum value of IMMDC primary arm currents depend on $i_P^{\max}$ as well. A similar argument can be made for the secondary side as well, implying that $i_P^{\max}$ is an indicator of the current stress on all of the IMMDC power switches.

As a result, in this section the SPS and PSAR methods are compared based on evaluating $i_P^{\max}$ and $i'^{\max}_P$ when using the two control methods. To conduct a fair analysis, comparison is made at the same delivered active power levels by the IMMDC when using the two control methods ($P = P'$ for comparison). Also, since the amount of transferred power is symmetrical relative to $D, D' = 0.5$ plane as shown in Fig. 32, and since current stress in (60)-(63) increases linearly with D and D', its only necessary to conduct the comparison for the range of $0 < D, D' \le 0.5$. In the following, the current stress is analyzed for two cases based on the relative voltages of the two DC networks.

3.2.1 *Case A:* $V_1 > nV_2$ *which yields* $V_1 > nK_2V_2$

To compare the current stress for the same transferred power level for SPS and PSAR, $P = P'$ can be solved for K_2 by equating (58) and (59), which results in,

$$K_2 = \frac{D'(1-D')}{D(1-D)} \tag{64}$$

Examining (64) knowing that $D, D' \le 0.5$, one can easily conclude that in order to have $0 \le K_2 \le 1$, then D has to be larger than (or equal to) $D'\left(D' \le D\right)$. Meaning that in all cases the phase shift for PSAR needs to be larger than (or equal to) that of SPS to transfer the same amount of power. On the other hand, comparing (60) and (62), for having a smaller $i_P^{\max}$ when using PSAR, the $nK_2V_2(1-2D)$ term needs to be larger than $nV_2(1-2D')$, which considering $D' \le D$ condition, can at best happen when $K_2 = 1$ which results in $D = D'$. Meaning that the PSAR control in Case A can at best have the same current stress as SPS when $K_2 = 1$. Therefore, if

$V_1 > nV_2$ there is no operating point in which current stress when using PSAR is less than when using SPS.

3.2.2 *Case B1:* $V_1 < nV_2$ *and* $V_1 > nK_2V_2$

Before comparing the current stress in this case, the boundary of Case B1 $V_1 > nK_2V_2$ defined above is analyzed. The Case B1 boundary can be reformulated as $m > K_2$ where m is defined as V_1/nV_2. Substituting K_2 from (64) for equal power comparison will then yield,

$$D(1-D) > \frac{D'(1-D')}{m} \tag{65}$$

It must be noted that m is fixed since the voltage level ratio of the two DC networks are fixed, however, D' can be determined using (59) for any desired power level. Also, it can be easily shown that any D that fulfills (65) will also fulfill the $D' \le D$ condition discussed above since $m < 1$. To analyze (65), it can be reformatted as $\mathrm{R}(D) = -D^2 + D - D'(1-D')/m > 0$. Then, the range of $\mathrm{R}(D)$ can be determined by finding the solutions of $\mathrm{R}(D) = 0$, which are

$$\begin{cases} D_{R1} = 0.5 + 0.5\sqrt{1 - 4D'(1-D')/m} \\ D_{R2} = 0.5 - 0.5\sqrt{1 - 4D'(1-D')/m} \end{cases} \tag{66}$$

The D_{R1} is an unacceptable solution since it is out of the $0 < D \le 0.5$ range. The D_{R2} is an acceptable solution only if $1 - 4D'(1-D')/m > 0$ which dictates,

$$4D'(1-D') < m \tag{67}$$

Given that the quadratic coefficient of $\mathrm{R}(D)$ is negative (-1) and $D_{R2} < 0.5 < D_{R1}$, then $\mathrm{R}(D)$ is positive for the range of $(D_{R2}, 0.5)$. This completes the analysis on $V_1 > nK_2V_2$.

For current stress comparison and according to (60) and (62), having $i_P^{\max} < i'^{\max}_P$ can be formulated as,

$$\frac{1}{4L_{eq}f}\left(V_1 + (2D-1)nK_2V_2\right) < \frac{1}{4L_{eq}f}\left((2D'-1)V_1 + nV_2\right) \tag{68}$$

which can be simplified to,

$$m + (2D-1)K_2 < (2D'-1)m + 1 \tag{69}$$

Substituting (64) into (69) for equal power comparison will result in,

$$\mathrm{E}(D,D') = 2(1-D')m + (2D-1)\frac{D'(1-D')}{D(1-D)} - 1 < 0 \tag{70}$$

which can be rearranged in the form of,

$$\mathrm{E}(D,D') = \frac{\mathrm{F}(D,D')}{D(1-D)} < 0 \tag{71}$$

where

$$\begin{aligned}\mathrm{F}(D,D') = {} & \left(1 + 2m(D'-1)\right)D^2 \\ & + \left(2D'(1-D') + 2m(1-D') - 1\right)D - (1-D')D'\end{aligned} \tag{72}$$

According to (71), since $D(1-D) \geq 0$ for $0 \leq D < 0.5$, then $\mathrm{E}(D,D')$ is less than zero if $\mathrm{F}(D,D') < 0$. The range of $\mathrm{F}(D,D')$ function can be evaluated considering that $\mathrm{F}(D,D')$ is a quadratic equation with respect to D, where $a = 1 + 2m(D'-1)$, $b = 2D'(1-D') + 2m(1-D') - 1$

and $c = -(1-D')D'$ are the coefficients. Subsequently, the range is evaluated for the two cases of $a \geq 0$ and $a < 0$.

3.2.3 Case B1.1

Case B1.1 for $a \geq 0$ which dictates that $m \leq 1/2(1-D')$: In this case since $\mathrm{F}(D,D')\big|_{D=0} = -D'(1-D')$ is always less than or equal to zero for the entire range of D', and $\mathrm{F}(D,D')\big|_{D=0.5} = (2m(1-D')-1)/4$ is less than or equal to zero for $m \leq 1/2(1-D')$, the quadratic function will be negative for a certain the range of D. This range can be determined considering that D and D' need to also satisfy $a \geq 0$ and $V_1 > nK_2V_2$ (Case B1 boundary defined above). As mentioned previously, $a \geq 0$ will simply be satisfied with,

$$m \leq \frac{1}{2(1-D')} \tag{73}$$

Meaning that for any m and D' which satisfy (67) and (73), D can be selected from the $(D_{R2}, 0.5)$ range which results in $\mathrm{E}(D,D') < 0$ and thus yields a current stress for SPAR which is less than that of SPS. After selecting D from the $(D_{R2}, 0.5)$ range, a corresponding K_2 can be calculated using (64). The resulting D and K_2 pair can then be used in (47)-(48) to generate voltages for the secondary side of the converter using PSAR.

The inequalities of (67) and (73) are plotted in Fig. 33(a) to illustrate the range of D' and m where $i_P^{\max}$ can be made lower than $i_P'^{\max}$. The dashed region in Fig. 33(a) shows the acceptable operating region. The interconnection of the two curves is at $(D', m) = (0.19, 0.62)$.

Finally, it should be noted that although any obtained D and K_2 pair will lead to less current stress than when using SPS, however, the current stress for different D and K_2 pairs will be different. The best operating point from $(D_{R2}, 0.5)$ which results in the least current stress then can be determined by taking the derivative of $\mathrm{E}(D, D')$ with respect to D,

$$\frac{\partial \mathrm{E}(D, D')}{\partial D} = \frac{2D(1-D) + (2D-1)^2 D'(1-D')}{\left(D(1-D)\right)^2} \tag{74}$$

Since (74) is clearly always positive, the best operating point with the least current stress will happen at $D_b = D_{R2}$.

3.2.4 Case B1.2

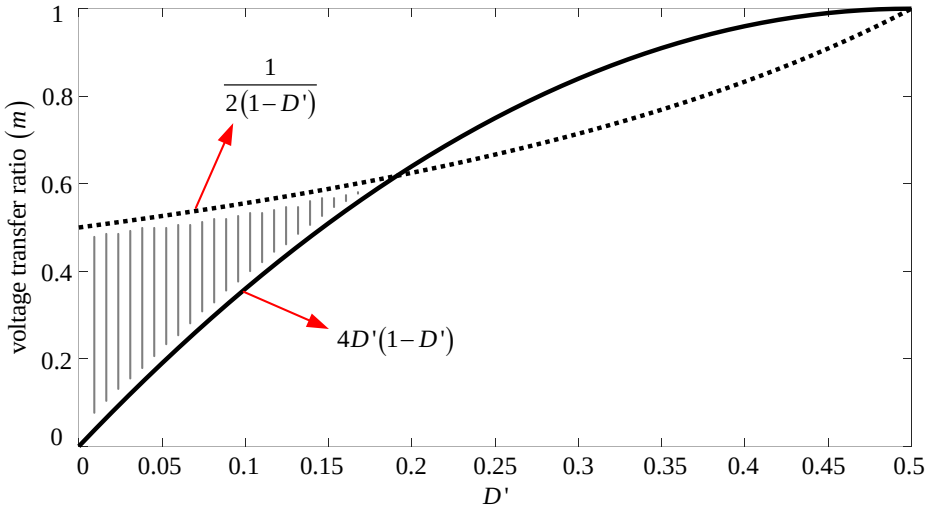
Case B1.2 for $a < 0$ which dictates that $m > 1/2(1-D')$: In this case, it can be shown that $\mathrm{F}(D, D')\big|_{D=0}$ is negative while $\mathrm{F}(D, D')\big|_{D=0.5}$ is positive. Therefore, since $a < 0$, the $\mathrm{F}(D, D')$ will be negative for the range $(0, D_{rF})$ where D_{rF} is a root of $\mathrm{F}(D, D') = 0$ with a value between 0 and 0.5. Solving $\mathrm{F}(D, D') = 0$ will result in,

$$\begin{cases} D_{F1} = \dfrac{-\left(2\left(D'+m\right)\left(1-D'\right)-1\right)+\sqrt{q}}{2+4m\left(D'-1\right)} \\ D_{F2} = \dfrac{-\left(2\left(D'+m\right)\left(1-D'\right)-1\right)-\sqrt{q}}{2+4m\left(D'-1\right)} \\ \text{where} \\ q = \left(2\left(D'+m\right)\left(1-D'\right)-1\right)^2 + 4\left(1+2m\left(D'-1\right)\right)\left(1-D'\right)D' \end{cases} \tag{75}$$

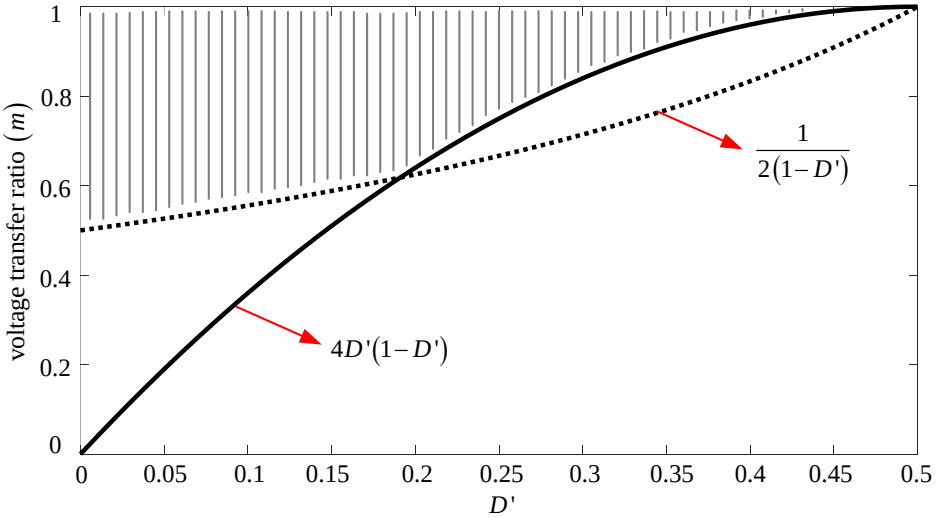
It can be shown that both solutions D_{F1} and D_{F2} exist, while only D_{F1} is between 0 and 0.5. Therefore, it can be concluded that $\mathrm{F}\left(D, D'\right)$ is negative for $\left(0, D_{F1}\right)$. Nevertheless, similar to Case B1.1 we also need to consider additional constraints to narrow down this region. As mentioned earlier, the $a < 0$ condition will be satisfied with,

$$m > \frac{1}{2\left(1-D'\right)} \tag{76}$$

while similar to Case B1.1, the $V_1 > nK_2V_2$ and the equal power comparison conditions will result in (65) and eventually (67), yielding an acceptable region of $\left(D_{R2}, 0.5\right)$. Merging the two regions of $\left(0, D_{F1}\right)$ and $\left(D_{R2}, 0.5\right)$ will result in final acceptable range of $\left(D_{R2}, D_{F1}\right)$. The conditions in (67) and (76) for Case B1.2 are shown in Fig. 33 (b). Similar to previous case, we can conclude that for any m and D' that fall in the highlighted region in Fig. 33 (b), an arbitrary D can be selected from the $\left(D_{R2}, D_{F1}\right)$ range which results in $F\left(D, D'\right) < 0$. It should be noted that $\left(D_{R2}, D_{F1}\right)$ region is found by assuming that D_{F1} is larger than D_{R2}. In case D_{F1} is found to be smaller than D_{R2}, there will be no acceptable operating point for Case B1.2 which would result in less current stress using SPAR. Furthermore, since as shown earlier in (74) the $\partial \mathrm{E}\left(D, D'\right)/\partial D$ is



(a)



(b)

Fig. 33. (a) Case B1.1: regions of m and D' to have $a \geq 0$ (b) Case B1.2: regions of m and D' to have $a < 0$.

positive for any D in the (D_{R2}, D_{F1}) range, the $D = D_{R2}$ point will result in the least current stress

3.2.5 Case B2: $V_1 < nK_2V_2$

Similarly first the boundary condition for case B2 ($V_1 < nK_2V_2$) is analyzed. Substituting K_2 from (64) for equal power comparison will then yield:

$$D(1-D) < \frac{D'(1-D')}{m} \tag{77}$$

which is the same as $\mathrm{R}(D) < 0$ where $\mathrm{R}(D)$ is defined earlier. By following similar discussions as above, we can conclude if $4D'(1-D') > m$ then (41) will hold true for any D in $(D', 0.5)$. If m and D' fulfil $4D'(1-D') > m$ they are called to be in region 1. However, if $4D'(1-D') < m$ then the acceptable range of D to fulfill (41) is (D', D_{R2}) where D_{R2} is obtained in (30). If m and D' fulfil $4D'(1-D') < m$ they are called to be in region 2. The condition for D to be larger than D' is a basic condition that has to be considered. It can be proved that D_{R2} is always greater than D'.

For current stress comparison and according to (61) and (63), having $i_P^{\max} < i_P'^{\max}$ can be formulated as,

$$\frac{1}{4L_{eq}f}\left((2D-1)V_1 + nK_2V_2\right) < \frac{1}{4L_{eq}f}\left((2D'-1)V_1 + nV_2\right) \tag{78}$$

which can be simplified using (64) to,

$$J(D, D') = 2(D-D')m + \frac{D'(1-D')}{D(1-D)} - 1 < 0 \tag{79}$$

The defined $J(D, D')$ term in turn can be rearranged as,

$$\mathrm{J}(D, D') = \frac{\mathrm{H}(D, D')}{D(1-D)} < 0 \tag{80}$$

where

$$\begin{aligned}\mathrm{H}\left(D,D'\right)=&-2mD^3+\left(2m\left(1+D'\right)+1\right)D^2\\&-\left(2mD'+1\right)D-D'^2+D'\end{aligned}\tag{81}$$

According to (80), since $D\left(1-D\right)$ is always positive for $0<D<0.5$, then $\mathrm{J}\left(D,D'\right)$ is negative if $\mathrm{H}\left(D,D'\right)<0$, satisfying (78) and thus resulting in a lower current stress using PSAR compared to SPS. The range of $\mathrm{H}\left(D,D'\right)$ can be evaluated by finding the roots of $\mathrm{H}\left(D,D'\right)=0$,

$$\begin{cases}D_{H1}=D'\\D_{H2}=\dfrac{2m+1-\sqrt{4m\left(m+2D'-1\right)+1}}{4m}\\D_{H3}=\dfrac{2m+1+\sqrt{4m\left(m+2D'-1\right)+1}}{4m}\end{cases}\tag{82}$$

According to (82), since $4m\left(m+2D'-1\right)+1$ is positive for $0<m<1$ and $0<D<0.5$, the $\mathrm{H}\left(D,D'\right)$ has three positive real poles, however, since D_{H3} is larger than 0.5, it will be ignored for the rest of the analysis. The range of $\mathrm{H}\left(D,D'\right)$ as a function of D then will depend on the values of D_{H1} and D_{H2} which depend on m and D'. As shown in Fig. 34, the $\mathrm{H}\left(D\right)$ has one or two poles in the $0<D<0.5$ region, based on the values of D_{H1} and D_{H2}. Therefore, the study of range of $\mathrm{H}\left(D,D'\right)$ can be carried-out by considering the three possible cases shown in Fig. 34. Case B2.1 will be studied for $D_{H2}>0.5$, while Case B2.2 will be studied if $D_{H1}<D_{H2}<0.5$, and Case B2.3 will be studied when $D_{H2}<D_{H1}<0.5$.

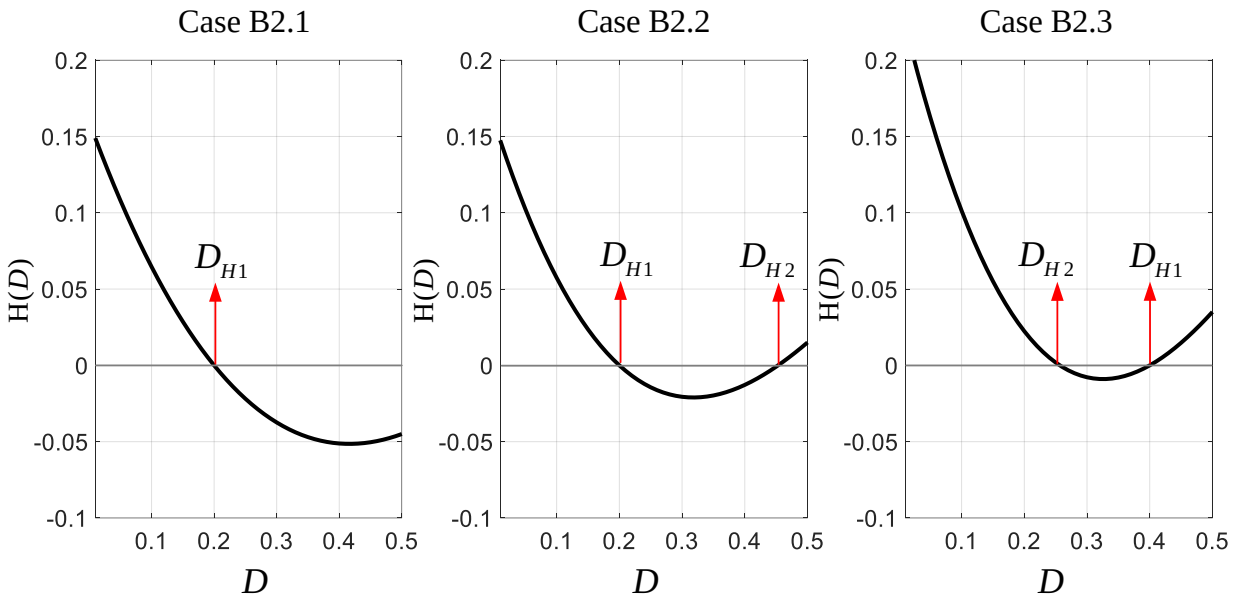


Fig. 34. Three different cases based on D_{H1} and D_{H2}. Case B2.1: for an example case of $m = 0.3$ and $D' = 0.2$, Case B2.2: for an example case of $m = 0.7$ and $D' = 0.2$, Case B2.3: for an example case of $m = 0.9$ and $D' = 0.4$

3.2.6 Case B2.1

It can be shown for D_{H2} to be greater than 0.5, following equation has to hold true:

$$\frac{1}{2}+\frac{1}{4m}-\frac{\sqrt{4m\left(m+2D'-1\right)+1}}{4m}>\frac{1}{2} \tag{83}$$

which can be simplified as

$$m<1-2D' \tag{84}$$

In case B2.1 shown in Fig. 34, the D_{H2} is greater than 0.5 as (84) holds true. D_{H1} is the only pole of $\mathrm{H}\left(D,D'\right)$ in the region of $0<D<0.5$.

Similar to before, the $V_1 < nK_2V_2$ and the equal power comparison conditions for this case need to be evaluated to find the acceptable range of D for lower current stress operation using SPAR. Regarding discussions on results for (77) and (84), acceptable range of m and D' for case B2.1 can be plotted in Fig. 35(a). Therefore, if m and D' fall in the region 1 of Fig. 35 (a), any D which is larger than D' is a solution yielding an $i_P^{\max}$ less than $i_P^{'\max}$. If m and D' fall in the region 2 of Fig. 35 (a), then any D which is larger than D' and less than D_{R2} is an acceptable solution.

For investigating the best operating point and by taking derivative of $\mathrm{J}(D,D')$ with respect to D, we can have:

$$\frac{\partial \mathrm{J}(D,D')}{\partial D} = 2m + \frac{(2D-1)D'(1-D')}{D^2(1-D)^2} \tag{85}$$

It should be noted that $\mathrm{J}(D=D')=0$ and $\mathrm{J}(D=0.5)= \; m(1-2D')+4D'(1-D')-1$ is equal or less than zero for $0 \le D' \le 0.5$. It can be shown that $\frac{\partial \mathrm{J}(D,D')}{\partial D}|_{D=0.5} = 2m$ is greater than or equal to zero. Therefore, it can be shown that $\frac{\partial \mathrm{J}(D,D')}{\partial D}$ has a root between and 0.5. Solving (85) will result in a quartic equation. Using Ferrari's method by back changing the variables, the local minimum of between and 0.5 can be obtained as:

$$D_{\mathrm{J\,min}} = \frac{1}{2}\left(1 - Z + \sqrt{1 + \frac{2D'(1-D')}{mZ} - Z^2}\right) \tag{86}$$

where $Z = \sqrt{\frac{1}{3} + \frac{W}{6m} + \frac{2m}{W}}$, $W = \sqrt{\frac{\Delta_1 + \sqrt{\Delta_1^2 - 256m^6}}{2}}$, and $\Delta_1 = 16m^3 + 216mD'^2(1-D')^2$.

The operating point at $D_b = D_{\mathrm{J}\min}$ is the best operating point with the least current stress in region 1 of case B2.1. In region 2 of case B2.1, $D_b = \min\left(D_{\mathrm{J}\min}, D_{R2}\right)$ is the best operating point with the least current stress.

For smaller m values, i.e. operating with a high step-down ratio, $\mathrm{J}\left(D, D'\right)$ can be written as,

$$\mathrm{J}\left(D, D'\right)_{m\to 0} = \frac{D'\left(1-D'\right)}{D\left(1-D\right)} - 1 \tag{87}$$

which is less than zero for any D greater than D'. Therefore for $m \to 0$ any D greater than D' will result in currents stress in PSAR to be lower compared to SPS. The same result can be interpreted from Fig. 35 (a) that as $m \to 0$, for any delivered power and its subsequent D', the PSAR will have less current stress compared to SPS control.

3.2.7 Case B2.2

In case B2.2, D_{H2} is less than 0.5 which indicates that,

$$m > 1 - 2D' \tag{88}$$

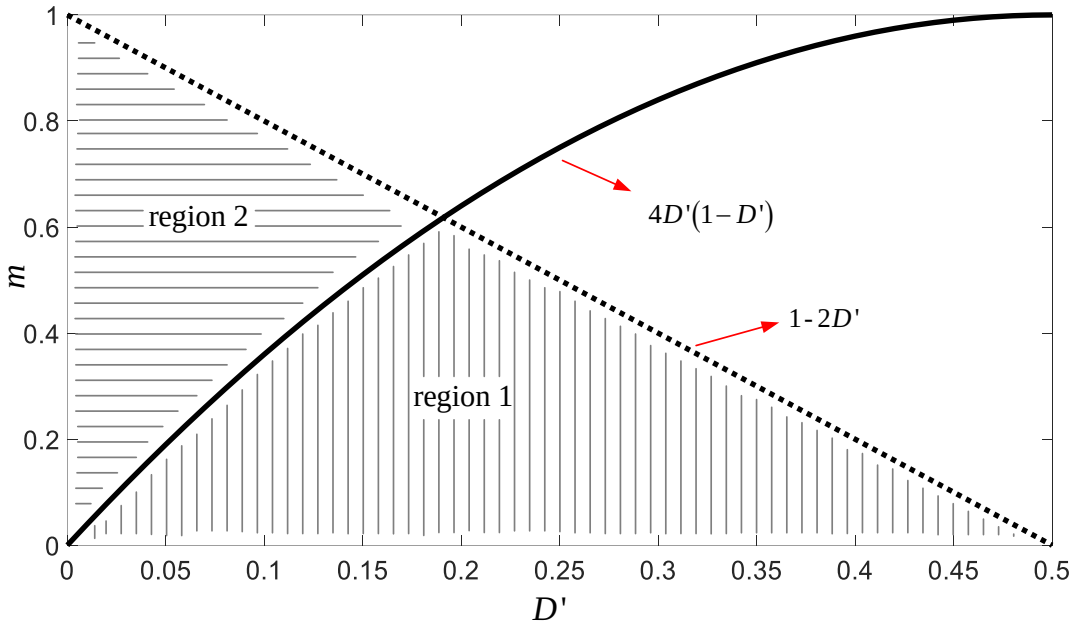
In addition, in this case $D_{H2} > D_{H1}$ which using (82) can be simplified to,

$$m < \frac{1-2D'}{2D'\left(1-D'\right)} \tag{89}$$

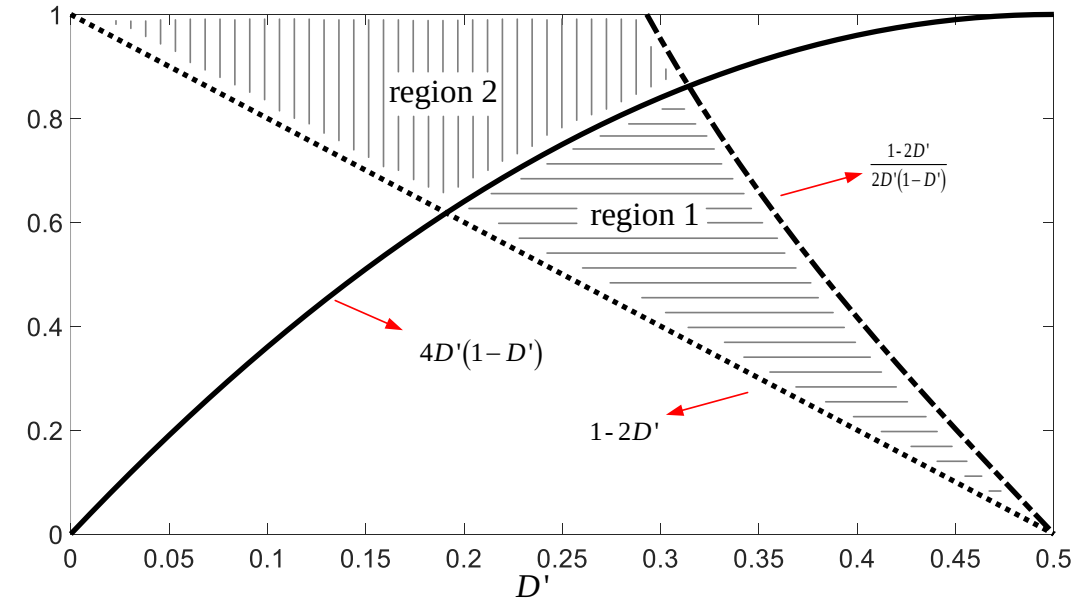
Therefore, using (88) and (89) combined with the condition discussed on (77), the acceptable regions for m and D' for case B2.2 are plotted in Fig. 35 (b). If m and D' fall in region 1 of Fig.

35 (b), any D which is larger than D' and less than D_{H2} is a solution which yields an $i_P^{\max}$ less than $i_P'^{\max}$. The $D = D_{\mathrm{J}\min}$ operating point is the best operating point with least current stress in region 1. If m and D' fall in region 2 of Fig. 35 (b), then any D which is larger than D' and less than $\min\left(D_{H2}, D_{R2}\right)$ is an acceptable solution. In this case $D = \min\left(D_{\mathrm{J}\min}, \min\left(D_{H2}, D_{R2}\right)\right)$ is the best operating point yielding the least current stress.

Finally, it should be noted as D need to be greater than D', case B2.3 does not result in PSAR to have lower current stress than in SPS. It is because the region of D for function H to be negative is $\left(D_{H2}, D_{H1}\right)$ according to Fig. 34; while $D_{H1} = D'$ according to (46). So, any D greater than D' will not be in the $\left(D_{H2}, D_{H1}\right)$ region.



(a)



(b)

Fig. 35. (a) Range of m and D' for Region 1 and Region 2 of case B2.1 (b) Range of m and D' for Region 1 and Region 2 of case B2.2

Table VII summarizes the analysis and findings related to different cases investigated in this work. Fig. 36 illustrates a flowchart that is provided for simple implementation of the PSAR control to work at the least current stress operating point. It can be seen from the left branch of Fig. 36 that there can be pair of m and D' that be common in case B1 and case B2. Hence, the best operating points in each case is obtained separately. D_{b1} and associated K_2 are obtained for case B1, and by inserting them into (61) the associated $i_{p,b1}^{\max}$ is obtained. Similarly, D_{b2} and associated K_2 are obtained for Regions 2 of case B2, and by inserting them into (61) the associated $i_{p,b2}^{\max}$ is obtained. By comparing the maximum current stress of the two points, the one with less maximum current stress will be the final operating point. The output of the PSAR control are D_b and K_2 which will be employed in (47) and (48) to obtain the reference voltages of the upper and lower arms of the MMC on secondary side of transformer

Table VII
Summarizing results of different cases

Case		Regions of D to have $i_P^{\max} < i'^{\max}_P$	Conditions for m and D' to fulfil	Best Operating point D_b
Case A1 $V_1 > nV_2$			-	-
Case B1 $V_1 < nV_2$ & $V_1 > nK_2V_2$	**Case B1.1** quadratic coefficient in (72) is positive	$(D_{R2}, 0.5)$	$4D'(1-D') < m$ & $m \le \frac{1}{2(1-D')}$	$D_b = D_{R2}$
	Case B1.2 quadratic coefficient in (72) is negative	(D_{R2}, D_{F1}) D_{F1} is larger than D_{R2}.	$4D'(1-D') < m$ & $m > \frac{1}{2(1-D')}$	$D_b = D_{R2}$
Case B2 $V_1 < nV_2$ & $V_1 < nK_2V_2$	**Case B2.1** $D_{H2} > 0.5$	Region 1: $(D', 0.5)$	$4D'(1-D') > m$ & $m < 1-2D'$	$D_b = D_{J\min}$
		Region 2: (D', D_{R2})	$4D'(1-D') < m$ & $m < 1-2D'$	$D_b = \min(D_{J\min}, D_{R2})$
	Case B2.2 $D_{H1} < D_{H2} < 0.5$	Region 1: (D', D_{H2})	$4D'(1-D') > m$ & $m > 1-2D'$ & $m < \frac{1-2D'}{2D'(1-D')}$	$D_b = D_{J\min}$
		Region 2: $(D', \min(D_{H2}, D_{R2}))$	$4D'(1-D') < m$ & $m > 1-2D'$ & $m < \frac{1-2D'}{2D'(1-D')}$	$D_b = \min(D_{J\min}, D_{H2}, D_{R2})$
	Case B2.3 $D_{H2} < D_{H1} < 0.5$	-	-	-

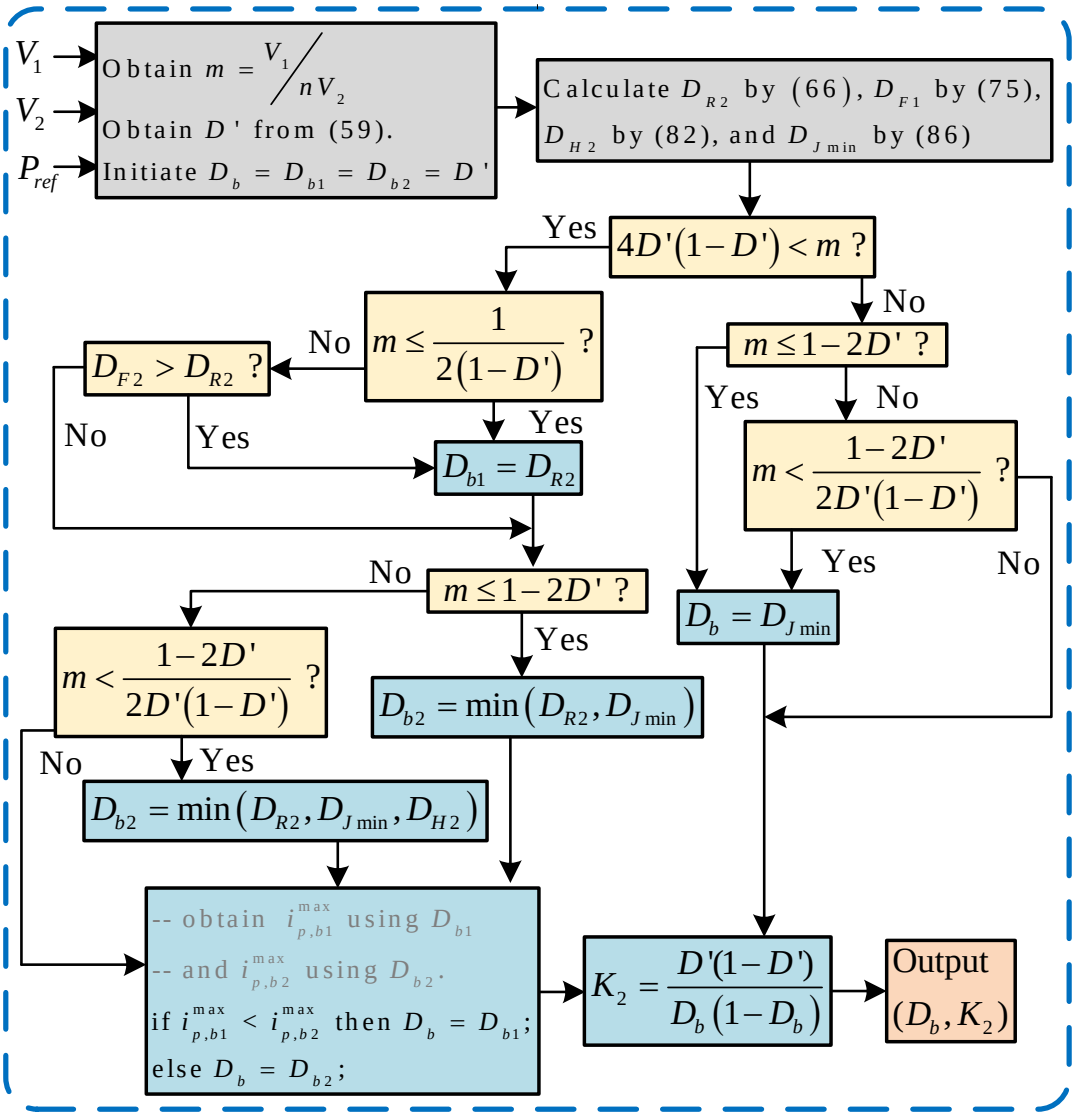


Fig. 36. Flowchart for implementation of the PSAR control

3.4. HIL Experimental Results and Discussion

Different case studies are performed based on TI TMS320F28377S to verify the effectiveness of the PSAR control applied in cases mentioned earlier. For stable operation of the IMMDC, it is essential to control the voltage balancing of the SM's floating capacitors. To do so, the phase-shifted averaging-control method proposed in [28] is combined with phase-disposition

level shifted PWM and sort and select algorithm for voltage balancing of IMMCDC. The reference voltage of the SM capacitors in the primary leg $V_C^{ref,p}$ and secondary leg $V_C^{ref,s}$ are defined as

$$V_C^{ref,p} = V_1 / k \tag{90}$$

$$V_C^{ref,s} = V_2 / j \tag{91}$$

where *j* and *k* are number of SMs in each arm of the MMCs in primary and secondary leg; respectively. Without losing generality, the *j* and *k* are set to 5 in the case studies. The different cases mentioned in Table V are investigated using experimental hardware-in-the-loop setup in following.

1. *Case B1.1*

In this case, the voltages of the DC networks and the transmitted power are set as $V_1 = 4$ kV , $V_2 = 10$ kV , and $P' = 2.1$ MW ; accordingly. This will result in $D' = 0.05$ using (59). It can be seen that point $(m, D') = (0.4, 0.05)$ will fall in the Case B1.1 in Fig. 33(a). Hence, by selecting D from region (0.13, 0.5) and associated K_2 from (64) and inserting them in (47) and (48), the PSAR control would result in an $i_P^{\max}$ less than $i'^{\max}_P$.

The reference voltage for capacitors of MMCs in primary side and secondary side are 800V and 2 kV using (90) and (91); respectively. Fig. 37(a) and Fig. 37 (b) show the SM capacitor voltages of primary left leg under SPS control with $D' = 0.05$ as an example case. It can be seen

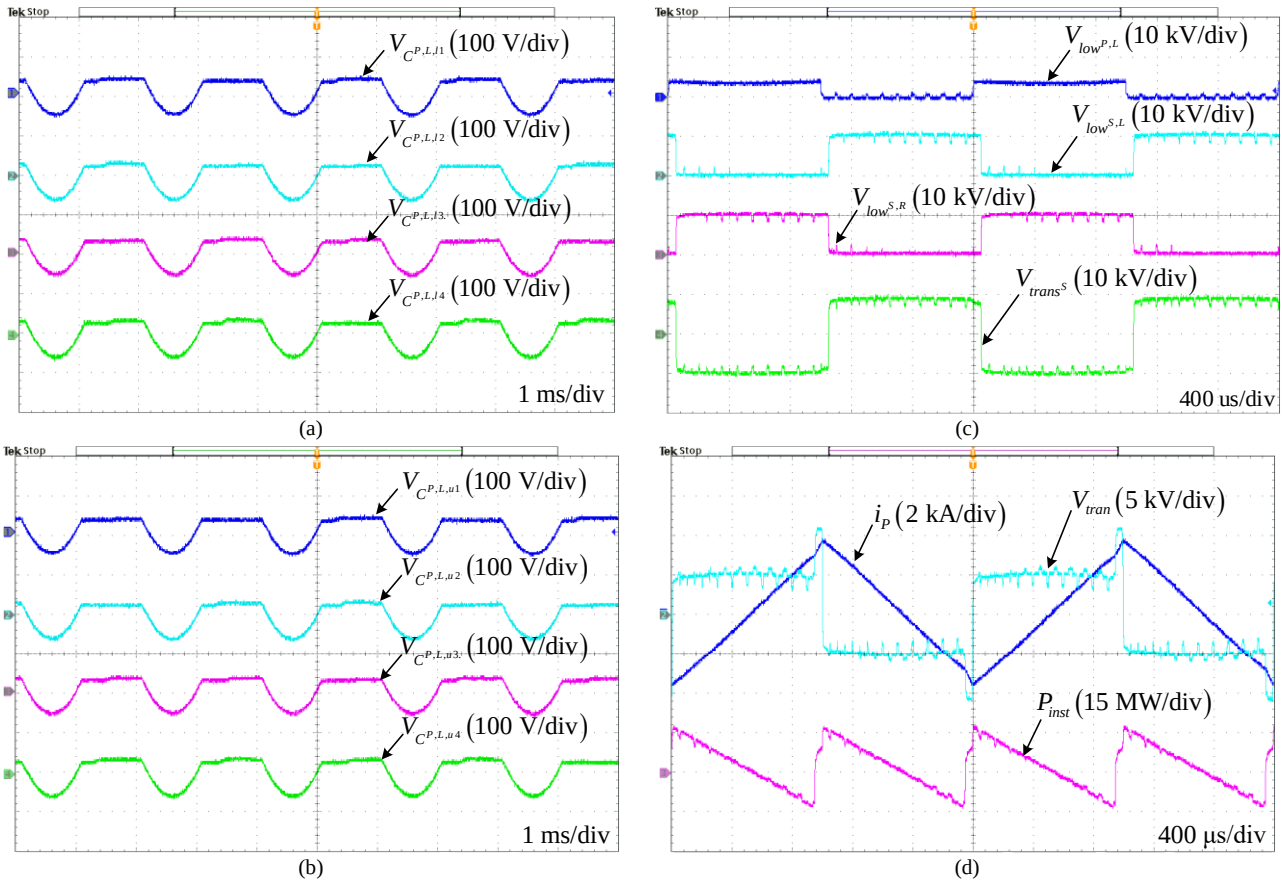


Fig. 37. Experimental HIL results for case B1.1 under SPS control (a) Capacitor voltages of the SM in lower arm of the primary left leg (b) Capacitor voltages of the SM in upper arm of the primary left leg (c) Arm voltage references and transformer secondary voltage (d) Voltage drop on transformer leakage inductance, transformer primary current, and instantaneous transmitted power.

from Fig. 37 (a) and Fig. 37 (b) that capacitor voltage can follow their reference value with acceptable range of around 100 V. SM capacitors of other legs also follow the reference voltage. Fig. 37 (c) shows the $V_{low^{P,L}}$, $V_{low^{S,L}}$, $V_{low^{S,R}}$ and $V_{trans^{S}}$ with the phase shift $D' = 0.05$ between $V_{low^{P,L}}$ and $V_{low^{S,L}}$. As under SPS control K_2 is set to unity, $V_{low^{S,L}}$ and $V_{low^{S,R}}$ vary from 0 to 10 kV according to (47) and (48). Fig. 37 (d) shows the voltage drop on transformer leakage inductance V_{tran}, transformer primary current i_P, and instantaneous transmitted power P_{inst}. It must be noted V_{tran} is

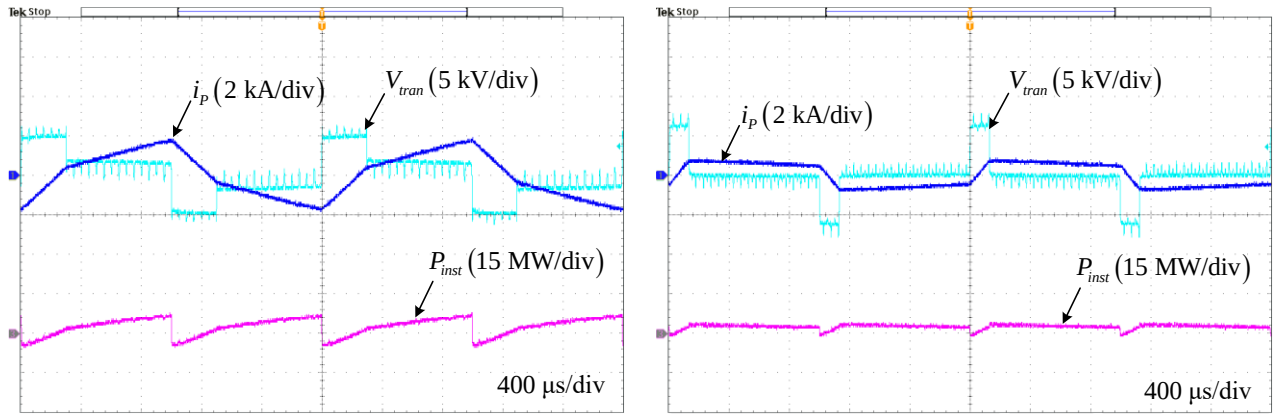


Fig. 38. Experimental HIL results for Case B1.1 under PSAR control. Voltage drop on transformer leakage inductance, transformer primary current, and instantaneous transmitted power for (a) $D = 0.3$ (b) $D_b = D_{R2} = 0.13$

equal to $V_{trans^P} - nV_{trans^S}$ .It can be seen that the instantaneous power frequency is double of the transformer frequency. The current stress is around 3685 A which is close to analytical value of 3555 A.

Fig. 38(a) and Fig. 38 (b) show the waveforms V_{tran}, i_P and P_{inst} of the same circuit under PSAR control with two different $D = 0.3$ and $D_b = D_{R2} = 0.13$ for the same transmission power of 2.1 MW. It can be seen in both cases the current stress is reduced compared to SPS control. The active power, which is obtained by averaging instantaneous power over its period of 0.001 s, is equal to 2 MW in both cases and is close to the analytical value of 2.1 MW.

2. *Case B1.2*

In this case, the voltages of the DC networks are considered as $V_1 = 8$ kV and $V_2 = 10$ kV .

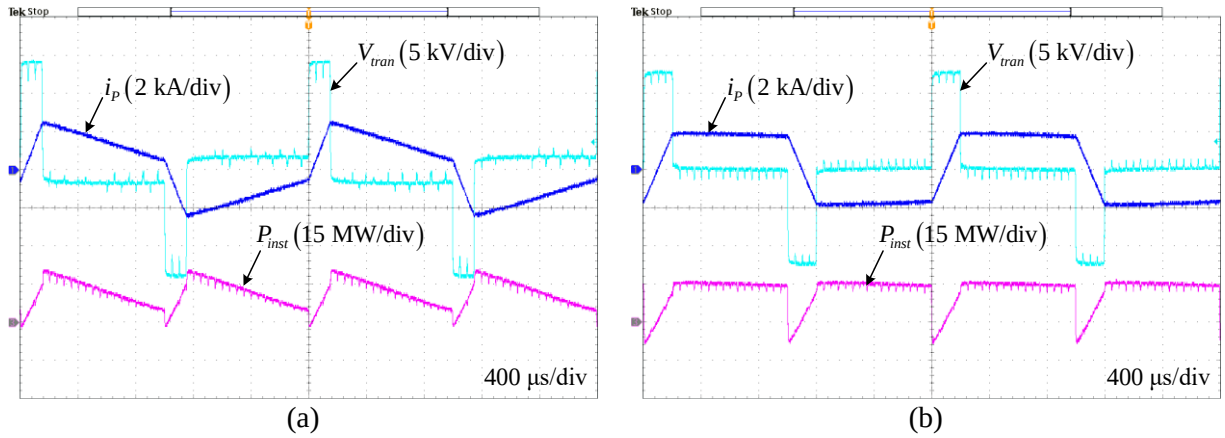


Fig. 39. Experimental HIL results for Case B1.2 under PSAR control. Voltage drop on transformer leakage inductance, transformer primary current, and instantaneous transmitted power for (a) $D'=0.15$ (b) $D_b = D_{R2} = 0.2$

In addition, the power to be delivered is set as 11.3 MW, which will result in $D'=0.15$ using (59). It can be seen that point $(m, D') = (0.8, 0.15)$ will fall in the Case B1.2. Hence, by selecting D from region (0.2, 0.24) and associated K_2 from (64), the PSAR control would result in an $i_P^{\max}$ less than $i_P'^{\max}$. It must be noted least current stress will be obtained by setting $D = D_{R2} = 0.2$.

Fig. 39 shows V_{tran}, i_P and P_{inst}. Fig. 39 (a) shows the waveforms in SPS control with $D'=0.15$, and Fig. 39 (b) shows the waveforms in PSAR control $D=0.2$ for the same transmission power. The value of current stress in SPS control from analytic and experiment is equal to 2444 A and 2456 A; respectively, while these values in PSAR control are equal to 1769 A and 1640 A; respectively. It can be seen that current stress in PSAR is reduced compared to SPS control.

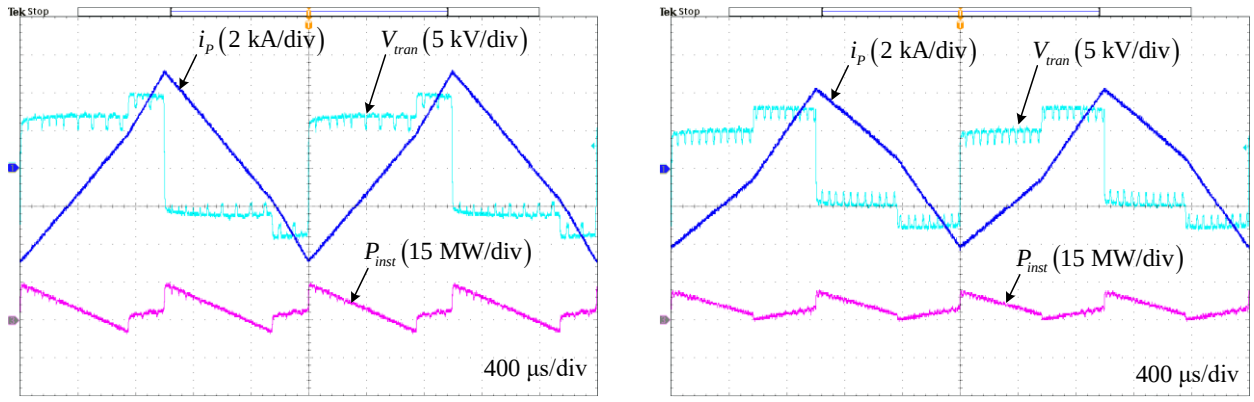


Fig. 40. Experimental HIL results for Region 1 of Case B2.1 under PSAR control. Voltage drop on transformer leakage inductance, transformer primary current, and instantaneous transmitted power for (a) $D' = 0.25$ (b) $D = D_{J\min} = 0.435$

3. Region 1 of Case B2.1

In this case, the voltages of the DC networks are considered as $V_1 = 2$ kV and $V_2 = 10$ kV. In addition, the power to be delivered is set as 4.1 MW, which will result in $D' = 0.25$ using (59). It can be seen that point $(m, D') = (0.2, 0.25)$ will fall in the region 1 of Case B2.1 following implementation of Fig. 36. Hence, by selecting D from region (0.25, 0.5) and associated K_2 from (64), the PSAR control would result in an $i_P^{\max}$ less than $i_P'^{\max}$. It must be noted least current stress will be obtained by setting $D = D_{J\min} = 0.435$.

Fig. 40(a) shows the waveforms in SPS control with $D' = 0.25$, and Fig. 40(b) shows the waveforms in PSAR control $D = 0.435$ for the same transmission power. The value of current stress in SPS control from analytic and experiment is equal to 5000 A and 5020 A; respectively, while these values in PSAR control are equal to 4094 A and 4210 A; respectively.

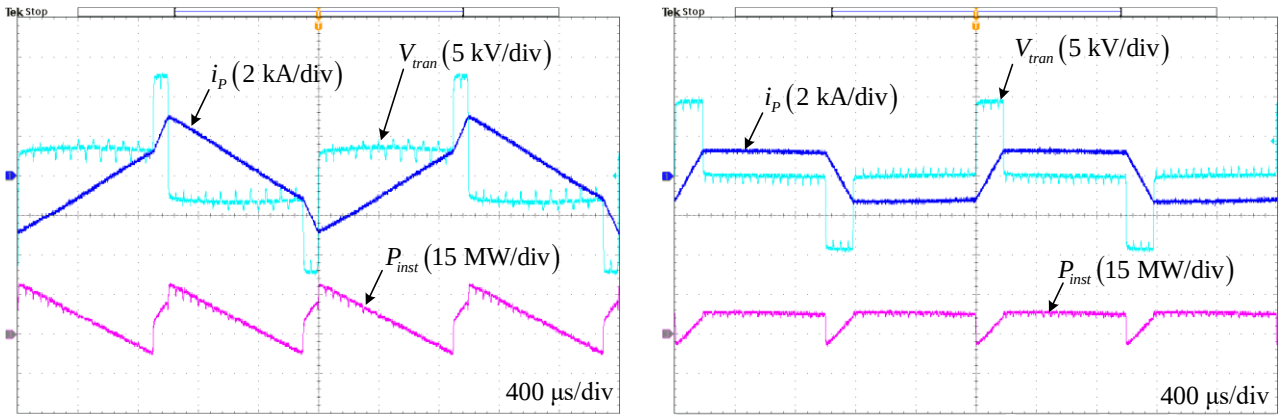


Fig. 41. Experimental HIL results for Region 2 of Case B2.1 under PSAR control. Voltage drop on transformer leakage inductance, transformer primary current, and instantaneous transmitted power for (a) $D' = 0.1$ (b) $D = D_{R2} = 0.184$

4. Region 2 of Case B2.1

In this case, the voltages of the DC networks are considered as $V_1 = 6$ kV and $V_2 = 10$ kV. Also, the power to be delivered is set as 6 MW, which will result in $D' = 0.1$ using (59). It can be seen that point $(m, D') = (0.6, 0.1)$ will fall in the region 2 of Case B2.1 in Fig. 35(a). Hence, by selecting D from region (0.1, 0.184) and associated K_2 from (64), the PSAR control would result in an $i_P^{\max}$ less than $i_P'^{\max}$. It must be noted least current stress will be obtained by setting $D = D_{R2} = 0.184$.

Fig. 41(a) shows the waveforms in SPS control with $D' = 0.1$, and Fig. 41(b) shows the waveforms in PSAR control $D = 0.184$ for the same transmission power. The value of current stress in SPS control from analytic and experiment is equal to 2888 A and 2945 A; respectively, while these values in PSAR control are equal to 1225 A and 1282 A; respectively.

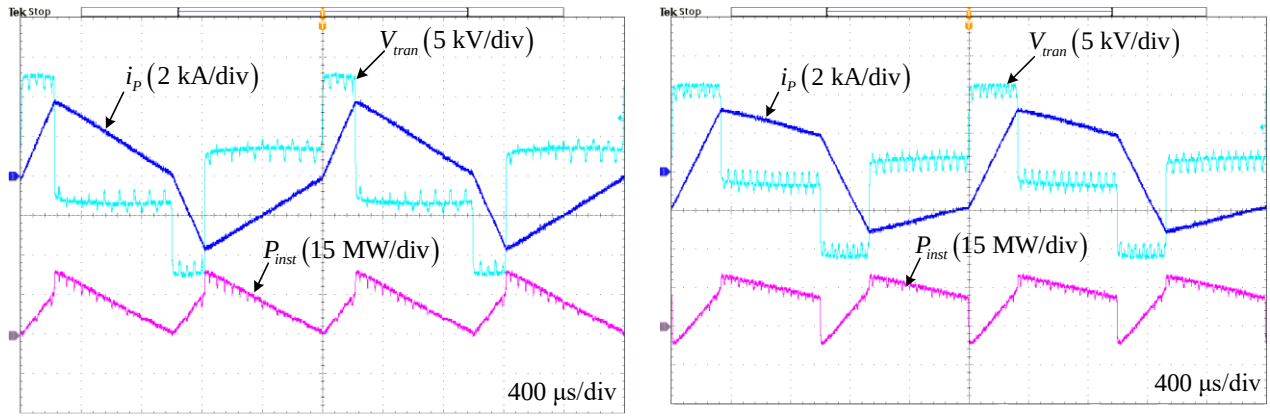


Fig. 42. Experimental HIL results for Region 1 of Case B2.2 under PSAR control. Voltage drop on transformer leakage inductance, transformer primary current, and instantaneous transmitted power for (a) $D' = 0.22$ (b) $D = D_{J\min} = 0.33$

5. Region 1 of Case B2.2

In this case, the voltages of the DC networks are considered as $V_1 = 6$ kV and $V_2 = 10$ kV. Also, the power to be delivered is set as 11.4 MW, which will result in $D' = 0.22$ using (59). It can be seen that point $(m, D') = (0.6, 0.22)$ will fall in the region 1 of Case B2.2 in Fig. 35(b). Hence, by selecting D from region (0.22, 0.48) and associated K_2 from (64), the PSAR control would result in an $i_P^{\max}$ less than $i_P'^{\max}$. It must be noted least current stress will be obtained by setting $D = D_{J\min} = 0.33$.

Fig. 42(a) shows the waveforms in SPS control with $D' = 0.22$, and Fig. 42(b) shows the waveforms in PSAR control $D = 0.33$ for the same transmission power. The value of current stress in SPS control from analytic and experiment is equal to 3688 A and 3720 A; respectively, while these values in PSAR control are equal to 3192 A and 3145 A; respectively.

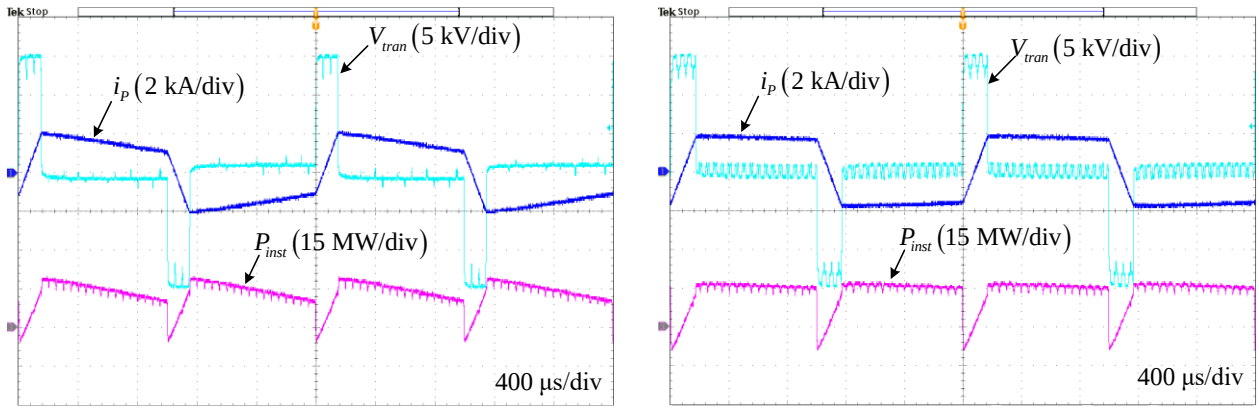


Fig. 43. Experimental HIL results for Region 2 of Case B2.2 under PSAR control. Voltage drop on transformer leakage inductance, transformer primary current, and instantaneous transmitted power for (a) $D' = 0.15$ (b) $D = D_{R2} = 0.17$

6. Region 2 of Case B2.2

In this case, the voltages of the DC networks are considered as $V_1 = 9$ kV and $V_2 = 10$ kV. Also, the power to be delivered is set as 12.7 MW, which will result in $D' = 0.15$ using (59). It can be seen that point $(m, D') = (0.9, 0.15)$ will fall in the region 2 of Case B2.2 in Fig. 35(b). Hence, by selecting D from region (0.15, 0.17) and associated K_2 from (64), the PSAR control would result in an $i_P^{\max}$ less than $i_P'^{\max}$. It must be noted least current stress will be obtained by setting $D = D_{R2} = 0.17$.

Fig. 43(a) shows the waveforms in SPS control with $D' = 0.15$, and Fig. 43(b) shows the waveforms in PSAR control $D = 0.17$ for the same transmission power. The value of current stress in SPS control from analytic and experiment is equal to 2055 A and 2050 A; respectively, while these values in PSAR control are equal to 1709 A and 1780 A; respectively.

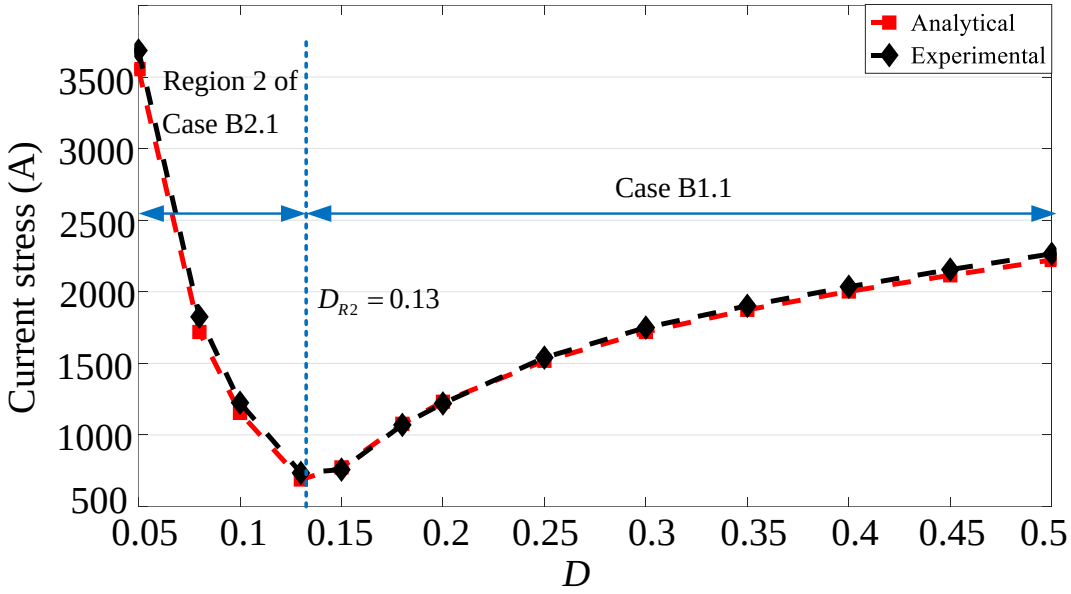


Fig. 44. Least current stress by changing D from 0.05 to 0.5.

It had been mentioned earlier that there could be pair of m and D' that be common in case B1 and case B2. For example the $(m, D') = (0.4, 0.05)$ falls both in case B1.1 and Region 2 of case B2.1. For case B1.1 the least current stress is at $D_b = D_{R2} = 0.13$ according to Table V. For Region 2 of case B2.1, the least current stress is at $D_b = \min(D_{\text{J min}}, D_{R2})$. Since in this case $D_{\text{J min}} = 0.23$, then the least current will also be at $D_b = D_{R2} = 0.13$ for Region 2 of case B2.1. Therefore considering the operation at both cases, the final best operating point is $D_b = D_{R2} = 0.13$. This result has also been investigated by selecting D from $(D', 0.5) = (0.05, 0.5)$ and setting associated K_2 from (64). The obtained result of current stress by changing D from 0.05 to 0.5 has been plotted in Fig. 44. It can be seen that least current stress happens around $D = 0.13$

Chapter IV: Conclusion and Future Work

The first part of this work presented a new medium-voltage high-power MMC topology to generate multilevel output voltages. The proposed TOMMC-based inverter can produce the same number of output voltage levels as a conventional MMC but with significantly lower SM count. It was shown that for generating output voltage of -12 kV to +12 kV with steps of 1000 V, there is a need for 24 SMs in a conventional MMC with two DC sources of 12 kV each. This will require 48 high-frequency switches with related gate drivers and protection circuitry, and 24 capacitors and corresponding voltage measurements. The proposed topology requires 9 SMs with 18 high frequency switches and 4 low frequency switches, 9 capacitors, and one 12 kV DC-source to generate the same voltage. In addition, a new modified carrier deposition PWM technique with SM capacitor voltage balancing was proposed that will result in even distribution of voltage ripple along the capacitors of different SMs in each arm. Also, the unequal DCPs of the carrier disposition techniques will be avoided which results in uniform power and heat distribution in each arm of the MMC. It had also been shown that under same output voltage and same load, the current stress of the high frequency switches of the proposed TOMMC is less than conventional MMC. Lower current stress for high frequency power switches will prolong the lifetime of employed high-frequency switches.

Comparative loss analysis of the conventional MMC and the proposed multilevel converter are carried out under different power factors and modulation indexes. The result illustrates the lower conduction loss and switching loss of proposed TOMMC. The conduction loss is reduced by around 10% to 20% in the proposed TOMMC compared to conventional MMC, and the switching loss has been reduced by around 40% to over 50%. The proposed TOMMC has lower total loss under all different studied power factors and modulation indexes.

Due to higher number of power switches in multilevel converters compared to two-level converters, it is an interesting topic to study the fault tolerance operation of multilevel converter. Study of fault tolerance methods for proposed TOMMC was not the focus of this dissertation, but is suggested as an interesting topic for future works.

The final part of this work proposes PSAR control method in IMMDC. IMMDC is a key component in HVDC and MVDC grids to realize power transfer and voltage matching between DC buses. SPS control is conventionally used as a control method in IMMDC converter that suffers from high current stress. Although PSAR has the same maximum power transfer capability, but it has been shown to offer wider power regulation range which helps to operate at points with less current stress but same transmission power level. Less current stress operation of MFT and power switches prolongs the lifetime of the converter. An algorithm had been also developed to operate for simple implementation of PSAR control method.

In the presented work, the idea of considering the modulation ratio indexes of the secondary side of the transformer as an extra control variable and the effect on current stress has been studied. For future work, the effect of modulation index ratio on soft switching of the IMMDC is a very interesting topic.

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