Fabrication and Manipulation of Metallic Nanofeatures and CVD Graphene through Nanopatterning and Templating

by

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Christina M. Edwards

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Abstract

Nanotechnology holds exciting potential to significantly advance research in many fields such as sensors, environmental sustainability and cleanup, energy harvesting and storage, as well as nanoelectronics. The resulting high demand for implementation into these areas has simultaneously created a large need for effective fabrication methods for nanostructured materials. It is important the fabrication methods are capable of significant control over size, orientation, and structural configuration of nanomaterials for effective function in these applications. Nanopatterning and templating are a promising means to achieve extreme selectivity over these parameters, and additionally be used as tools to control the growth and structure of large-scale materials through nanoscale manipulation. In this research, nanopatterning and templating are implemented to create metallic nanowire structures on surfaces of silicon substrates with highly selectivity over nanowire placement and design. Additionally, templating is incorporated in graphene growth on metallic substrates to influence the quality of graphene films,and further film patterning is used to improve the graphene electrical and optical properties.

The first part of this work focuses on the fabrication of copper metallic nanowires through resist patterning coupled with electroless copper deposition. An atomic force microscope is used to selectively remove portions of a self-assembled monolayer resist on a silicon substrate, with patterns reaching down to widths of 20 nm. Electroless metal plating provides a facile way to deposit metal in selectively activated areas on surfaces with nanoscale dimensions. Here, it is employed to deposit copper selectively within these nanopatterned lines to create copper nanowire features. Through variation of the electroless metal solution conditions, the dimensions of the AFM-patterned line, and the

doping of the underlying silicon substrate, the dimensions and uniformity of copper deposition within AFM-patterned lines can be influenced. Furthermore, this method provides a successful level of control to construct copper nanowire features between gold microelectrodes, which allows the electrical properties of these nanowires to be examined. The ability to selectively place nanowire features on a substrate surface with dimensions down to the tens of nanometers, as well as the capability to manipulate the nanowire size and uniformity, make this a promising method to construct metallic nanofeatures for complex nanodevices and circuitry.

The second portion of this research investigates techniques to develop high quality graphene films produced by chemical vapor deposition (CVD) on copper substrates. Chemical vapor deposition shows great potential for developing graphene films of large area, but unfortunately CVD graphene oftentimes possesses low conductivity values due to an increased amount of misaligned grain boundaries and point defects, and oftentimes exhibits low optical transparency. The focus of this research is to better understand the role the copper substrate plays in CVD graphene formation, and to find ways to directly enhance CVD graphene quality through changes in the copper substrate template. The surface morphology, optical transmittance, and electrical properties of CVD graphene manufactured on two copper substrates with different surface structures were investigated. It was found that differences in the copper substrate grain alignment and crystal lattice could significantly influence the deposition and quality of graphene on copper substrates. Furthermore, the possibility of developing graphene films on nonmetallic substrates, as well as enhancing its properties through chemical doping, is demonstrated by nanopatterning and templating of graphene films.

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Chapter 1: Introduction

1.1 Background

Nanotechnology has been a rapidly growing field for the past three decades, and consequently there has been a great demand for fabrication and manipulation of materials at the nanoscale. Development of new production methods as well as techniques to controllably influence properties and structure on the nanoscale is paramount, considering most material properties are different at the nanoscale when compared to their larger counterparts. The major contributors to differences in material properties at the nanoscale are the emerging importance of quantum confinement effects and greatly increased surface area to volume ratio. For this purpose, a vast amount of research has been focused on topics such as the properties of nanostructured materials, the role of nanostructure on interface properties, chemistry at the interfaces of nanostructured materials, and patterning and templating for controllable nanoscale growth. A reduction in the dimensions of materials towards the nanoscale limit can effect several properties of materials such as their melting point,[1] electrical conductivity,[2] thermoelectric property,[3] fluorescence,[2] magnetic permeability,[4] plasticity,[5] and a host of other characteristics. Researchers may utilize these changes in behavior at the nanoscale to tune the properties of materials for improved photonic and electronic devices,[6] cancer diagnosis and therapy,[7,8] power generation and cooling technologies,[9] cellular adhesion and manipulation,[10] and even improved insulation for clothing and homes.[11,12] In addition, the nanoscale structure at interfaces has a significant impact on the properties of materials specifically at their surface. For instance, the hydrophobicity of materials can be enhanced with nanoscale roughening or patterning of a surface, which is promising in the

industrial area of self-cleaning materials and antioxidant surfaces as well as in microfluidics to decrease drag.[13] Changes in the surface nanostructure may considerably impact wettability, friction, and wear that can be used for practical benefits in the realm of industry such as improved lubrication or packaging material. They also can be applied in the biomedical field for cellular manipulation and reduced fouling of medical implants.[14,15] A nanostructured surface topography is clearly capable of influencing interface properties, but can further influence the chemistry at the surface interface as well. For example, gold with a nanoporous structure demonstrates a different chemical reactivity in comparison to bulk gold,[16] and nanostructured surfaces have been widely used to enhance the chemical reactivity in catalysis applications.[17] In order to manufacture well-defined nanostructured materials, or control bulk material growth by nanoscale manipulation, a high degree of control on size, shape, and orientation is necessary. Nanopatterning and nanotemplating are promising means to achieve these requirements. Nanopatterning with a scanning optical microscope has allowed for the creation of complex patterns within self-assembled monolayers,[18] for instance, and boron nitride with structured orientation has been grown from nanoscale graphene templates.[19] From all these considerations, it is evident the properties of materials change when reduceddown to the nanoscale dimensions, and the capability to manufacture materials at this scale requires a heightened control of spatial dimensions.

Some of the most common areas which benefit immensely from nanotechnology advances are lab-on-a-chip (LOC) devices, sensing, environmental applications, energy, and nanoelectronics. Lab-on-a-chip devices involve synthesis and analysis of chemicals on a miniaturized scale within a portable device. There is a profound interest in

transitioning from the current implementation of microfluidics for LOC devices to smaller scale nanofluidics.[20] In order to do so, fabrication of nanoscale components is imperative. Recent work has shown manufacture of nanochannels[21] and nanosensors[22] for incorporation into LOC devices, but the field of nanofluidics is still relatively new, and a great potential remains for nanostructure implementation into LOC devices to improve their routine processing, as well as adding new functionality into current microfluidic devices.[20] The production of nanosensors for LOC incorporation is only one example of how nanotechnology can provide improved sensing. It also possesses broad applications in bio-sensing,[23] electrochemical sensing,[24] single molecule sensing,[25] and magnetic sensing.[26] Many of these applications utilize the heightened surface area to volume ratios of nanostructured material for signal enhancement and sensitivity. Nanosensors for electrochemical detection exhibit enhanced signal to noise ratios,[27] and limits of detection can reach down into the nanomolar and single molecule range with the occurrence of the plasmon resonance phenomenon at the surface on gold nanorods.[25,28]

The increased surface area to volume ratio on nanostructured material not only has positive benefits for sensing applications, but also for fundamental application in environmental chemistry. As mentioned in the previous paragraph, nanomaterials can be implemented for sensing, which includes detection of harmful or toxic substances in the environmental sector. Newly developed nanomaterials show potential for improved detection of such analytes as trace heavy metals (Hg(II), Cr(VI), Cd(II), As(III), As(V), Pb(II), etc.) in food and surface water,[29,30] environmentally hazardous gases (NO_2, H_2S, CH_4, SO_2, CO_2, etc.),[31] and persistent organic pollutants (pentachlorophenol (PCP), trinitrotoluene (TNT), polychlorinated biphenyls (PCB), etc.).[30,32] In addition to

detection, materials with nanoscale features may be used to clean the environment of these hazardous materials. Nanostructured catalytic membranes, nanosorbents, nanocatalysts, and bioactive nanoparticles have all been implemented for environmental treatment, purification, and disinfection.[33] All these substances described thus far have been limited to detection and purification of chemical species, but nanotechnology has implications in the biological realm of the environment as well, such as monitoring ecosystem health with biosensors.[34,35] Due to these possible detrimental effects nanotechnology may play on the environment and living organisms, there has also been great focus on green chemistry nanotechnology for use in environmental and biological systems by creating more biocompatible nanomaterials and developing new synthesis pathways to reduce hazardous waste production.[36,37]

Closely related to the idea of sustainability for nanotechnology in environmental applications, nanomaterials have shown great promise in the area of renewable energy sources. As of 2007, about 80% of global energy consumption was powered by chemical energy stored in fossil fuels, and according to the US Department of Energy, the energy demand is expected to increase by 71% from 2003 to 2030.[38] Consequently, the demand for alternative energy sources and energy storage devices is paramount. Nanoscale materials have demonstrated enhanced energy harvesting and storage in devices including solar cells, fuel cells, and batteries.

A solar cell is an electronic device that converts solar energy into electrical energy via the photovoltaic effect. It utilizes the excitation of an electron in a semiconductor material by light photons, with subsequent creation and splitting of an electron-hole pair, to induce a current between two electrodes. Significant photon

absorption at the correct bandgap energy for electron excitation is crucial for electron-hole production. If a photon of too little or too high of energy contacts the solar cell surface, the light will either pass through the material without being absorbed, or be lost as heat. Furthermore, it is imperative for current production for the electron to travel toward the cathode and the hole toward the anode for current generation, but oftentimes, the electron-hole pair recombine before traveling to their respective electrode surfaces. Nanotechnology provides a promising means to overcome these limitations by increasing the effective optical path for absorption due to reflections of light on the nanoscale surface, creating shorter path lengths for electrons and holes to travel, and providing band gap tunability of the semiconductor by size of the nanostructured material.[39] Gold nanomesh implemented into an organic solar cell has been shown to only reflect 4% of incident light, absorbing 96%, leading to an overall efficiency in converting light to energy at a value 52% higher than its conventional counterpart.[40] Other morphologies that have been explored for use in solar cells have included titania nanorods and nanoflowers,[41] ZnO nanoneedle arrays,[42] silicon nanopore and nanowire arrays,[43] and many more.[44,45]

Similar to solar cells, fuel cells and batteries convert chemical energy into electrical energy. Fuel cells are highly dependent on chemical reduction and oxidation reactions at electrode surfaces, and thus catalysts are commonly incorporated into electrodes for increased reactivity. Currently, platinum is the dominant material used for fuel cells due to its superior catalytic capabilities, and is commonly deposited as nanoparticles on nanostructured foundations such as carbon nanotubes[46] and nanoporous gold[47] to increase the available electrode surface area for oxidation and reduction, which

raises reaction rate. However, other nanomaterials with high catalytic behavior are also being explored such as edge-halogenated graphene platelets[48] and graphene coated with cobalt nanoparticles.[49] Nanostructured materials provide benefits in batteries as well, such as increasing available power, decreasing charging time, and improving the shelf life. Silicon-coated nanotubes have been used as anodes in lithium-ion batteries and exhibit energy capacities up to 10 times that of conventional ion batteries.[50] Additional silicon structures, such as silicon nanowires[51] and silicon nanoparticles,[52] are employed in lithium ion batteries to prevent cracking which is normally experienced in Li^+ batteries composed of bulk silicon. The silicon nanostructures can significantly increase battery lifetime and reduce charging time to within 10 minutes.

In the area of electronics, there is a drive to create devices of ever-decreasing dimensions,[53] leading to the field of nanoelectronics. By creating electronic components of smaller size, it is possible to manufacture electronic devices with reduced weight and power consumption. Advantages of nanoscale electronics are not only limited to size reduction, but also low cost, ease of production with the advent of self-assembly, and potentially improved intrinsic properties compared to microscale electronics devices resulting from improved system integration.[54,55,56] These benefits may have implications in the scientific realm in addition to the world of industry, permitting the construction of devices with more computing power for intricate computational studies. Coupled with nanoelectronics, nano-robotics is an emerging field involving fabrication of robotics components in the size range of 1- 100 nm. Even though most of the work in this area remains theoretical for man-made devices, nature's biological nanorobotic systems are the basis for current research involving drug delivery in medicinal chemistry.[57] The trend

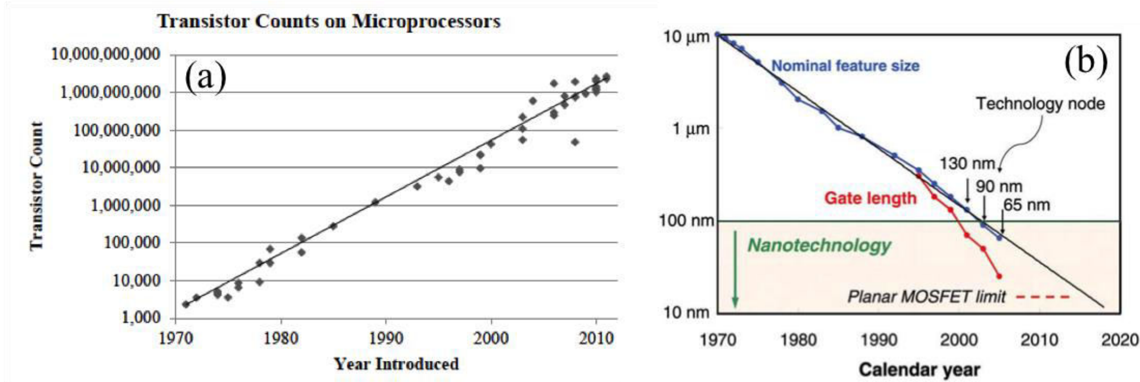

Figure 1.1. (a) Log scale plot of transistor count vs. date of introduction for commercially available microprocessors. Graph adapted from Reference 34. (b) Logic technology node and transistor gate length versus calendar year. Note mainstream Si technology is nanotechnology. (Published at the International Electron Devices Meeting.)

in rapid miniaturization of electronic components for nanoelectronic and nanorobotics applications is observed in Figure 1.1. Clearly, there has been a constant push to increase transistor counts in microprocessors over the past three decades by the slope of the line in Figure 1.1-a.[58] This has led to an additional drive to decrease transistor gate length size as apparent in Figure 1.1-b.[59]

Unfortunately, the fundamental limit on transistor size is rapidly approaching, due in part to the limitation of current fabrication methods, but primarily problems experienced by transistors at small gate lengths.[59,60] Modern lithography techniques can produce silicon transistors with sizes near 30 nm in high volume production at fairly cheap processing costs,[59,61] which keeps them as the predominant choice for current nanotechnology technologies. Additionally, with recent advances in nanoscale fabrication, it is highly probable in the near future to manufacture silicon transistors smaller than 30 nm. However, transistor gate lengths that are lower than tens of nanometers do experience significant current leakage due to tunneling, power consumption, and problems with heat dissipation. Present day transistors can experience

a 20-30% leakage of dissipated power.[59] As a result, other nanoscale materials with superior mobilities and thermoconductivities that show great potential to replace silicon are being extensively explored, such as germanium[62], silicon alloys,[63] alloys of Group III-V elements,[64] and graphene nanoribbons or carbon nanotubes.[65]

Clearly, nanostructured materials provide wide-spread benefits in the areas of lab-on-a-chip devices, sensing, environmental sustainability and cleanup, energy, and nanoelectronics. For effective implementation of nanostructures into these applications, however, it is imperative to develop new methods for precise control and manipulation over the size, shape, and orientation of materials at the nanoscale. Two promising means to achieve these requirements are nanopatterning and templating. These two techniques are the basis for the two major projects described in this thesis: the fabrication of surface-attached metallic nanofeatures, and the controlled growth and manipulation of graphene films, as described below.

1.2 Fabrication of Metallic Nanowire Features

Nanowires have been the basis for advancements in several technologies such as sensing,[66,67] solar cells,[68] batteries,[51] and nanoelectronics[69] as described above, but they also provides benefits in the areas of transparent electrodes,[70] biomedical delivery,[71] and biological cell manipulation.[72] Most of these applications require the bulk production of nanowires in solution, or the formulation of large nanowire arrays from structured templates. However, for progress in the area of nanoelectronics and nanorobotics, it is essential to be able to study a single nanocircuit or nanodevice systems for prototyping prior to large-scale production. To accomplish this objective, it is necessary to

manufacture single metallic features on surfaces with highly controllable placement and design to act as interconnects between nanocapacitor and nanotransistor components, or as the nanoscale components themselves. Therefore, a simple and flexible method to manufacture nanoscale metallic features of varying shape, size, and arrangement is desirable for investigations involving a variety of electronic nanodevices with a range of dimensions and configurations. One such device among many that could be envisioned is a bionanodevice comprised of the molecular rotor, ATP synthase. This device requires extensive control over metallic feature location and size, and which is the focus for future application of the research described here. The following sections briefly describe this device, as well as methods for fabrication of metallic nanowire features on surfaces including photolithography, electron beam lithography, nano-imprint lithography, dip-pen lithography, oxidative lithography, and nanopatterning and grafting. These methods are additionally described in Chapter 4.

1.2.1 ATP Synthase Nanobiodevice

ATP synthase is a membrane-bound protein that plays a key role in the energy metabolic pathway of most organisms by converting adenosine diphosphate (ADP) to adenosine triphosphate (ATP) through a phosphorylation reaction. It consists of the membrane-embedded hydrophobic F_0 portion, and a hydrophilic F_1 portion that protrudes out of the membrane. The F_0 portion consists of 3 subunits labeled a, b, and c, and the catalytic F_1 portion is composed of 3 α subunits, 3 β subunits, and one γ subunits.[73] The three α and three β subunits are organized in a barrel-like hexamer arrangement of alternating α and β sections, with the long rod-like γ subunit located partially within the hexamer structure and partially protruding out of the hexamer. In order to synthesize

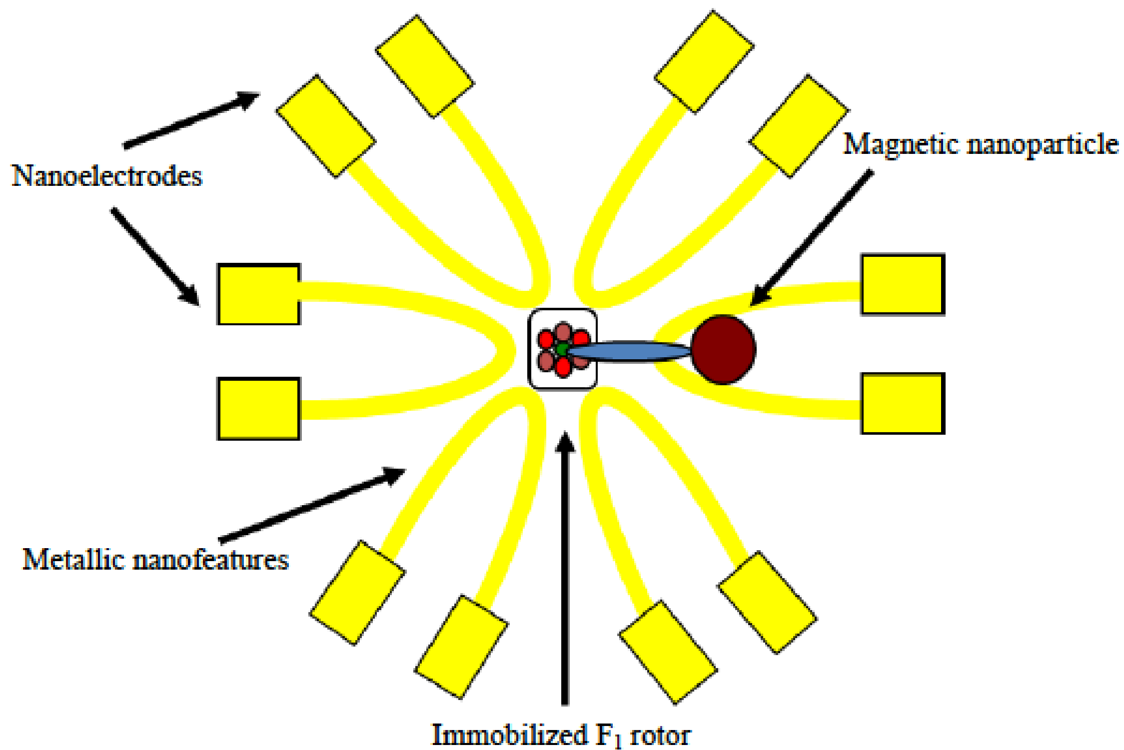

Figure 1.2. Schematic of nanobiodevice with immobilized F_1 portion of ATP-synthase surrounded by metallic nanofeatures connected to nanoelectrodes.

ATP, the central γ subunit rotates inducing conformational changes in active sites on the α and β hexamer to drive ATP synthesis. When the F_1 portion is separated from the F_0 counterpart, it will rotate in the opposite direction to convert ATP to ADP and phosphate. The specific details regarding the stepwise rotation of the γ subunit still remain unclear,[74] and therefore methods to adequately characterize its function are desired. Furthermore, if the rotation of the F_1-ATP synthase can be well-understood and characterized, it may potentially permit future manipulation of the rotation mechanism, and allow the ATP synthase to be used as a motor for hybrid biological-inorganic devices. Its small diameter of 10 nm is favorable for such an application.

A schematic of a potential nanodevice incorporating the F_1 portion of ATP-synthase within a metallic electrode array is depicted in Figure 1.2. In the center of the nanodevice, the F_1 portion of ATP-synthase would be selectively placed in an upright orientation with the γ subunit protruding up from the surface interface. Attached to the apex of the protruding subunit would be an armature, parallel to the surface, that would extend out from the γ subunit, over the α and β hexamer, and into the regions surrounding the surface-bound protein. The long armature would be further terminated with a magnetic bead. In the immediate vicinity around the central ATP-synthase component, there would be a fabricated array of metallic nanofeatures in a circular configuration, which are attached to larger microelectrodes. In the presence of ATP, the γ subunit of the protein would rotate to chemically produce ADP, thereby rotating the connected armature around the central immobilized ATP-synthase, and the magnetic bead over the metallic nanofeatures. As the magnetic bead passes over the individual metallic nanofeatures, a current is induced within the metal nanofeatures which can be measured via the nanoelectrode components.

For this device to be operational, the metallic nanofeatures need to be small enough to fit around the immobilized F_1 portion of ATP-synthase, as well as allow the proper rotation of the armature and magnetic without any hindrance, and make it feasible for the magnetic bead to induce a detectable current in the metallic nanofeatures. In view of the fact that the size of the F_1 portion of ATP-synthase is approximately 10 nm, the metallic nanofeatures could only extend 10 nm or less above the surface, and be in the low 10s of nanometers in width. The objective of this research was to be able to fabricate metallic nanowire features that allow high selectivity of surface location, as well as

control on nanowire dimensions at the tens of nanometers scale. This type of fabrication control and flexibility would not only be beneficial for the construction of the ATP-synthase nanobiodevice as described above, but also for a large variety of other nanoelectronic devices.

1.2.2 Nanofabrication Methods for Surface-Attached Metallic Nanowire Features

Current methods for nanowire production on substrate surfaces include photolithography,[75] electron beam lithography,[76] nano-imprint lithography,[77] dip-pen lithography,[78] oxidative lithography,[79] and nanopatterning[80] and grafting.[81] A majority of these techniques are composed of an initial nanopatterning step of a resist-coated surface with a focused beam, nanotemplate, or probe tip, followed by selective metal deposition in the patterned area. Therefore, for the fabrication of metallic nanowire features using these methods, it is imperative they possess the capability to create patterns down to and lower than the tens of nanometers scale. Additionally, these nanoscale patterns need to be placed in highly selective locations on sample surfaces.

Photolithography has been utilized for decades as a means to manufacture bulk microscale integrated circuits on semiconductor surfaces via patterning with a focused beam of light. Most equipment utilized in photolithography is restricted to patterns on the microscale or hundreds of nanometers due to the diffraction limit of light. However, modern development of sophisticated instrumentation, such as eximer lasers and extreme ultraviolet lithography, have led to fabrication of patterned features with widths down to the tens of nanometers.[61,82] Unfortunately, this instrumentation can be very costly and complex. For example, some systems with an eximer laser can have an objective with up

to 30 purified quartz lenses.[83] Furthermore, more significant advances are needed to in order to approach pattern widths of 10 nm or smaller.

Electron beam lithography is a technique similar to photolithography, but uses a focused beam of electrons to pattern resist-coated materials. Beam sizes have been shown to be able to reach down into single-nanometer sizes, and this technique has been capable of producing patterned lines with widths down to 5-7 nm.[84] However, the exposure of the resist to the electron beam only destabilizes the resist in that region, and a necessary etch step is required to remove the resist from within the patterned area. Previous studies have demonstrated that with lines widths on the order of 5-7 nm produced by electron beam lithography in PMMA resists, it may be difficult to dissolve the destabilized resist.[84] Furthermore, if the electron beam power is not sufficient enough once focused to a few nanometers in size, it will inadequately destabilize the resist coating and be unsuccessful at patterning. Lastly, this method takes place with a vacuum chamber, which may adversely effect sensitive samples.

Nanoimprint lithography utilizes a templated mold or stamp to pattern surfaces on a bulk scale. The stamp is applied to the target surface commonly under increased pressure and temperature, and then removed. Lines with 10 nm widths have been produced within PMMA resists using nanoimprint lithography.[85] Even though line widths of a 10 nm width can be fabricated, there are a few drawbacks to this method for the fabrication of single metallic nanowire fabrication on surfaces. First, placement of the stamp on the substrate surface, and thus the location of patterned regions, is far less controllable as compared to the other fabrication techniques described here. Also, this technique is used to manufacture large arrays of patterns, which can make this method

quite costly for making master template stamps with complex patterns, and limits its flexibility to create a variety of patterns. It is quite inefficient for construction of a complex singular system.

Dip-pen lithography is a technique used to directly write molecules onto the surface of a target substrate via a coated atomic force microscope (AFM) tip. The AFM tip is coated with molecules by either dipping the tip into a solution containing the species or its neat liquid. Upon tip contact onto the substrate surface, a meniscus is formed due to ambient humidity, and the molecules on the coated tip can travel to the substrate surface. The size features that can be obtained with this technique are on the order of tens of nanometers.[86] It is not possible to reach smaller dimensions due to the fact the size of the features is limited by the size of the meniscus, which can be very sensitive to atmospheric conditions and difficult to control. Control of specific nanowire placement on the surface may be difficult as well, considering one cannot image the surface before depositing the molecules onto the surface.

Oxidative lithography is performed by applying a negative potential between an AFM probe tip and sample surface. In the presence of the aqueous environment due to the meniscus formed between the sample and probe tip, the surface becomes oxidized. Oxidized regions can be direct templates for metallic deposition. Researchers have used this technique to form oxidized patterns in monolayers on silicon oxide, and subsequently deposit silver on those features.[87] The patterned line dimensions are also dependent on the size of the meniscus formed between the tip and sample surfaces, and has only reached line widths at the tens of nanometers scale.[88]

Nanopatterning and nanografting use an AFM tip with increased force on the surface to dig out selective areas of a resist-coated surface. In nanopatterning, an AFM tip with a high value of applied force may penetrate through the top layer or a resist coating down into the lower levels of the sample substrate. As the tip scans, it removes the upper regions of the surface, leaving the underlying regions of the substrate exposed. The resulting pattern is thus dependent on the regions where the tip has scanned. If the patterning is performed in the presence of another solution with molecules that can bind to the uncovered substrate regions, this process is known as nanografting. These two techniques are promising for creation of patterned lines down into the single nanometer range considering dimensions are dependent on the AFM tip size, and modern sharpened tips with radius of curvature values of 2-5 nm are commercially available. Even though the beam size of electron beam lithography rivals these sizes, nanopatterning and nanografting provide the advantage of direct removal of a resist coating as opposed to resist destabilization with electron beam lithography, and do not require additional processing steps for nanopattern fabrication. Nanofeatures using these methods have been able to produce widths as low as ten nanometers,[81] and using sharpened tips there is great potential in the near future to further reduce this size.

Nanopatterning and nanografting show a great potential to pattern resist-coated surfaces with single nanometer dimensions and highly selectivity of pattern location and configuration. For this reason, this method was coupled with electroless metal deposition to fabricate copper nanowire features. It is the focus of this research project to utilize these two techniques to develop an easy and versatile method to construct surface-attached metallic nanofeatures with controllable size and surface location.

1.3 Controlled Growth and Manipulation of Graphene Films

In the previous section, the role of controllable nano-patterning for formation of single metallic nanofeatures was discussed. In this section, the role of templating for controllable growth and manipulation of graphene films is described.

Graphene is a one-atom thick layer of sp^2 carbon atoms arranged in a hexagonal lattice, and due to its characteristic structure, it possesses unique properties such as great mechanical robustness,[89] high electron mobility,[90,91,92] transparency,[93,94,95] chemical stability,[95,96] and flexibility to conform to various surface morphologies.[94,97] Consequently, graphene has had widespread applications into the previously described fields of sensors, [98,94,99] solar cells, [100,101] and energy storage devices,[102] as well as memory devices,[103,104] transparent electrodes, [105,106,107] and transistors. [108] Graphene can be developed into several different structures such as sheets, nanoribbons, carbon nanotubes, and fullerenes depending upon the application demand. Graphene nanoribbons and carbon nanotubes, with their small sizes, low resistance, thermal conductivity, and highly tunable band gaps, are prime candidates for nanoelectronics such as tiny transistors[109] and nanoelectronic interconnects.[110] Fullerenes with their small cage-like structure and functionalization potential have been investigated for use in gene and drug delivery in medicinal chemistry,[111] and additionally hydrogen storage for fuel cell applications.[112] Clearly, there has been significant research regarding fabrication and manipulation of micro and nanoscale graphene-like structures. However, the transition to large-scale graphene sheets while retaining its highly favorable properties has proven difficult. The minimum calculated sheet resistance for single-layer graphene is approximately 31 Ω/square,[91] however experimentally observed sheet resistance values

fall within the range of 125 to 10,000 Ω/square,[105,113] with most values falling near the larger value in this range. Values at the lower end of this range oftentimes result from multi-layered graphene, graphene of small area, or retain these values at cost of lowered optical transmittance. Many applications, such as transparent electrodes for solar cells, require optical transparency as well as high conductivity.

Chemical vapor deposition (CVD) is a promising method to produce large-area graphene with high conductivity and optical transparency. Researchers have been able to produce graphene with sheet resistances in the hundreds of Ω/square utilizing chemical vapor deposition, [105,113] but sheets with this high value are limited to transmittance values of around 80%,[105] which is much lower in comparison to values of modern ITO transparent electrodes. Therefore, there has been a push to create not only highly conductive large-area graphene, but produce this graphene with transmittance values that surpass ITO. Some ways accomplish this objective is to gain a better understanding of the CVD graphene deposition mechanism on copper, leading to potential control of graphene formation and its quality on these metallic substrates. The conductivity of graphene is significantly dependent on the presence of graphene boundaries and point defects within its film. Thus, to create films with higher quality, it is important to be able to control the number and alignment of grain boundaries, as well as point defect density.

Researchers have shown that the underlying copper substrate can make a significant difference in graphene quality, with Cu (111) lattice faces producing graphene of higher quality as opposed to CVD graphene on Cu (100) and (110) faces. [114,115] Furthermore, graphene on expensive single-crystal copper surfaces has shown significantly better conductivity as opposed to polycrystalline surfaces, likely due to

increased grain boundaries in the polycrystalline copper. It is for this purpose there is a push to be able to manipulate copper substrate surfaces, which act as templates for graphene growth, on a commercially cheap scale to align grain boundaries, increase grain size, and promote the formation of mostly single-crystalline surface. An additional method to increase graphene conductivity, which has been the focus of much research, is chemical doping.[116,113] Researchers have shown increases in conductivity in several orders of magnitude by chemical doping. Graphene is easily doped at edges or defects, but terrace sites are quite inert and do not easily react with dopants. Therefore, an increase in edge sites with hole array fabrications would allow control of dopant density and distribution within the graphene, and the ability to directly influence conductivity.

Thus, this research is focused on the role the copper substrate plays on CVD graphene deposition, as well as the possibility to control and manipulate the features of the copper substrate that influence CVD graphene formation. It is the hope that through controlled changes in the copper substrate template, it is possible to develop large-area CVD graphene with high conductivity and optical transmittance values. Furthermore, it is the focus to enhance the doping of the graphene films to further increase the conductivity behavior of graphene. It is believed through patterning of the graphene, it is likely chemical doping can be enhanced without significantly damaging the graphene layer, and potentially raising optical transparency.

1.4 Overview

As discussed in the previous sections of this chapter, nanotechnology is pervasive in a wide variety of applications such as lab-on-a-chip devices, sensing, environmental sustainability and clean up, energy harvesting and storage, and nanoelectronics.

However, for successful implementation of nanostructured materials for these applications, recise control over size and structure are imperative. Nanopatterning and templating are promising means to achieve these requirements. Nanopatterning utilizing lithography methods can provide highly selective placement and size control over nanopatterned lines, which may act as templates for electroless copper deposition. Templating of copper substrates provides the potential to controllably develop large-area CVD graphene of high quality, as well as enhanced chemical doping by patterning graphene films.

Chapter 2 is an overview of general methods and basic instrumentation used for the research presented in this work. Self-assembled monolayers (SAMs) provide a facile means to coat bulk substrates with a thin layer and change the chemistry at surfaces. Ellipsometry can be used to characterize the quality of these SAMs by measuring the thickness values, and can detect changes in thickness on the angstrom level. Goniometry is also an effective characterization tool to determine the hydrophilicity or hydrophobicity of substrates coated with SAMs, and can provide information of how well the SAM protects the underlying substrate through contact angle measurements. Atomic force microscopy is a versatile technique to not only characterize the surface morphology of SAMs, but also successfully create patterns within the monolayer resists exposing layers of the underlying substrate. The combination of all these techniques allows for in-depth analysis of SAM on silicon substrates, and can be used to effectively fabricate metallic nanofeatures on silicon substrates.

Chapter 3 describes electroless copper deposition experiments performed on bulk silicon to optimize electroless metal plating conditions. The optimization was done in

order to produce uniform and well-adhered copper films on silicon substrate surfaces. Copper films with different characteristics were observed when the concentration of solution components were varied, demonstrating the significant role concentration variation plays on electroless copper deposition behavior. Furthermore, preliminary studies were performed to investigate the role of additives in the electroless deposition process.

Chapter 4 includes detailed investigations of nanopatterning with subsequent electroless copper deposition within SAMs to fabricate copper nanowire features. Nanopatterning within three different types of monolayers were examined, and the capability of these monolayers to act as adequate resists to metal deposition probed. In addition, the behavior of electroless copper deposition upon changes in solution conditions, patterned lines dimensions, and silicon substrate doping was studied. The dependence of the fabricated copper nanowire feature on these parameters suggests a capability to manipulate nanowire dimensions and deposition uniformity. The conclusions of these experiment provided information for the successful construction of copper nanowire features connecting two gold microelectrodes, which permitted characterization of the electrical properties of these copper nanowire features.

Chapter 5 details the studies done on the chemical vapor deposition (CVD) of graphene on copper substrates. Graphene was grown via the CVD method on copper substrates with different structural characteristics, and the properties of the resulting graphene were probed, and demonstrated significant differences in quality. A time-sequenced analysis was done for CVD graphene deposition on these two copper substrates, and their deposition mechanisms illustrate behavior dependent upon features

of the underlying copper substrate. In order to manufacture graphene on relatively insulating substrates and controllably template graphene growth, graphene nanohole array templates were fabricated, and the possibility of inducing graphene growth at the edge of the templates examined.

Chapter 6 describes other graphene-based experiments again incorporating the manufacture of graphene nanohole arrays, but this time investigating their potential to enhance chemical doping of graphene films.

Chapter 7 summarizes the conclusions from the previous research chapters, and details future directions for the project focused on fabrication of copper nanowire features, as well as the research involving manipulation and controlled growth of CVD graphene. It is the focus of this research to continue to refine fabrication methods for both of these projects, specifically create nanowires with smaller dimensions and more complex geometries as well as develop better copper substrate templates for production of high quality CVD graphene. Furthermore, to continue to explore how these fabrication methods can be applied to other systems, such as the manufacture of nanowire features consisting of other metals besides copper, or constructing high quality CVD graphene on more complex patterned templates. In the end, it is the hope to utilize the controllability and flexibility of copper nanowire placement and configuration to create these complex patterned templates, which may be used to deposit graphene on surfaces in highly intricate arrangements.

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Chapter 2: General Methods and Instrumentation

2.1 Summary

This chapter provides a general description of methods and instrumentation utilized for the research discussed in the subsequent chapters of this dissertation. Self-assembled monolayers (SAMs) are a means to easily coat a surface with a molecule-thick layer, and allow manipulation of surface chemistry in addition to providing a protective coating against corrosion or other harsh processing conditions, as well as a resist for lithographic patterning.[1,2] In this research, SAMs on silicon and silicon oxide surfaces are implemented as a resist against metal deposition, and are formed via a simple wet chemistry method. SAMs of several different types are made and characterized to determine the optimal SAM coatings to use in the implemented scanning probe lithographic process. These characterization methods include goniometry and ellipsometry to characterize the contact angle and thickness of a SAM coating, which are good indicators of the quality and durability. Through goniometry one may obtain information about the type of chemical functionalities present on a surface. It involves measurement of the contact angle between a water droplet and the surface on which it resides, and can demonstrate the quality of a SAM by how well the value matches the predicted large contact angle values for a hydrophobic surface or the anticipated low contact angles for a hydrophilic surface.[3] Ellipsometry is a technique to determine thickness measurements of a SAM, and can provide information about the packing organization of the molecules on the surface. It measures the change in light polarization as a laser light is reflected off the surface, and the thickness of the SAM may be calculated based on this information coupled with the optical constants of the organic coating. Atomic force microscopy (AFM) is an effective tool to characterize surface morphology as well as manipulate it through the use of a scanning probe tip. Here the AFM

instrument is implemented to characterize the surface of SAMS, and to further pattern the surface for nanowire formation. This chapter outlines basic theory and method descriptions for the implementation of SAMs, goniometry, ellipsometry, and atomic force microscopy in this work.

2.2 Self-Assembled Monolayers

Self-assembled monolayers (SAMs) are monomolecular thin-film layers which spontaneously adhere and organize onto a substrate surface upon solution exposure. They are a simple means to control surface functionality on a wide range of surfaces, are highly ordered, and can provide a robust surface coating to prevent chemical wear or functionalization of the underlying material. All these features have led to their pervasive use in several research fields such as biosensing,[4,5,6] tribology,[7,8] electrochemistry,[9,10] catalysis,[11] microfabrication,[12,13] electronics,[14,15] and a host of other fields. A biosensor constructed by Frederix *et al*. consisting of gold coated with mixed SAMs of carboxylic or poly (ethylene glycol) groups demonstrated better SPR sensitivity, stability, and selectivity in comparison to commercial available affinity biosensors.[6] Kim *et al*. studied the friction behavior of gold surfaces coated with alkanethiols and silicon with silane monolayers to probe the capability of these monolayers to perform as industrial lubricants.[8] Fan *et al*. investigated charge transport through monolayers of thiolates and acrylates on gold and found differences in electron conductivity through SAMs containing different functionalities, lying the foundation for understanding charge transport for molecular wires.[16] In this research, the robust ability of SAMs to act as surface resists against harsh chemical exposure is employed.

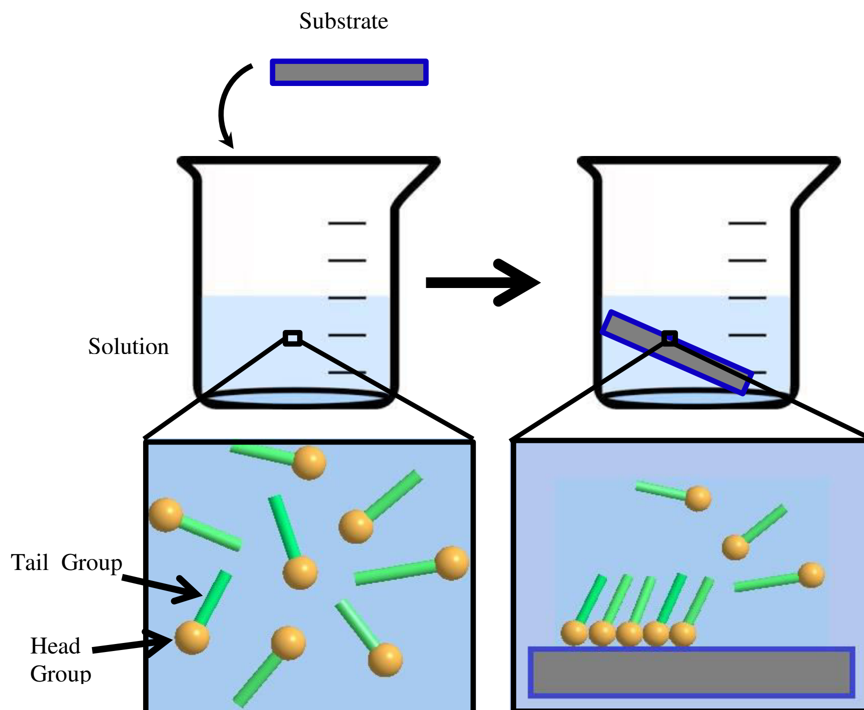

Figure 2.1. Schematic of self-assembled monolayer formation

Self-assembled monolayers are very easy to form via a wet chemical method, as demonstrated in Figure 2.1. A substrate is placed in a solution containing a millimolar concentration of a molecule with a functional head group that either has an affinity for or may react with the substrate surface. As head groups from several molecules interact with the substrate and surface coverage increases, the tail groups of the surface-attached molecules begin to interact by Van der Waals forces to help stabilize the SAM. Molecules located far apart from one another tilt from the surface normal to maximize these interactions,[17] as illustrated in the lower right hand box in Figure 2.1. Most robust SAM tail groups consist of long alkane chains, which have been shown to create highly stable monolayers with chain lengths greater than about 15 carbon chains,[18,19] but aromatic rings[20,21] and other functionalities to promote hydrogen bonding and cross-linking have also been studied.[22,23,24] Monolayers consisting of alkane chain lengths shorter than

approximately 15 carbons exhibit characteristics of a liquid-like structure on the surface indicative by widely spaced molecules, large molecular tilt angles, and low contact angles.[18] However, SAMs with alkane chains with a carbon number greater than 15 display densely packed organization with low tilt angle, and high contact angle. In order to maximize substrate coverage and the stabilizing interactions of the tail groups, most well-ordered monolayers are formed within a 24 hour period.[25,26] A majority of molecular adsorption onto the target substrate occurs within the initial seconds of solution exposure, and organized structuring may occur within a large range from minutes to hours depending upon the type of SAM, but most monolayers illustrate permanent structures by the end of 24 hours.[25,26]

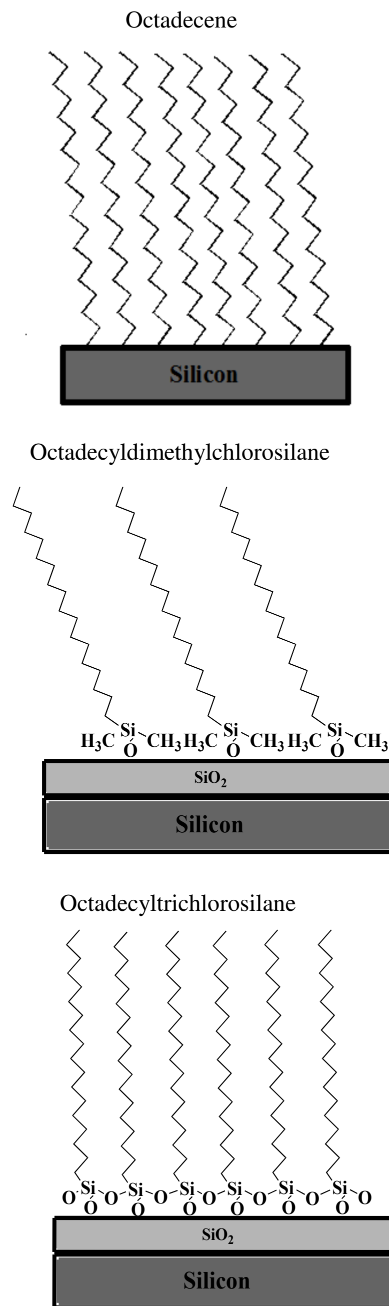

Figure 2.2. Schematic of octadecene on silicon (top), octadecyldimethylchlorosilane (ODMS) on silicon oxide (middle), and octadecyltrichlorosilane (OTS) on silicon oxide (bottom).

The two types of monolayers utilized in the following chapters will be an octadecyl moiety attached to silicon, as well as reactions of octadecyldimethylchlorosilane (ODMS) and octadecyltrichlorosilane (OTS) to attach these silanes onto silicon oxide, as shown in Figure 2.2. The alkyl system on silicon results from the thermal[27,28] or photoactivated[28] reaction of an alkene molecule with a hydrogen-terminated silicon surface. To form the ODMS and OTS SAMs, the chlorosilanes initially undergo a

hydrolysis reaction with the trace amounts of water in the nonpolar solvent and adsorbed water at the oxide surface to give –OH functionalites, and then the silanes become attached to the oxide surface by a subsequent dehyrolysis reaction with the oxide's –OH surface groups.[29] Alkyl functionalities on silicon and silanes on silicon dioxide have been studied extensively for their robust qualities to act as a resist for patterning methods.[1,30,31,32] All three molecules are of similar length, approximately 2.4 nm,[33] with 18 carbon chains which are long enough to promote good packing via Van der Wahls interactions. The major differences between the three SAMs include a strong covalent bond directly onto the silicon surface for the octadecyl SAM, and the silanes are atop the silicon oxide, which is able to provide a more insulating surface for the specific application of this research to form metallic nanowires. Furthermore, the ODMS monolayer contains methyl groups adjacent to its silane functional groups, which may negatively influence its molecular packing capability due to steric hindrance between molecules. The octadecyl SAM on silicon and the OTS SAM do not contain such side groups. Lastly, the OTS is able to polymerize at the SAM-oxide interface to create a connected network between the surface-attached molecules. All of these characteristics can lead to differences in molecular packing, and their capability to act as chemical resists. Further details of each monolayer system are given in later chapters.

2.3 Goniometry

Goniometry is a method that may be employed to measure the contact angle between a liquid droplet and the solid surface, and measures surface free energies, which can also be related to the hydrophobicity or hydrophilicity of the surface.[3] Here, it is a method implemented to characterize SAMs seeing as the surface functionality of the sample has a strong influence on whether the surface chemistry is more hydrophobic or hydrophilic, leading to differences in

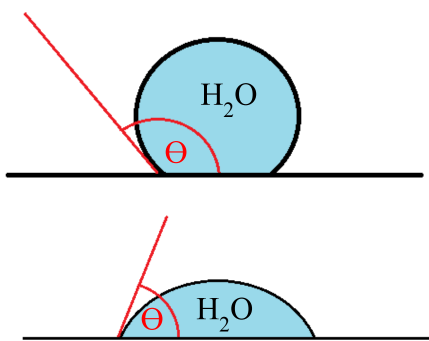

Figure 2.3. Illustration of a contact angle measurement (Θ) with a water droplet on a hydrophobic surface (top) and hydrophilic surface (bottom).

contact angle values with a water droplet. As one changes the exposed terminal group at the substrate surface, the contact angle changes in value due to differences in the relative energies of the solid-liquid, solid-air, and liquid-air interfaces.[34] This relationship of the contact angle, θ, and the interfacial energies can be expressed in Young's Equation as follows:

$$\gamma_{SG} = \gamma_{SL} + \gamma_{LG} cos\theta$$

where γ_{SG}, γ_{SL}, and γ_{LG} are the solid-air interfacial energy, solid-liquid interfacial energy, and liquid-air interfacial energy.[34] For instance, a methyl-terminated SAM is hydrophobic and results in a large contact angle as seen in the top image of Figure 2.3. The tension for the solid-air interface is comparably lower than the tension for the solid-liquid interface, the droplet beads up, resulting in a higher contact angle value. Conversely, a surface composed of hydroxyl groups will express a significantly lower contact angle, as illustrated in the bottom image in Figure 2.3. The hydrophilic surface possesses a greater solid-air interfacial tension in relation to the solid-liquid tension, and the water droplet spreads out across the surface. In this research, only hydrophobic methyl-terminated SAMs with long alkane chains on silicon substrates are implemented. By comparison to previous literature values of well-characterized robust methyl-terminated SAMs of the same composition we can determine the quality of SAMs in this work. Deviation from literature values can result from increased surface roughness,[35] conformational defects in packing,[36] or influence from the underlying hydrophilic substrate penetrating through the monolayer.[3,36] Even though it may not be possible to specifically pinpoint the reason why monolayers in this work may deviate significantly from literature values, a majority of the causes

Monolayer	Contact Angle (°)
SiO_2	4 ± 2
H-terminated Si	68 ± 1
Octadecene	100. ± 2
ODMS	73 ± 1
OTS	109 ± 2

Table 2.4. Representative contact angle values for octadecene, ODMS, and OTS monolayers on silicon (100).

for deviation are undesirable for a densely packed, well-ordered SAM, and would most likely lead to a monolayer of poorer quality to act as a chemical resist.

Contact angles measurements were obtained for SiO_2, H-terminated silicon, octadecyl SAMs, ODMS SAMs, and OTS SAMs, and representative values are shown in Table 2.4. It is evident that modifications in surface functionality, and its relative hydrophobicity or hydrophilicity, can be tracked through contact angle measurements as we see the contact angle change from a few degrees for the very hydrophilic SiO_2, to a greater value for the less hydrophilic H-terminated silicon, to comparatively large values for the methyl-terminated SAMs with long alkane chains. Thus, as we form the SAM atop their designated substrates, we can use goniometry to verify the presence of the hydrophobic methyl-terminated SAMs. Furthermore, it is possible to measure differences in contact angle measurements between the three monolayers themselves, which will be discussed in more detail in later chapters.

Contact angles are presented in this text as average values calculated from 6 measurements obtained across each sample surface, unless otherwise indicated. The goniometer used was a Ramé-Hart, Inc. NRL C.A. Goniometer.

2.4 Ellipsometry

Ellipsometry is an optical technique which can be used to investigate many different properties of thin films, such as dielectric constants,[37,38] thickness values,[37,38] surface roughness,[39] crystalline structure,[40,41] electrical conductivity,[42,43] and other material characteristics. Giri *et al*. investigated the crystalline to amorphous phase transition of silicon due to argon ion implantation utilizing ellipsometric techniques.[41] Tiwald *et al*. coupled infrared ellipsometry and anodic oxidation sectioning to obtain resistivity measurements and develop doped silicon carrier concentration profiles.[43] For this research purpose, ellipsometry is used to characterize SAMs on silicon substrates and obtain thickness values. These values provide information about the monolayer molecular packing and organization at the monolayer-substrate interface, and reflect the monolayer's potential ability to act as a resist for the formation of electroless-plated copper nanowires on the substrate surface.

A schematic of a single-wave ellipsometer is shown in Figure 2.5, and represents the setup found within the Rudolph Auto EL III ellipsometer used in this research. A light source is

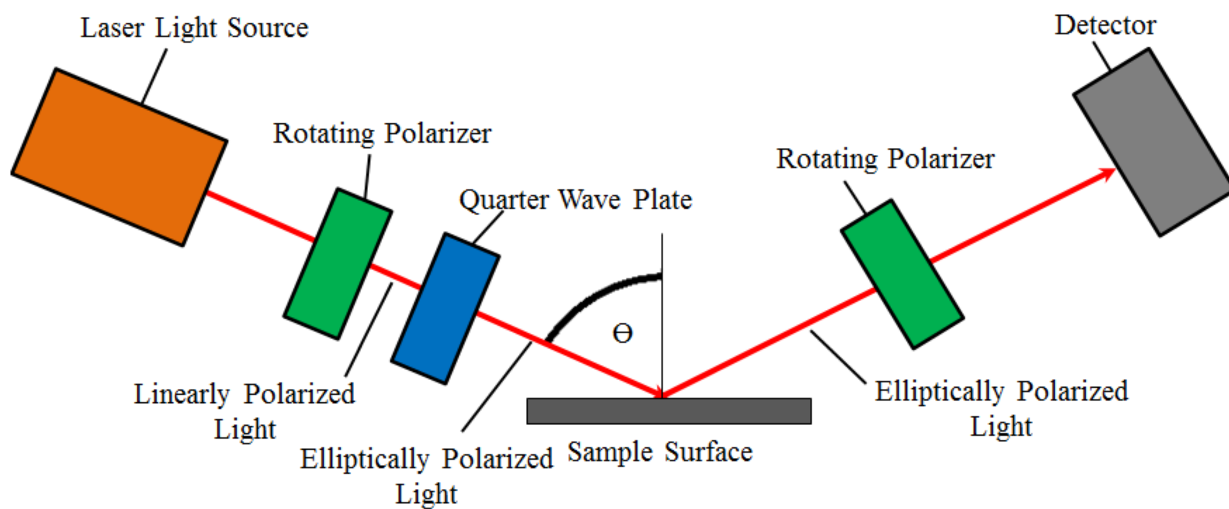

Figure 2.5. Schematic of ellipsometer instrument.

focused toward a sample surface at a 70° incident angle, ϴ. Before the light reaches the

sample surface, it first passes through a rotating polarizer to change the unpolarized laser light to linearly polarized light, and continues on through a quarter-wave plate compensator to further adjust the light to an elliptical polarization. When the elliptically polarized light hits the sample surface it travels through the thin film on the substrate surface until it reaches the film-substrate interface, where it is then reflected and passes through the film a second time. If the light travels through a dielectric thin film, the amplitude and phase will change in the s-polarized and p-polarized light components of the elliptically polarized light. The second polarizer rotates in conjunction with the first rotating polarizer to minimize the reflected light intensity at the detector. The parameters Δ and Ψ are then calculated from the angles of the two rotating polarizers relative to the quarter-wave plate. The parameter Δ is the change in phase difference between the s-polarized and p-polarized light before sample interaction relative to after reflection. The tangent of parameter Ψ is the ratio of the normalized amplitude intensities of the p-polarized and s-polarized light components. These parameters paired with pre-determined index of refraction values can be used to calculate the thickness of a thin film on a substrate down to the sub-nanometer level utilizing the following equation:

$$\frac{R_p}{R_s} = \tan\Psi \bullet e^{i\Delta}$$

The variables R_p and R_s represent the normalized amplitudes of the p-polarized and s-polarized light components and i is the imaginary number.[44]

Ellipsometry was used to determine thickness values of octadecyl, ODMS, and OTS SAMs on silicon substrates, and example values for these monolayers are shown in Table 2.6.

Monolayer	Thickness (Å)
Octadecene	23.9 ± 0.9
ODMS	11.3 ± 0.5
OTS	28.2 ± 0.6

Table 2.6. Representative thickness values of octadecene, ODMS, and octadecene monolayers.

All three of these molecules are 18 carbon chains with an approximate length of 2.4nm.[33] If all three molecules had similar packing and orientation, it would be expected their thickness values would mirror one another. The differences in their thickness values likely result from their different packing behavior, which will be examined in more detail in later chapters. All thickness measurements presented are calculated averages obtained from 6 randomly-placed measurements across each sample surface.

2.5 Atomic Force Microscopy

2.5.1 General Overview

Atomic Force Microscopy (AFM) is a powerful scanning probe method to investigate many surface properties on a micron to sub-nanometer length scale. These surface properties may include morphology, elasticity, magnetic domains, conductivity, relative surface energy values, electrostatic behavior, and a host of other characteristics. Due to its adaptability to measure a wide variety of surface qualities, research utilizing atomic force microscopy spans a large range of applications including nanofabrication,[45,46] molecular electronics,[47,48] cellular motion and surface interactions,[49,50] tribology,[51] polymer science,[52] DNA studies and manipulation,[53,54] electrochemical mapping,[55] and several other research areas. Electrical measurements of a single dithiolated molecule inserted into an insulating SAM were conducted by Rawlett *et al*. to understand its electron transport properties.[48] Muller *et al*. was able to image

real time motions of purple membrane down to a resolution of 0.7 nm.[49] Macpherson *et al*. simultaneously mapped surface morphology and electrochemical properties of polycarbonate ultrafiltration membranes with a platinum probe tip coated with electrophoretically deposited paint.[55] In this work, the AFM microscope is employed to create topographical maps of surfaces on the microscale, as well as pattern SAMs at the nanoscale.

A basic schematic of an atomic force microscope is shown in Figure 2.7. A diode laser is focused near the edge of a cantilever positioned above a sample surface. At the end of the cantilever is a small tip, with a radius of curvature in the tens of nanometers, which will scan the surface in the x and y axis implementing motion via a piezoelectric unit. The piezoelectric unit may be attached to the tip to scan across a stationary sample, or be coupled to a sample stage to move in relation to a stationary tip, which is found in the Digital Instruments Nanoscope IIIa Multimode and Nanoscope E with Lateral Force Mode used for this research. As the tip encounters changes in height, it becomes deflected in the z axis. All these changes in the x, y, and z axis are detected by a photodetector as the laser light is deflected to different regions on its surface. The laser light creates voltage readings as it hits various locations on the photodetector, and the differences in voltage between the four partitioned quadrants of the photodetector indicate the position of the deflected laser light. These voltage readings can be analyzed by a computer interface to

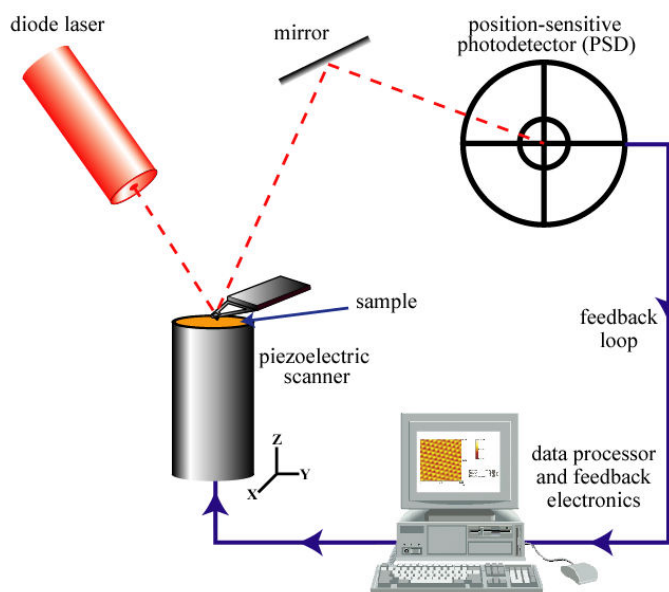

Figure 2.7. Basic schematic of AFM instrument and operation.

determine changes in deflection as the tip scans the surface, and thereby create maps of surface features. Resolution of AFM images can get down to the sub-nanometer scale due to the controlled motion of the piezoelectric scanner. An AFM microscope may be operated is a variety of modes to map different surface properties, and the two modes used here are contact mode and tapping mode.

2.5.2 Contact Mode

Contact Mode AFM, as the name suggests, involves direct contact of the tip with the sample surface. The tip is lowered onto a sample surface until contact is made with a set applied force, and then the tip scans the surface of the sample in the x and y direction. When the tip comes across a surface feature with a difference in height, the tip becomes deflected in the z direction, and causes a change in position of the deflected laser light on the photodetector

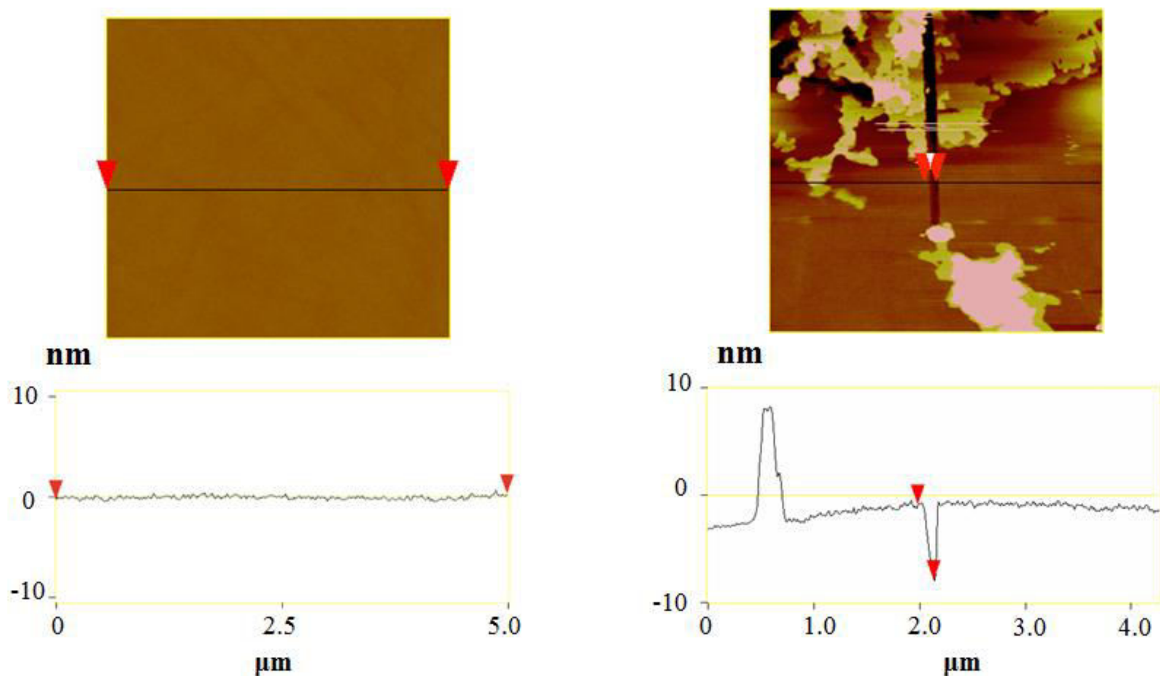

Figure 2.8. AFM image of flat OTS monolayer with cross section analysis (left). AFM image of OTS monolayer with surface debri and etched line, with cross section analysis (right).

surface. In order to keep a constant force on the surface, the piezoelectric scanner moves the sample stage in the z direction during the course of the scan. These movements in conjunction with x and y motions during scanning allow the computer interface to produce a topographical map of a microscale area on the sample surface.

An example of a topographical AFM image is shown in Figure 2.8. The left image is a flat OTS monolayer, and shows no change in color across the 5 micron square dimension. This indicates a flat surface, which can be reaffirmed by the relatively flat line in the cross section analysis with a 20 nm height scale. However, when there are surface features with variations in height, high features show up as bright colors in the AFM image, and low features can be attributed to dark colors. This is observed in the right image of Figure 2.8, which has similar lateral dimensions and height scale, and illustrates an OTS monolayer with surface debris with a large height and an AFM-patterned line with a large depth. The AFM patterned line was developed by scanning the substrate surface with a large force of approximately 3000 nN, which consequently etches away part of the substrate surface. These nanoscale variations in height across the few-micron size image can be noted in the cross section analysis for this OTS monolayer as well. Thus, AFM can be effectively utilized to note surface morphology on the nanoscale, and in addition be used as a tool for patterning. It allows for the production of selectively placed patterns on the surface with nanoscale dimensions for nanowire formation, as well as tracking of topography changes before and after electroless metal deposition.

2.5.3 Tapping Mode

Tapping mode is implemented here to create topographical maps identical to ones produced by contact mode, but is used for imaging delicate samples. If the surface is delicate,

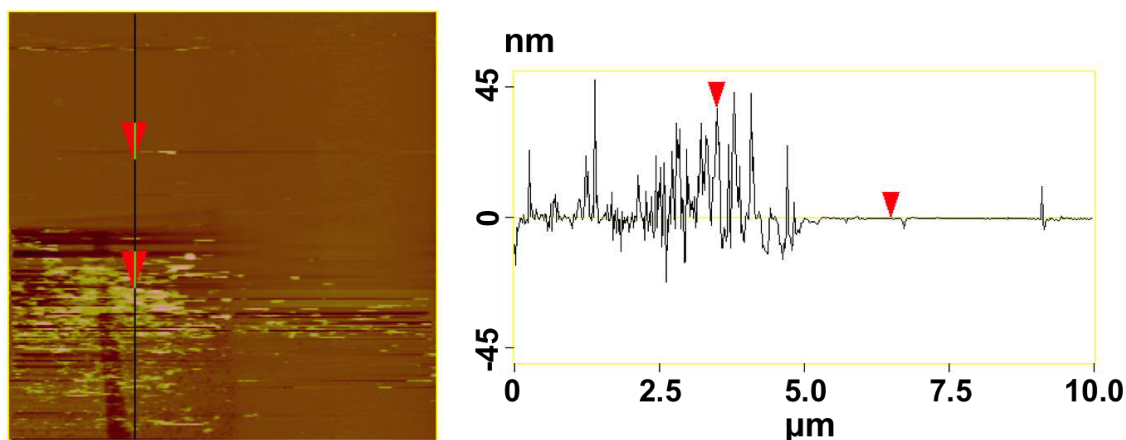

Figure 2.9. AFM image and cross section of ODMS monolayer after AFM patterning, contact mode imaging, and electroless copper deposition.

such as a disordered SAM or a sample with components weakly adhered to the surface, contact mode can damage the SAM in the imaged region or loosen the weakly attached material and drag it across the surface. An example of this is illustrated in the AFM image displayed in Figure 2.9. This image depicts an ODMS monolayer after AFM patterning of the darkly-colored line, followed by imaging of the line in contact mode, and subsequent exposure to electroless metal deposition. There is clear debris accumulated in the square region near the AFM-patterned line, which indicates enhanced metal deposition in this area as compared to the flat surrounding region. The square in the AFM image was the imaging area performed in contact mode prior to electroless copper plating. Clearly, contact mode may disrupt a SAM enough weaken its chemical resistance. Furthermore, this image displays streaks adjacent to the tall debris on the surface, suggesting it is being dragged across the surface by the scanning contact mode AFM tip. In this research, sensitive samples such as silicon oxide, microelectrode arrays with a potentially disordered SAM, and samples with weakly adhered debris are imaged in tapping mode to prevent disruption of the sample surface.

The basis for tapping mode atomic force microscopy is to oscillate the cantilever with the imaging tip close to its resonance frequency via a piezo located in the AFM tip holder, and place

the oscillating cantilever in close enough proximity of the sample surface for the tip to "tap" the surface near its downward oscillation minimum. Similar to contact mode, a constant oscillation amplitude is set while the tip scans the sample surface. When the tip encounters changes in height, the tip-sample interaction changes and either dampens or increases the oscillation amplitude. To keep the amplitude constant, the piezoelectric unit in the sample stage moves in the z direction to compensate for these changes in oscillation amplitude.

2.6 Implementation

The research presented in this work was performed utilizing the methods and techniques described throughout this chapter. Detailed descriptions of methods stemming from these techniques, and other minor techniques will be described in their relevant chapters. Self-assembled monolayers (SAMs) act as resist monolayers to electroless metal deposition, and are thin enough to permit AFM nanopatterning for selective placement of nanowires within the monolayer area. They are implemented primarily in Chapters 3 and 4. Goniometry and ellipsometry are characterization techniques for these SAMs by measuring contact angles and thickness values, and provide information about the packing of the SAMs. Atomic Force Microscopy is a powerful tool that is present in all the following chapters of this text, but is heavily applied in Chapters 4 and 5. In Chapter 4 the AFM is used to characterize a variety of monolayers, as well as selectively pattern nanoscale regions of the monolayers' surfaces, and obtain topographical images of metallic nanowires formed within microelectrode arrays. It is used in Chapter 5 to characterize the morphology of CVD graphene on a variety of copper surfaces, as well as graphene regrown within graphene templates.

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Chapter 3: Electroless Copper Deposition – Solution Optimization Studies

3.1 Abstract

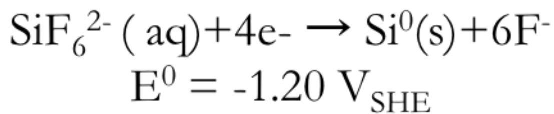
Electroless metal deposition has been shown to be a quick and simple method to create metallic features for implementation into circuits and other electronic devices. It is the objective of this research to utilize metal deposition from electroless plating solutions to form nanoscale copper wires on the surface of silicon substrates in a very selective and controlled manner. Optimization of the electroless plating solution was performed on bulk silicon (100) surfaces with the hopes of producing high quality copper wires on the nanoscale, as well as investigating the role of the solution components in the electroless deposition process. Silicon (100) wafers were exposed to copper plating solutions with a range of ammonium fluoride, copper sulfate, ascorbic acid, and sodium tartrate concentrations. It was found that ascorbic acid promotes adhesion of the electrolessly deposited copper film to the underlying silicon, however at high concentration it forms stress-induced features from high deposition rates. For this purpose, sodium tartrate is necessary to complex with the free copper ions, leading to a reduction in deposition rate and uniformly plated copper films with no visible evidence of stress-induced formations. The optimal plating solution was chosen to be 0.27 M NH_4F, 0.13 M $CuSO_4$, 14 mM ascorbic acid, and 18 mM sodium tartrate, which produced uniform copper films with strong adhesion to the silicon surface.

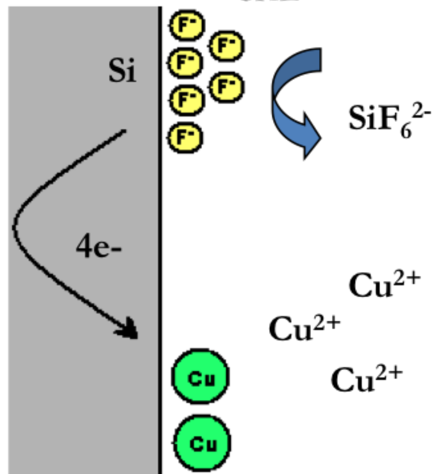
3.2 Introduction

Electroless metal deposition provides a quick and easy method to produce uniform metallic films,[1] and more importantly may produce high quality plating within nanoscale templated regions on a substrate surface.[1,2,3] It is for this reason electroless metal deposition is a well-utilized method for fabrication of modern integrated circuit (IC) technology.[1,4] But, it also

has other applications in microfluidics,[5] plasmonics,[3,6] electromagnetic shielding,[7] fuel cells,[8,9] catalysis,[10] sensors,[11],[12] and several other additional applications. Allen *et al*.[5] used electroless metal deposition to develop a Ni-Ag thermocouple capable of measuring changes in temperature caused by chemical reactions within a microfluidic channel. Byeon *et al*.[10] were able to monitor the catalytic conversion of carbon monoxide at the surface of bimetallic nanostructure formed by electroless metal deposition. Hilmi *et al*.[11] electrolessly deposited gold films on glass substrates for capillary electrophoresis chips, and were able to increase sensitivity of catechol and several nitroaromatic explosives. The experimental procedure for electroless metal deposition simply requires creating a deposition solution with all the necessary components, and exposing a target substrate surface to the solution for a specific amount of time. Other common metallic film deposition methods such as vapor deposition,[13,14] thermal spray coating,[15] and electrodeposition[16,17] require expensive equipment, time-intensive work, heating of the substrate, application of an external voltage, or are limited to only high quality production of thick bulk films rather than deposition on nanometer-size regions of the substrate surface. In this research, electroless copper deposition offers a cheap, fast, and easy means to selectively deposit copper in regions of a silicon surface that are templated for copper nanowire growth.

Electroless deposition occurs when either the material at a substrate surface is displaced by a metallic ion in solution due to the lower oxidation potential of the metallic ion compared to the substrate material, or a reducing agent in the bulk solution catalytically reduces the metal ion at the substrate surface.[1] The first instance describes galvanic displacement, and the second is termed autocatalytic deposition. In galvanic displacement, the material of the substrate is dislodged from the surface and is released into solution as a charged ion, whereas the previously dissolved metallic ion is reduced and adheres to the surface. Autocatalytic deposition does not





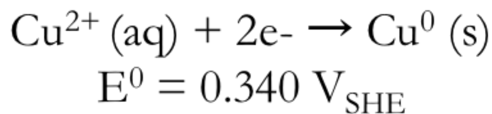
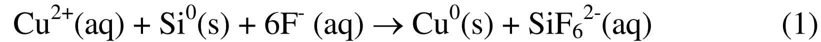


Figure 3.1. Schematic of electroless copper deposition process at surface interface with oxidation and reduction half cell reactions and standard electrode potentials.

involve any removal of the substrate material, and only involves oxidation of a reducing agent at the substrate surface, freeing electrons for metal reduction.[1] Copper has been a common metal to utilize with galvanic displacement and autocatalytic deposition because of its low cost, low resistance values,[18,19] high electromigration resistance,[18,19] and strong adhesion to silicon surfaces,[19] which is a prominent material in the electronics field. Other metals utilized in electroless metal deposition such as gold,[20,21] silver,[22] and nickel[23,24] are either comparatively costly, possess higher resistance values, or adhere poorly to silicon surfaces. There have been several studies investigating galvanic displacement or autocatalytic deposition of copper on silicon substrates.[19,25,26] Solutions implemented in galvanic displacement for deposition on silicon normally consist of a copper source, complexing agent, and fluoride-containing species.[1] Autocatalytic deposition of copper frequently involves a similar solution with a copper ion source and complexing agent, but it further includes formaldehyde as a common reducing agent, and NaOH to create a highly basic solution necessary for formaldehyde oxidation.[27] Autocatalytic deposition provides some benefits over galvanic displacement such as unlimited deposition and more uniform film structure.[1] However, for application into this research, galvanic displacement methods were chosen since the

deposition solution for this method does not require highly basic solutions. Previous studies have shown the stability of silane self-assembled monoalyers (SAMs) is significantly compromised when exposed to very basic solutions,[28] which is a requirement for many autocatalytic deposition solutions. It is the ultimate objective of this research to use electroless copper deposition to create nanowires within AFM-patterned SAM resists, mainly silane SAMs. Thus, galvanic displacement deposition is expected to provide more selective copper deposition within patterned regions of the SAM monolayer resists, and not adversely influence monolayer stability, which could lead to metal deposition within the resist surface regions.

Galvanic displacement deposition of copper on silicon surfaces via fluoride-containing solutions is a redox reaction where both the anodic and cathodic processes occur simultaneously at the silicon substrate surface.[1] Electrons from the oxidized silicon are transported to the copper ions at the substrate surface for copper reduction, as illustrated in Figure 3.1. The overall reaction equation at the silicon surface in the presence of F^- is:[25]



$$Cu^{2+}(aq) + Si^0(s) + 6F^-(aq) \rightarrow Cu^0(s) + SiF_6^{2-}(aq) \qquad (1)$$

The surface silicon is oxidized and becomes freed from the surface in the form of the SiF_6^{2-} species, whereas the copper ions in solution located near the substrate interface become reduced and subsequently adhered to the substrate. The overall reaction in equation (1) can be split into two half-cell processes as depicted by the anodic reaction at the top of Figure 3.1 and the cathodic reaction at the bottom of the same figure:[1]

$$SiF_6^{2-}(aq)+4e- \rightarrow Si^0(s)+6F^- \qquad E^0 = -1.20\ V_{SHE} \qquad (2)$$

$$Cu^{2+}(aq) + 2e- \rightarrow Cu^0(s) \qquad E^0 = 0.340\ V_{SHE} \qquad (3)$$

The largely positive standard electrode potential of the copper reduction at 0.340 V versus the standard hydrogen electrode (SHE) in comparison to that of reaction (2), with a value of -1.20 V_{SHE}, shows the affinity for copper reduction in the presence of silicon and fluoride ions. However, the standard reduction potential of Cu^{2+}/Cu^0 significantly decreases in electroless deposition solutions containing fluoride species (-0.48V_{SHE} in 40% NH_4F and -0.12V_{SHE} in 0.5% HF). As a result, hydrogen evolution occurs at the silicon surface as well as copper deposition:

$$2H^+(aq) + 2e- \rightarrow H_2(g) \qquad E^0 = 0.0\ V_{SHE} \qquad (4)$$

Hydrogen production at the silicon surface is believed to create electrolessly deposited copper films with weak adhesion to the silicon surface.[19] Because of this, chemical species are added into the deposition solution which are believed to quench the hydrogen at the silicon substrate surface. Some of these additives include ascorbic acid[19,29] and fumaric acid,[19] which are well-known hydrogen scavengers. Da Rosa *et al.*[29] has discovered upon inclusion of the ascorbic acid into the deposition solution, though, large raised features are induced in the plated copper films, which are believed to be the result of film restructuring to relieve compressive stresses during film growth with high deposition rates. The further addition of sodium tartrate to the deposition solution, which is proposed to act as a chelator of copper ions to reduce copper deposition rates,[26] resulted in the formation of uniform copper films which were well-adhered to the surface.[29] In constrast to the claim by Maganin *et al.*[19] that ascorbic acid acts as a hydrogen scavenger for improved film adhesion, Da Rosa claims the increased copper film adhesion with the ascorbic acid additive is a consequence of the localized increase of silicon dissolution rates surrounding nucleated copper metal during the metal deposition process. The inhomogeneous etching of the silicon leads to a rough and jagged silicon-copper interface with an increased surface area, which allows for the improved adhesion. Furthermore, Da Rosa made no claim as

to the specific mechanism behind improved copper film growth with the sodium tartrate additive. Clearly, copper deposition by galvanic deposition with the inclusion of additives to produce well-adhered and uniform copper thin films is not well understood. Additionally, no studies have been performed to optimize the concentration of deposition solution additives to maximize film adhesion and uniformity, as well as to investigate the role these additives may play in electroless copper deposition.

It is for this purpose the electroless deposition of copper was studied on bulk silicon substrates by deposition solutions with varying concentrations, and the concentrations optimized to produce copper thin films with good adhesion and uniformity. The solution components included ammonium fluoride, copper sulfate, sodium tartrate, and ascorbic acid. The concentration of each one was individually varied, and the uniformity of copper films investigated with an optical microscope, as well as the adhesion with the scotch tape test. The optimized concentrations were found to be 0.27 M NH_4F, 0.13 M $CuSO_4$, 18 mM sodium tartrate, and 14 mM ascorbic acid to form electrolessly deposited copper films with good adhesion to the bulk silicon substrates as well as uniform deposition. Also, ascorbic acid was found to aid in the reduction of free copper ions and increase the adhesion and uniformity of deposited copper. However, in large concentrations it induces large raised structures across the film surface which interfere with its adhesion capability. The addition of sodium tartrate is necessary to remove these raised formations and improve copper film uniformity.

3.3 Materials and Methods

3.3.1 Selectivity of Electroless Copper Plating

Self-Assembled Monolayer Formation and Characterization

In order to demonstrate the selectivity of electroless copper deposition on bare silicon as opposed to silane-coated resist regions, bulk silicon wafers with native oxide and wafers with an OTS coating were exposed to an electroless copper deposition solution, and their surface morphology investigated by AFM. Bare instrinsic Si(100) wafers (L441 - El-Cat.com) with a native oxide approximately 1 cm^2 in area were sonicated in acetone for 10 minutes and rinsed with acetone. They were then subject to a piranha solution (3:1 v/v solution of sulfuric acid and 30% hydrogen peroxide in water) for 10 minutes, following an extensive rinse with Nanopure water (18 MΩ). One bare silicon wafer was saved under nitrogen for further experiments, and all other wafers were sonicated in toluene for 20 minutes. The wafers were then placed in a solution of 1.3 mM octadecyltrichlorosilane (OTS) in toluene for 24 hours. After the wafers were removed from the OTS solutions, they were sonicated in toluene for 30 minutes, and rinsed with toluene, chloroform, acetone, and ethanol.

The OTS monolayers on intrinsic Si(100) were characterized using thickness and contact angle measurements. Ellipsometry measurements were obtained using a Rudolph Research AutoEL ellipsometer with Program 221 (NU = 1.45, TL = 17.0, NL = 1.469). For the specific OTS sample used in this section, a value of 28.0 ± 0.7 Å was calculated by averaging five readings across the sample surface. The literature for the OTS thickness is approximately 26 nm,[30] showing relatively good agreement with the thickness value observed here. Contact angle measurements were acquired with a Ramé-Hart, Inc. NRL C.A. Goniometer. The particular OTS

sample utilized in this section also had a contact angle value of 109.8 ± 0.8º calculated by averaging six readings across the sample surface.

Atomic Force Microscopy (AFM) Imaging and Electroless Copper Deposition

The topography of the bare intrinsic Si(100) wafer was obtained using AFM with a Digital Instruments Nanoscope IIIa Multimode instrument in tapping mode. The tip was a diamond-like carbon coated tip (TAP300DLC, Ted Pella) with a force constant of 40 N/m and a resonance frequency of approximately 300 kHz. The scan rate was around 0.5 Hz. Tapping mode was incorporated because the silicon oxide surface is sensitive, and may be disrupted by the AFM tip in contact mode.

The OTS sample on the intrinsic Si(100) was imaged using a Digital Instruments Nanoscope E in contact mode. The tip utilized for this imaging was a silicon nitride tip (NPS, Bruker) with a force constant of 0.24 N/m, and scan rate of 1.5 Hz. The silicon sample coated with an OTS monolayer is relatively robust,[31] and therefore can be imaged in contact mode most likely without damaging the monolayer integrity. It was employed here for faster data collection, considering contact mode can obtain adequate images with faster scan rates in relation to tapping mode AFM.

Both the bare intrinsic silicon (100) and the OTS monolayer on top of the intrinsic (100) surface were exposed to a copper plating solution for one minute containing 0.28 M NH_4F, 0.13 M $CuSO_4$, 19 mM sodium tartrate, and 15 mM ascorbic acid. Upon removal they were rinsed with Nanopure water (18 MΩ) and topographical maps of the resulting surface morphologies collected with the same AFM instruments and parameters as described above.

3.3.2 Concentration Studies and Optimization of Electroless Copper Deposition on Bulk Silicon

Following confirmation that electroless copper deposition primarily occurs only on bare silicon surfaces and not within OTS monolayers regions with the plating solutions listed above, the individual concentrations of the electroless copper plating solution were varied and the effect on deposited copper films examined. Bare instrinsic Si(100) wafers (L441 - El-Cat.com) with a native oxide approximately 1 cm^2 in area were sonicated in acetone for 10 minutes, rinsed with acetone, and dried with nitrogen gas. As a control experiment, a single wafer was exposed to a solution for one minute with 0.27 M NH_4F and 0.13 M Cu^{2+} with no ascorbic acid or sodium tartrate additives. Six silicon wafers were subject for one minute to a copper deposition solutions containing 0.27 M NH_4F, 18 mM sodium tartrate, 14 mM ascorbic acid, and a range of $CuSO_4$ concentrations: 0 M, 0.017 M, 0.032 M, 0.068 M, 0.13 M, and 0.25 M. Six silicon wafers were subject for one minute to a copper deposition solutions containing 0.13 M $CuSO_4$, 18 mM sodium tartrate, 14 mM ascorbic acid, and a range of NH_4F concentrations: 0 M, 0.095 M, 0.18 M, 0.28 M, 0.36 M, and 0.46 M. Five silicon wafers were subject for one minute to a copper deposition solutions containing 0.27 M NH_4F, 0.13 M $CuSO_4$, 18 mM sodium tartrate, and a range of ascorbic acid concentrations: 0 M, 7 mM, 14 mM, 28 mM, and 56 mM. Five silicon wafers were subject for one minute to a copper deposition solutions containing 0.27 M NH_4F, 0.13 M $CuSO_4$, 14 mM ascorbic acid, and a range of sodium tartrate concentrations: 0 M, 9 mM, 19 mM, 88 mM, and 0.45 M.

After the copper films were formed on the surfaces of the silicon substrates, optical images were obtained to probe the macroscale structure of the electrolessly deposited copper on the bulk silicon wafers. Optical images were acquired with a Nikon 10x objective lens with DC12V Sony camera and GrabBee software. UV-Vis spectra were collected with a Cary 300

UV-Vis Spectrometer. Tape tests were performed by placing a piece of scotch tape over a portion of the wafer samples with electrolessly deposited copper films, the tape was pressed down gently, and removed.

3.4 Results and Discussion

3.4.1 Selectivity of Electroless Copper Plating

In order to confirm electroless copper deposition occurred only on the surface of exposed silicon, a piece of bare silicon (100) and OTS monolayer were both exposed to a standard copper plating solution for one minute. The AFM images with cross sections displayed in Figure 3.2 illustrate the microscale surface morphology of bare silicon with native oxide (a) and OTS monolayer on SiO_2 (b). Before electroless deposition solution exposure, both the silicon and monolayer surfaces are flat as observed by their cross sections with minor height variability across a 5-micron length, and by their small roughness values of 0.15 nm and 0.19 nm. The topography of the bare silicon surface changed drastically after solution exposure, however, due to the deposition of copper features depicted in the AFM image in Figure 3.2-c. The corresponding cross section immediately below the AFM image displays larger changes in height across a similar 5-micron length, producing increased surface roughness values of approximately 10.3 nm. The surface morphology of the OTS monolayer remained very flat following exposure to the electroless copper deposition solution as apparent in image (d), with roughness values remaining similar to those prior to copper deposition exposure at 0.21 nm. Additionally, the photographs of the macroscopic wafers shown in Figure 3.2-e showing the bare silicon substrate (right) and OTS-coated wafer (left) after electroless copper deposition demonstrate how the bare grey-colored silicon substrate has become copper colored following copper deposition exposure, whereas the wafer coated with the OTS monolayer remained a grey color characteristic of a bulk

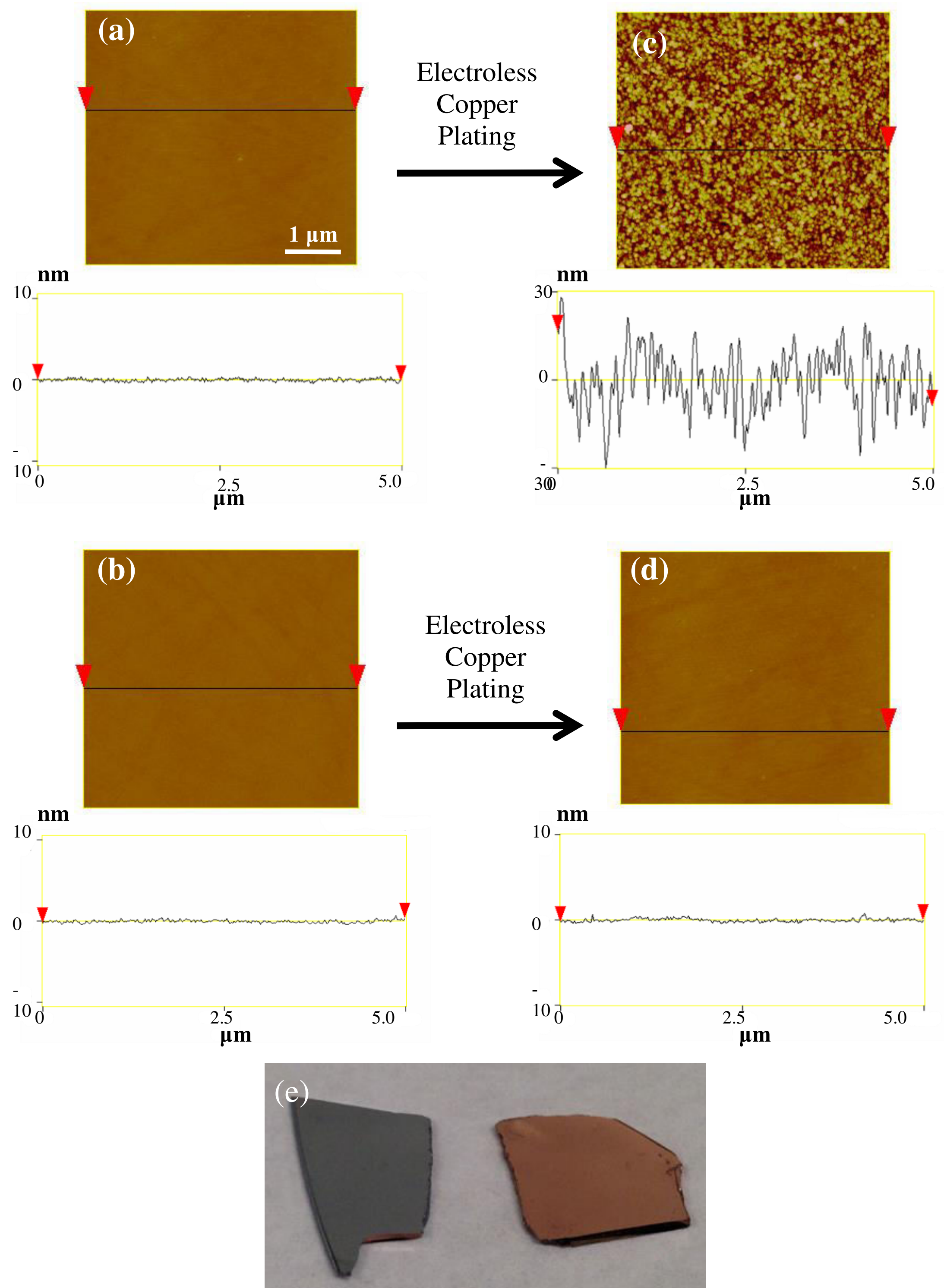


Figure 3.2. AFM images and cross-sections of (a) bare silicon (100) and (b) an OTS SAM-coated silicon wafer before electroless copper deposition. AFM images and cross-sections of (c) bare silicon (100) and (d) an OTS SAM-coated silicon wafer after electroless copper deposition. (e) Photograph of a bare silicon (100) wafer after copper deposition exposure (right) and a silicon wafer coated with an OTS monolayer after copper deposition exposure (left).

silicon sample. All of this evidence supports that electroless copper deposition occurs selectively on exposed silicon surfaces, and areas coated with a SAM resist inhibit copper plating.

3.4.2 Concentration Studies and Optimization of Electroless Copper Deposition on Bulk Silicon

After confirmation that electroless copper plating only occurred on exposed silicon surfaces, the structure and surface adhesion of the electrolessly deposited copper films was probed when electroless plating solution conditions were varied. The purpose behind this investigation is to optimize electroless deposition solution conditions to produce high quality copper films, as well as potentially examine the role some solution components play in the deposition process. The concentration of each solution component was varied independently as all other components were held constant, and information was obtained via photographs of the deposition solutions as well as the copper-coated sample wafers, optical images, and UV-Vis spectra analysis.

Figure 3.3-a,b shows an initial study where a bare silicon (100) wafer was exposed for one minute to an electroless copper plating solution with only 0.27 M NH_4F and 0.13 M $CuSO_4$, which dissolves in solution to produce solvated Cu^{2+} ions. In both the photograph and optical images in (a) and (b), it is evident that a copper film was deposited on the bulk silicon wafer. Normal silicon bare

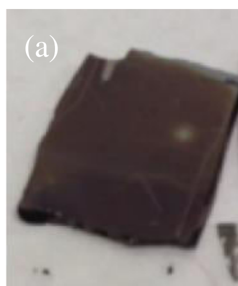


Figure 3.3. (a) Photo of silicon wafer after 1 minute exposure to copper plating solution with 0.27 M NH_4F and 0.13 M Cu^{2+}. (b) Optical image of same wafer from part (a).

silicon substrates visibly appear grey in color, but the substrate surface has changed to a copper color in images (a) and (b). However, the surface coverage of the copper film seems to be quite nonuniform in both the photograph and optical images. Variation in copper color, as well as cracks and nonuniform formations are especially visible in the optical image. To solve the issue of nonuniform deposition, sodium tartrate and ascorbic acid were added to the deposition solution, since they have been shown to increase the uniformity and copper adhesion to the silicon surface during deposition.[19,29] The ascorbic acid is believed to act as a hydrogen scavenger to quench hydrogen produced at the silicon surface during electroless copper plating, which is believed to produced deformities in the deposited copper films. The sodium tartrate chelates copper ions to reduce the electroless copper deposition rate and inhibit the production of stress-induced deformations in the copper film.

The results of sodium tartrate and ascorbic acid addition to the copper plating solution are shown in Figure 3.4. A bare silicon (100) wafer was again exposed to an electroless copper deposition solution of 0.27 M NH_4F and 0.13 M $CuSO_4$ for one minute, but the solution also included 19 mM sodium tartrate and 14 mM ascorbic acid. From the photograph of the resulting wafer surface in (a) and the optical image of the substrate surface in (b), it is clear the copper has deposited on the silicon surface in a much more uniform manner with the presence of tartrate and ascorbic acid species in relation to when they are absent from the electroless plating solution. In particular, there are no visible variations in color or surface

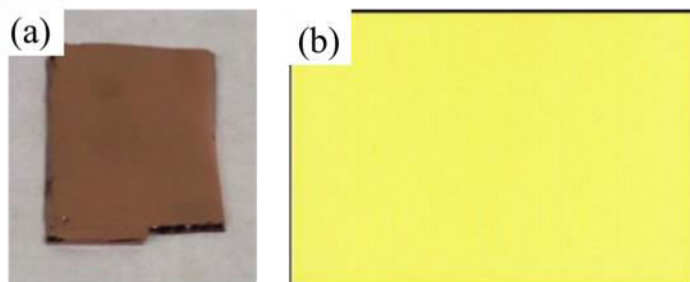


Figure 3.4. (a) Photo of silicon wafer after 1 minute exposure to copper plating solution with 0.27 M NH_4F, 0.13 M Cu^{2+}, 19 mM sodium tartrate, and 14 mM ascorbic acid. (b) Optical image of same wafer from part (a).

deformities in the optical image. Thus, the inclusion of ascorbic acid and sodium tartrate are believed to be necessary for the manufacture of electrolessly deposited copper films on bulk silicon substrates.

Once the importance of ascorbic acid and sodium tartrate in the copper deposition solution was made apparent, concentration studies were performed to investigate how the variation of copper ion concentration affected the deposited copper film, and the results are shown in Figure 3.5. The photos in part (a)-(f) show electroless copper deposition solutions with constant NH_4F, sodium tartrate, and ascorbic acid concentrations, and increasing Cu^{2+} concentrations from 0 to 0.25 M. Without any copper in solution, depicted in photo (a) of this figure, the solution appears colorless. However, as the concentration of the solution increases through images (b) – (f), the solution gains a green color, which deepens as the copper concentration is raised. Copper (II) ions are well known for their characteristic blue color in aqueous solutions. The UV-Vis spectra in part (g) of Figure 3.5 depicts a broad absorption peak between 600 and 900, with its maximum absorption at approximately 800 nm, for all the solutions containing copper ions, which confirms the solutions should be visibly exhibiting a blue color. Upon the addition of ascorbic acid into the solution, however, a small shoulder appears at around 400 nm. Absorption at this wavelength would contribute a yellow color to the electroless solution in addition to the blue color from the absorbance at around 800 nm, therefore leading to the experimentally observed green color. The green color and absorption shoulder at 400 nm are the consequence of the reduction of Cu^{2+} to Cu^{+} by the ascorbic acid, with its following chelation around Cu^{+}.[32] With an increase in the copper ion concentration, there is more copper present to be reduced and chelate with the ascorbic acid, leading to a deepening in green color. With the presence of sodium tartrate and ascorbic acid in these solutions, all the optical

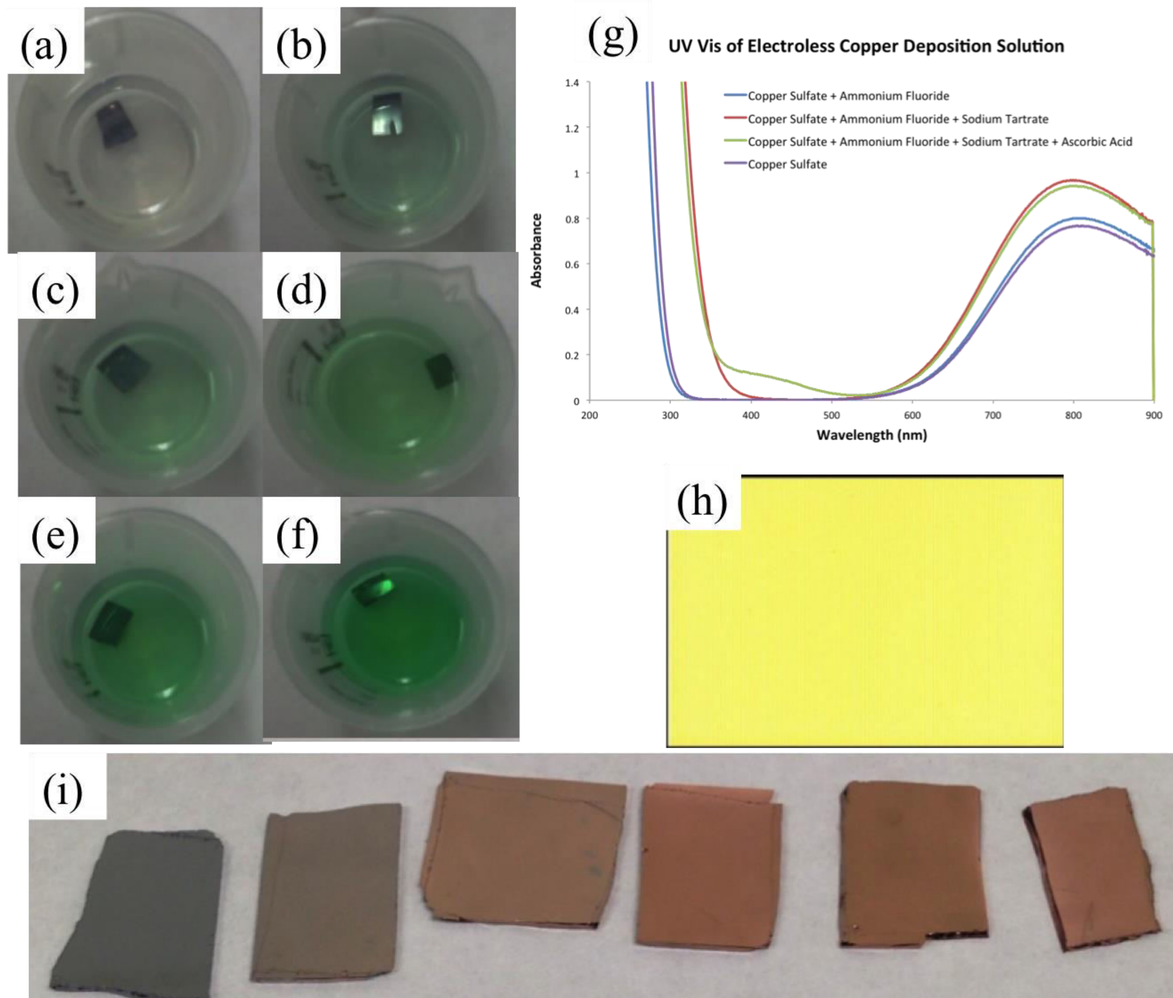


Figure 3.5. Photos of standard copper plating solutions with a range of Cu^{2+}concentrations: (a) no Cu^{2+} (b) 0.017 M (c) 0.032 M (d) 0.068 M (e) 0.13 M and (f) 0.25 M, as well as 0.27 M NH_4F, 18 mM of sodium tartrate, and 14 mM ascorbic acid. (g) UV-Vis spectra of standard electroless copper plating solution with different components. (h) Representative optical images of silicon wafer after exposure to solutions in part (a) – (f). (i) Photo of silicon wafer surfaces following copper deposition. From left to right are wafers exposed to electroless copper plating solutions with no Cu^{2+}, 0.017M, 0.032 M, 0.068 M, 0.13 M, and 0.25 M Cu^{2+}.

images of the deposited copper films demonstrated uniform copper plating, as displayed in the representative optical image in (h). Not only does the green color deepen in these electroless copper plating solutions when the concentration of copper ions is increased, but the copper color on the bulk silicon substrates deepens upon visual inspection of the sample wafers as well. The photo in Figure 3.5 part (i) shows the silicon wafers following electroless copper deposition as the copper ion concentration is raised. It is evident as the color of the wafer surface changes

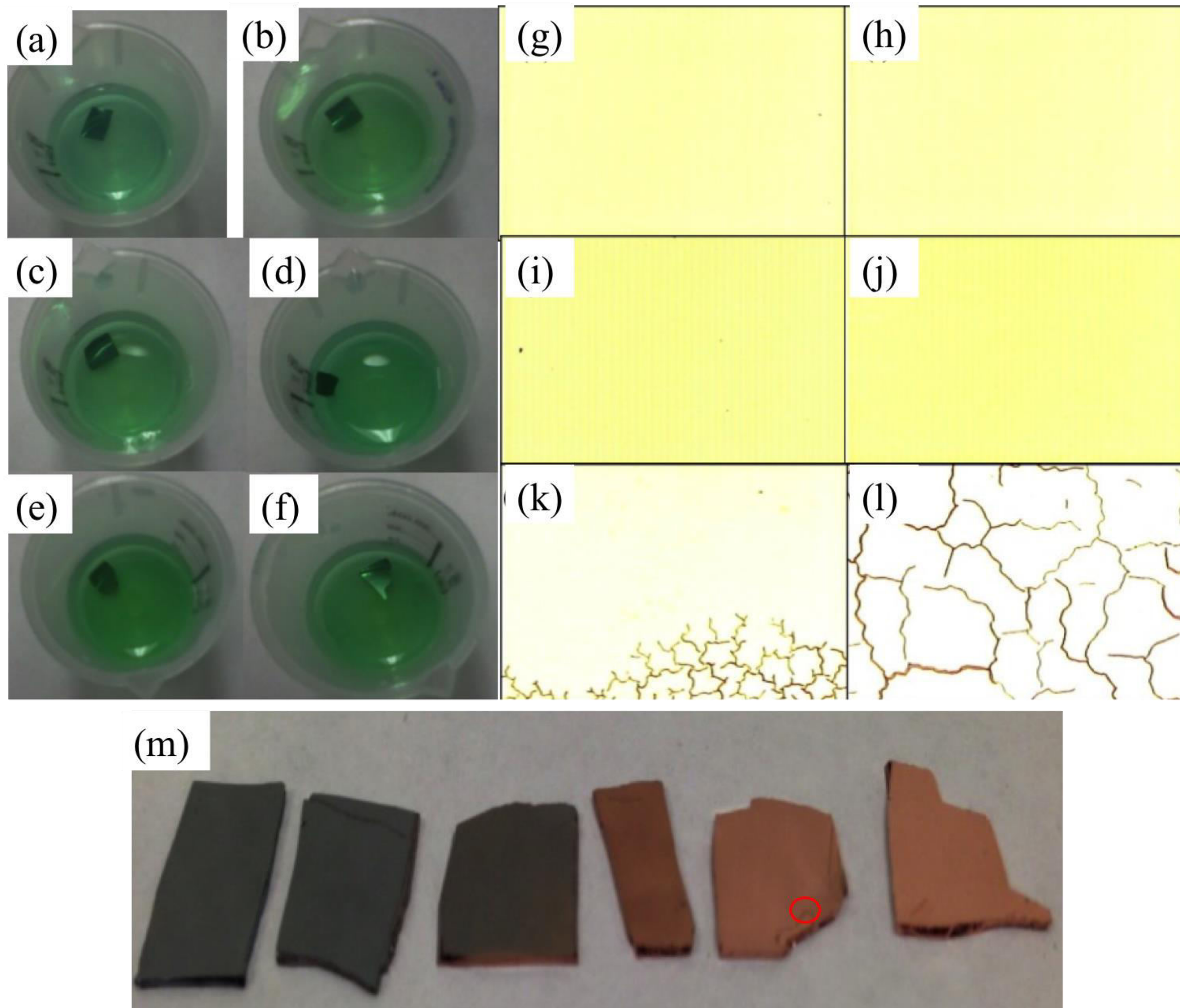


Figure 3.6. Photos of standard copper plating solutions with a range of NH_4F concentrations: (a) no NH_4F (b) 0.095M (c) 0.18 M (d) 0.28 M (e) 0.36 M and (f) 0.46M, as well as 0.13 M Cu^{2+}, 18 mM of sodium tartrate, 14 mM ascorbic acid. Optical images of silicon wafers after exposure to solutions in part (a)-(f): (g) no NH_4F (h) 0.095M (i) 0.18 M (j) 0.28 M (k) 0.36 M and (l) 0.46 M. (m) Photo of silicon wafer surfaces following copper deposition. From left to right are wafers exposed to electroless copper plating solutions with no NH_4F, 0.095M, 0.18 M, 0.28 M, 0.36 M, and 0.46 M. The red circle within this photo indicates the localized region where branch-like features were visible on the sample surface.

from silicon grey to an orange-brown characteristic of Cu^0 as the copper ion concentration is increased from left to right, likely due to the increase in copper film thickness. Thus, it can be concluded that as the copper concentration is increased, more copper is uniformly deposited on the silicon substrate. As long as the copper ion concentration is over 0.068 M, there seems to be

no dramatic difference in the structure of the copper film on the surface of the silicon substrate seeing as all the optical images and visually-inspected wafers show similar uniformity.

The influence of NH_4F concentration variation on electroless copper deposition on bulk silicon substrates is shown in Figure 3.6. Deposition solutions were made with NH_4F concentrations ranging from 0 to 0.46 M, with copper, sodium tartrate, and ascorbic acid concentrations remaining constant, and subsequently bare silicon (100) wafers were exposed to the plating solutions for one minute. There is not significant variation in the color from solutions pictured in Figure 3.6 parts (a)-(f) as the NH_4F is varied. As the ammonium fluoride concentration is increased from 0 to 0.28 M, the optical images in Figure 3.6 parts (g)-(j) illustrate uniform copper deposition without any visible localized differences in copper plating or visible structural defects. The photo in part (m) shows a uniform deepening in the copper color on the silicon surface as the ammonium fluoride concentrations is raised, similar to the same trends observed in the increase in copper ion concentration. Upon reaching 0.36 M ammonium fluoride, though, the optical images in (k) and (l) of this figure show branch-like features beginning to form on the silicon surface with deposited copper. Other researchers have observed this same phenomenon and associate it with either the addition of ascorbic acid, which significantly increases the deposition rate and leads to stress-induced restructuring of the deposited copper film, or accelerated formation of hydrogen gas in these areas. [1, 29,33] If these structures appear as a result of an increased deposition rate, it is not surprising these features appear with high concentrations of ammonium fluoride. It is directly involved in the electroless deposition reaction, and increasing its concentration would increase the deposition rate. Furthermore, it has been shown by Fukumuro *et al.*[34] that during electroless copper plating, copper thin films may undergo significant compressive stress during the initial stages of

deposition, and over time begin to experience tensile stress with thicker films. Stress in metallic films may adversely impact their electrical properties,[35] and metallic films of low stress are desirable. Thus, films containing these branch-like features are unfavorable if they may be used as an indicator for copper films experiencing significant stress during deposition growth. Roughening of the copper film can be observed visually as well as in the optical images. It is not apparent in the photo in part (m) of Figure 3.6, but on the silicon wafer exposed to a copper plating solution with 0.36 M ammonium fluoride, there is a rough patch where a roughening can be observed in comparison to an otherwise smooth surface of the copper-coated sample, which is designated by a red circle in the photo of sample wafers. This region corresponds to the location where the branch-like features appear in the optical image. Since branching seems to be localized on the surface, it is hypothesized a localized enhancement of the electroless copper deposition occurred due to regional defects in the substrate surface, resulting in these stress-induced structures that spread across the surface in a small region. The branching phenomenon is also seen on the sample exposed to the copper deposition solution with 0.46 M ammonium fluoride, but the features are spread all across the substrate surface and have larger spacing between structures in comparison to the solution with only 0.36 M ammonium fluoride. With the higher concentration of ammonium fluoride it is likely there is a high deposition rate uniformly across the silicon surface, leading to stress which is spread across the entire wafer, resulting in larger, spread out features rather than concentrated structures due a high amount of localized copper film stress. Thus, in order to avoid the presence of significant stress in the deposited copper and a significant deposition of copper within the one minute deposition time, 0.28 M was chosen as the optimal concentration for ammonium fluoride in the electroless copper deposition solution.

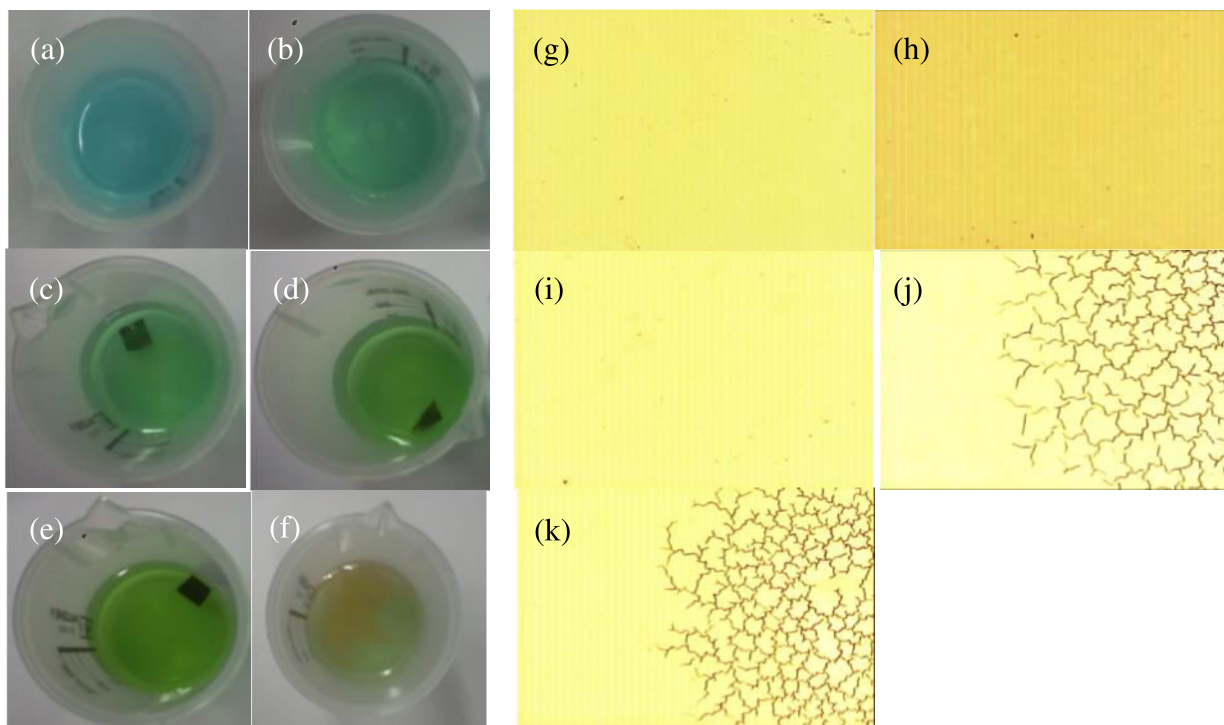


Figure 3.7. Photos of standard copper plating solutions with a range of ascorbic acid concentrations: (a) no ascorbic acid (b) 7 mM (c) 14 mM (d) 28 mM and (e) 56 mM, as well as 0.27 M NH_4F, 0.13 M Cu^{2+}, and 18 mM of sodium tartrate. (f) Copper solution immediately after removing plated wafer from deposition solution with 56mM ascorbic acid. Optical images of silicon wafer surfaces after exposure to solution from part (a) – (e): (g) no ascorbic acid (h) 7 mM (i) 14 mM (j) 28 mM and (k) 56 mM.

The results for the concentration variation in ascorbic acid are shown in Figure 3.7. As in the studies involving varying concentrations of copper ions and ammonium fluoride, bulk silicon wafers were subject to electroless copper deposition solutions with concentrations of ascorbic acid ranging from 0 mM to 56 mM, while the concentrations of all other solution components remained constant. The photos in (a) – (e) depict the visual characteristics of the electroless copper deposition solution with a range of ascorbic acid concentrations. In the photo in part (a) we see that without the addition of ascorbic acid the electroless copper deposition solution appears a clear blue color, which is consistent with the expected color from Cu^{2+} ions in solution, and the broad peak between 600 and 900 nm displayed in the previous Figure 3.5. Upon addition of ascorbic acid to the solution, the color changes to a green hue, indicative of the

reduction of Cu^{2+} ions to Cu^{+} ions from the ascorbic acid, and its further chelation around the Cu^{+} ions for stabilization.[32,36] The green color becomes more and more apparent as the initial concentration of ascorbic acid increases, and in part (e) there appears a tint of copper color in the deposition solution, indicating a further reduction to Cu^{0}. Figure 3.7 part (f) additionally shows the copper plating solution in part (e) once the silicon wafer is removed after 1 minute of exposure time, and there is a clear copper-colored precipitate developing within the solution. In order to choose the optimal concentration of ascorbic acid it is therefore imperative to keep the concentration under that which will cause Cu^{0} to precipitate out into the deposition solution while the silicon wafer is being exposed to it. This will ensure copper plates onto the silicon surface and does not precipitate out into the solution.

The optical images in Figure 3.7 part (g)-(k) and the photo in Figure 3.8 show how the structure of the copper film changes upon the increase in the ascorbic acid concentration. As the concentration increases from 0 to 14 mM, the optical images in Figure 3.7 (g) – (i) exhibit uniform plating of copper across the bulk silicon substrates. This same trend can be seen in the photo in Figure 3.8 moving from the far left wafer exposed to a copper plating solution with no ascorbic acid, to the two adjacent wafers on its right, which underwent deposition with an electroless copper plating solution containing 7 mM and 14 mM ascorbic acid. The uniformity is observed in the central regions of the wafers, and the grey-colored areas are the exposed silicon

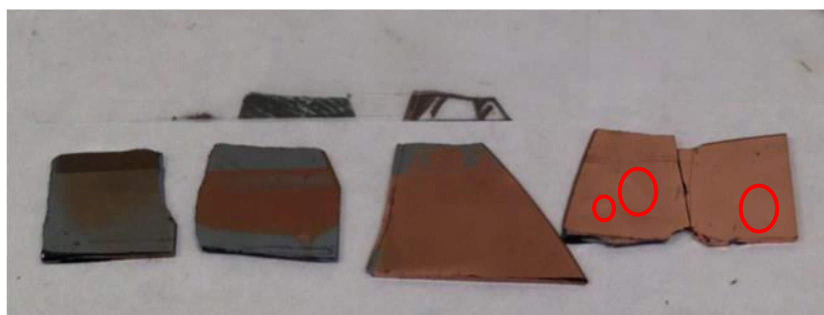


Figure 3.8. Photo of silicon wafer surfaces following copper deposition and scotch tape test. From left to right are wafers exposed to electroless copper plating solutions with no ascorbic acid, 7 mM, 14 mM, 28 mM and 56 mM ascorbic acid. See Figure 3.7 for optical images of these wafers.

resulting from film removal during the scotch tape test, which will be discussed in the following paragraph. More importantly, once the ascorbic acid concentration increased to 28 mM, the branching phenomenon begins to form, denoting a significant amount of stress in the deposited copper film during the deposition process. Not only can we observe these features in the optical images in Figure 3.7 parts (j) and (k), but these sections of branching are visibly clear to the eye by a localized surface roughening of the copper-coated substrate inside the red circles in Figure 3.8. Again as a result of these branching features, the ascorbic acid concentration should be kept under 28 mM in the copper deposition solution.

The role of the ascorbic acid species within the electroless copper plating solution becomes apparent in the photo in Figure 3.8. Adhesion of electrolessly deposited films can be qualitatively and easily examined with the scotch tape test.[37,38] If the deposited film adheres to a piece of scotch tape placed atop the film surface and comes off the substrate, it is said to have a weak adhesion to the substrate surface. The photo in Figure 3.8 demonstrates from the coated wafer on the far left that without ascorbic acid present in the plating solution, plating is relatively uneven even before the scotch tape test was implemented and minimal compared to the other wafers which were exposed to solutions with the addition of ascorbic acid. This reaffirms the importance of ascorbic acid inclusion into the electroless deposition solution for uniform copper plating. In the presence of 7 mM ascorbic acid in solution, the film becomes more uniform with a deeper copper color seen in the central regions of the sample pictured in Figure 3.8. However, upon application of the scotch tape test to the upper region of the sample wafer, the majority of the film is easily removed with scotch tape observed by the return of the grey color characteristic of bare silicon in the region where the tape was placed. The removed copper is adhered to the removed tape is depicted immediately above its corresponding sample. The removal of the

copper film denotes weak adhesion to the silicon surface when electroless copper deposition takes place in solution containing a small 7 mM concentration of ascorbic acid. When the ascorbic acid is increased to 14 mM, some copper film is removed, but the majority is removed around the edges of the wafer. In the following Figure 3.9 part (k) there is a silicon wafer exposed to similar conditions as the center silicon wafer in Figure 3.8 which undergoes the scotch tape test and does not show any sign of copper removal from the silicon surface. This behavior variation amongst coated wafers may be due to the difference in the cleanliness and surface defects of the initial silicon substrate surface. The center silicon wafer in Figure 3.8 was sitting out in air for a longer period of time after its initial cleaning compared to the wafer in Figure 3.9 part (k). It is therefore assumed the behavior of the copper film when exposed to a electroless plating solution with 14 mM ascorbic acid will demonstrate strong adhesion to the silicon surface as long as the initial silicon surface is well cleaned.

The silicon wafers exposed to deposition solutions with 28 and 56 mM ascorbic acid in Figure 3.8 show copper films with strong adhesion to the silicon surface since no noticeable trace of copper removed in the scotch tape test. However, there are regions denoted by the red circles that show the initial formation of stress-induced branching in certain areas of the substrate surface. Therefore, in order maximize adhesion of the copper film to the surface, and also to prevent significant stress formation in the deposited copper film, an optimal ascorbic acid concentration of 14 mM was chosen for the deposition solution.

The results for the concentration variation of sodium tartrate in the electroless copper plating solution are shown in Figure 3.9. The color of the deposition solutions in parts (a)-(e) show a change in color from a green to a bluish green tint as you increase the amount of sodium tartrate in the solution. It is proposed the sodium tartrate chelates the aqueous copper ions in

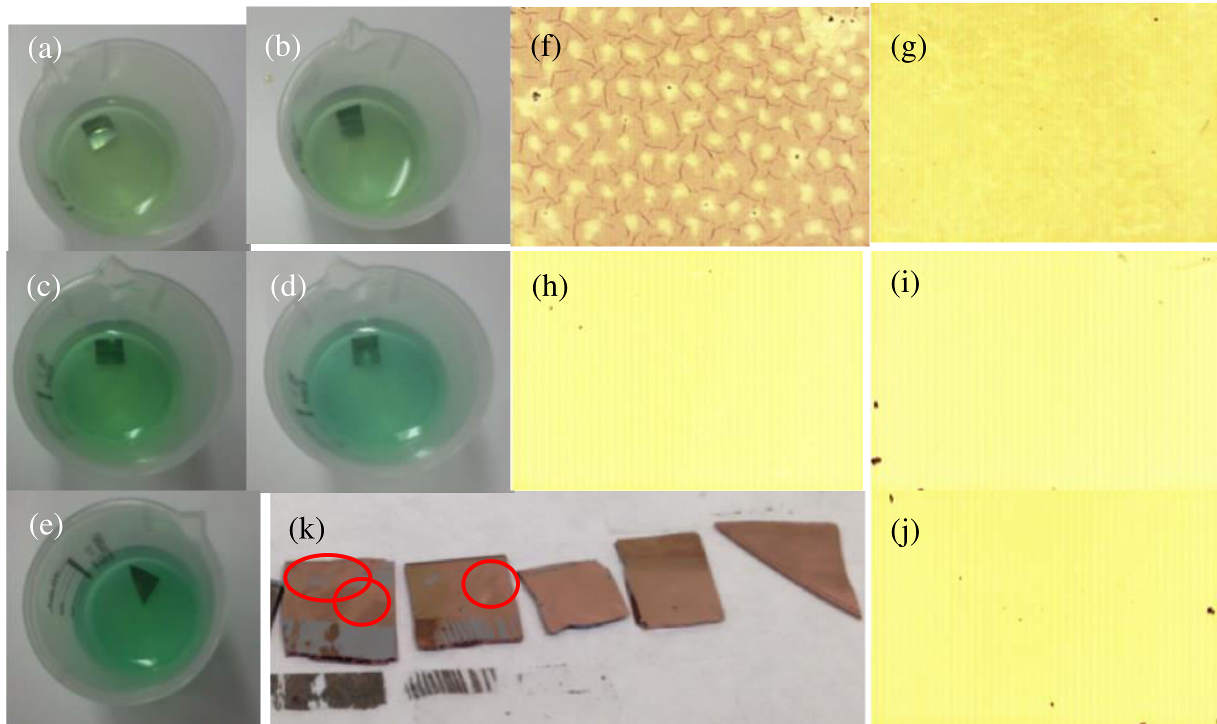


Figure 3.9. Photos of standard copper plating solutions with a range of sodium tartrate concentrations: (a) no sodium tartrate (b) 9 mM (c) 19 mM (d) 88 mM and (e) 0.45 M, as well as 0.27 M NH_4F, 0.13 M Cu^{2+}, and 14 mM ascorbic acid. Optical images of wafer surfaces after exposure to solutions from part (a) – (e): (f) no sodium tartrate (g) 9 mM (h) 19 mM (i) 88 mM and (j) 0.45 M. (k) Photo of silicon wafer surfaces following copper deposition and scotch tape test. From left to right are wafers exposed to electroless copper plating solutions with no sodium tartrate, 9 mM, 19 mM, 88 mM and 0.45 M sodium tartrate.

solution,[26] which would prevent the ascorbic acid from reducing Cu^{2+} to Cu^{+} and further chelating around the Cu^{+}, and eventually reducing the Cu^{+} to Cu^{0}. Thus, as the tartrate concentration increases, there is more tartrate present to protect the Cu^{2+} ions from being reduced to Cu^{+} and chelated by ascorbic acid, which causes the color to remain more of the characteristic blue color of Cu^{2+} ions. The optical images in Figure 3.9 parts (f)-(j) illustrate the copper-coated silicon wafer surfaces after exposure to the deposition solutions in parts (a)-(e). Without the presence of sodium tartrate within the electroless deposition solution, uneven plating as well as small branch-like features appear within the plated copper film as seen in part (f). Since these features are normally seen in the presence of ascorbic acid and high etch rates, the chelation of

the sodium tartrate is thought to chelate the copper ions in solution,[26] and thereby slow down the etch rate and prevent formation of stress-induced features on the substrate surface. A small addition of sodium tartrate to produce a concentration of 9 mM is not enough to completely overcome nonuniform copper plating as displayed in Figure 3.9 part (g). Uneven plating is also evident in the photo of the sample wafers in part (k), and striation-like structures can be seen within the red circles on the two far left samples, which correspond to wafers subject to copper plating solutions with no ascorbic acid as well as a small ascorbic acid concentration of 9 mM. However, any concentration of sodium tartrate over 19 mM seems to produce uniform copper films on the silicon substrate surface as seen in the optical images is Figure 3.9 part (h)-(j) and the three far right copper-coated silicon wafers in part (k).

Administration of the scotch tape test to the copper-coated silicon wafers formed from solutions in parts (a)-(e) of Figure 3.9 are illustrated in part (k) of the same figure. The copper films formed by deposition solutions with no sodium tartrate and 9 mM sodium tartrate detach easily from the silicon surface, seeing as most of the copper film is retained on the tape located immediately below their respective samples, demonstrating weak adhesion to the surface. The raised striation-like features in areas with stress-induced branching on the two sample surfaces likely disrupt the contact between copper and silicon at the copper-silicon interface, leading to a decrease in the film's adhesion strength. Conversely, there appears to be strong adhesion of the deposited metal onto the sample surface when the sodium tartrate concentration surpasses 19 mM, where no striation-like structures are observed. Thus, any tartrate concentration above 19 mM would be sufficient for good-quality copper film production with uniform plating and strong adhesion to the silicon surface. However, as discussed in the following chapter, the electroless copper deposition solution will be implemented for metal deposition within self-assembled

monolayers (SAM) resists for copper nanowire fabrication. The harsh conditions of the electroless deposition solution are likely to degrade the monolayer resist during prolonged exposure,[28] leading to unwanted metal deposition within resist areas. Therefore, it is important to maximize the amount of copper deposition within patterned locations for successful nanowire fabrication before the monolayer becomes destabilized and unfavorable metal deposition occurs within the SAM resist. Since sodium tartrate slows down the deposition of copper by chelating copper ions in solution, it is beneficial to minimize its concentration without compromising its role in copper film adhesion. Consequently, the concentration of 19 mM was chosen as an adequate sodium tartrate concentration for electroless copper deposition.

3.5 Conclusions

Electroless metal deposition is a fast and easy technique to deposit copper on silicon substrates, and has promise for application in metal deposition within nanoscale patterned lines, seeing as it can provide selective copper deposition on exposed silicon substrates as opposed to resist-coated samples. However, in order to create uniformly deposited copper with good adhesion to the surface, it is imperative to include additional materials into the deposition solution. The role of these additives is relatively unclear, and optimization of deposition conditions with the additives to maximize copper film adhesion and uniformity has not been previously performed. In the research presented here, optimization of an electroless plating solution was performed on bulk silicon (100) surfaces to produce copper films with maximized adhesion and uniformity, and the role of the deposition solution components examined. Silicon (100) wafers were exposed to copper plating solutions with a range of NH_4F, Cu^{2+}, ascorbic acid, and sodium tartrate concentrations, and the resulting copper films probed via optical imaging and implementation of a scotch tap test. It was found that changes in the concentration of Cu^{2+} do

not significantly influence the uniformity of deposited copper, and only impact the amount of deposited copper. Concentrations of NH_4F at 0.36 M and above create raised branch-like features across the copper films, likely due to stress created within the copper films due to increased etch rates. These features are undesirable in the films, because they indicate copper films with high levels of compressive stress, which may adversely affect the electrical properties of the deposited metal. These same features appear on sample surfaces when the ascorbic acid concentration in the deposition solution reaches 28 mM or higher. However, at lower concentrations it promotes adhesion of the electrolessly deposited copper film to the underlying silicon. Sodium tartrate is necessary to combat the formation of branch-like features within the electrolessly deposited copper films, likely because it complexes with copper ions in solution to reduce the deposition rate of copper. The optimal plating solution was chosen to be 0.27 M NH_4F, 0.13 M $CuSO_4$, 14 mM ascorbic acid, and 18 mM sodium tartrate, which produced uniform copper films with strong adhesion to the silicon surface.

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Chapter 4: Fabrication of Copper Nanowire Features

4.1 Abstract

Nanopatterning of self assembled monolayers (SAMs) via atomic force microscopy (AFM) followed by copper electroless deposition was implemented for the fabrication of copper nanowires. Many current methods to manufacture surface-attached metallic nanowires are limited by their capability to create patterned lines only down to tens of nanometers in width, their expensive equipment, or inability to create complex patterns in specific locations on a substrate surface. Nanopatterning with AFM is a promising means to create highly intricate patterns with line widths on the few nanometer scale. Electroless copper deposition is an easy and highly effective technique to deposit metal within patterned lines with such small widths. However, its capability to create metallic nanowires within these patterns with high uniformity and controllable dimensions has largely remained unexplored. Therefore, it is the main objective of this research to thoroughly examine how electroless copper deposition may change within AFM-patterned lines on organic monolayers with alterations in the resist monolayer composition, deposition solution conditions, patterned line features, and silicon substrate doping. AFM patterning was performed in three different SAM systems including an octadecyl monolayer on silicon, and octadecyldimethylchlorosilane (ODMS) on silicon oxide, and octadecyltrichlorosilane (OTS) on silicon oxide and their resist capabilities examined against the electroless copper deposition solution. In addition, solution concentrations of the individual electroless copper deposition components were varied and preliminary data collected in regards to how electroless plating changes within AFM-patterned lines. It was found that changes in solution concentration of the copper ion

source, sodium tartrate, and ascorbic acid may be used to impact nanowire height. Successful electroless deposition was demonstrated within AFM-patterned lines down to widths of 20 nm, but patterned line widths larger than a few hundred nanometers illustrated insufficient filling of the patterned line with deposited copper. This may likely be overcome, however, with changes in the electroless deposition solution conditions. Electroless copper plating on intrinsic silicon (100) showed copper plating behavior different from that of n-doped silicon (100), indicating the dopant level of the underlying substrate plays a role in electroless metal deposition within AFM-patterned lines. Lastly, copper nanowires were successfully manufactured between two gold microelectrodes, and the electrical properties examined. The nanowires exhibit behavior of nanowires with a possible copper oxide coating surrounding a reduced copper core.

4.2 Introduction

With the ever-increasing demand for nanotechnology and the ease of nanofabrication, nanowires have become a widely used resource for a variety of applications. Some of these applications include biomedical delivery,[1] magnetic cell separation,[2] biosensing,[3,4] electrochemical detection,[5,6] transparent electrodes,[7] energy storage,[4] solar cells,[8,9] nanophotonics and optoelectronics,[10,11] molecular electronics,[12,13] nanocircuits,[14,15] and host of other research areas. Kim *et al.*[1] produced silicon nanowires that could penetrate into mammalian cells, demonstrating the utility of the nanowires for potential biomedical delivery if the nanowires were coated with a target drug. Lee *et al.*[7] developed a high performance flexible transparent electrode out of long silver nanowires for application in touch-screen devices. Huang *et al.*[10] fabricated nanoscale light-emitting diodes with colors spanning the ultraviolet to near-infrared region of the

electromagnetic spectrum for integrating nanophotonic and nanoelectronic devices. Even though many advancements have been made for the successful incorporation of nanowires into several application areas, there remains a large unmet need for development of methods for incorporation of such nanowires into nanocircuitry. Many current nanoelectronic devices primarily consist of single components, such as nanotransistors[16] or nanocapacitors.[17] For the implementation of these components into nanocircuits, it is imperative to develop methods to create nanowires which may be selectively placed on surfaces to connect these individual elements, and in addition be fabricated with specific dimensions to be adaptable to fit in a variety of arrangements. Many current methods produce small nanowires with diameters of 10 nm or less, which is very desirable for nanocircuit applications, but are formed in arrays[18,19] or in bulk solution,[20] which make it difficult to manipulate single nanowires into specific configurations on a substrate surface. Either that, or the methods have high selectivity for surface placement, but exhibit diameters of several tens or hundreds of nanometers.[21,22] There is a crucial demand for a nanowire fabrication method which allows precise control of nanowire placement on a substrate surface, and additionally permits easy manipulation of the nanowire dimensions including height, width, and length. Both of these requirements must be met for successful implementation into nanoelectronic devices.

Current methods for nanowire production on substrate surfaces include photolithography,[23] electron beam lithography,[22] nano-imprint lithography,[24] dip-pen lithography,[21] oxidative lithography,[25] and nanopatterning[26] and grafting.[27] Most of these methods involve patterning of a resist-coated substrate to promote selective metal deposition in the patterned area. Photolithography uses light to pattern a resist layer

which either causes the patterned areas to become destabilized as with a positive resist, or strengthened for negative resist methods. The destabilized patterns may then be etched away leaving exposed patterned regions for further surface chemistry manipulation, or in the latter instance, the strengthened areas remain while the bulk of the resist is removed. This method is ultimately limited by the diffraction of light, and with expensive optics systems that may include extreme ultraviolet equipment, excimer lasers, or several costly lenses, has only been able to fabricate features of sizes reaching down to tens of nanometers.[28]

Electron beam lithography is a similar technique, involving a beam of electrons in place of light implemented in photolithography. Even though this method provides immense control over fabrication patterns on substrate surfaces, its beam size is limited by the repulsion experienced by the electrons within the beam. The beam may be tightly focused, and beam sizes can reach down to single nanometer size, but in order to do so the power of the beam must be lowered. Lowering the power of the beam inhibits the instrument's capability to successfully pattern strong resist coatings, which is imperative for subsequent electroless metal deposition within patterned self-assembled monolayers (SAMs) described in this work. Furthermore, manufactured nanowire utilizing this method exhibit widths on the order of tens of nanometers.[22]

Nanoimprint lithography incorporates the use of a mold or stamp to pattern substrate surfaces with large templated arrays. Stamps are normally fabricated using photolithography or electron beam lithography, so their feature sizes are limited as previously discussed. Furthermore, this technique is geared toward large-scale

development of arrays with repeating configurations instead of single nanowires with specified structure.

Dip pen-lithography includes the coating of an atomic force microscope (AFM) tip with a desired species by either dipping the tip into a solution containing the species or its neat liquid. As the tip contacts the surface, a meniscus of water is created between the tip and the sample due to ambient humidity, and the species is transferred from the tip to the surface as the tip is scanned. In order to create metallic nanowires, either the deposited species promotes copper metal reduction[21] or metallic nanoparticles can be deposited directly on the substrate surface.[29] The size of the features with this technique can reach on the order of tens of nanometers in width,[30] but oftentimes results in significantly larger widths on the order of hundreds of nanometers. [21,29] Additionally, the coated tip does not allow scanning of the targeted surface region prior to deposition, which limits the capacity to place the species in the pinpointed surface location. Furthermore, uniform deposition may prove difficult since deposition is dependent upon the coated species detaching from the AFM tip, diffusing through the water meniscus, and attaching onto the substrate surface at a constant rate while to the AFM tip is scanning.

Oxidative lithography is performed with a conductive AFM probe tip, which is able to oxidize the sample surface when a negative bias is applied between the tip and sample under the aqueous environment caused by the formation of a water meniscus between the tip and sample. This pattern may act as a template, similar to dip-pen lithography, to promote the reduction of metal ions, and lead to selective metal deposition. This method is again limited to the size of the meniscus formed between the

tip and substrate surface, and has demonstrated nanofeature fabrication on the order of tens of nanometers.[31] Furthermore, the ability to control the size of nanofeatures is highly sensitive to factors such as humidity, tip conditions, and the characteristics of the sample surface, which can make is difficult create patterns of controlled dimensions.

Nanopatterning and nanografting demonstrate a promising avenue to create nanowires with widths of 10 nm or less, seeing as the size of patterned regions is dependent primarily on the size of the AFM tip itself, and sharpened AFM tips can reach radius of curvature values as low as 1 nm.[32] Nanopatterning is performed by increasing the applied force of an AFM tip in contact mode on the sample surface, causing the tip to dig into the substrate. As the tip is scanned across the surface, it consequently removes the top layers at the sample surface, exposing underlying substrate regions beneath resist layers if the tip surpasses the depth of the resist coating. Nanografting is extremely similar, but the patterning is done in the presence of an aqueous solution containing a target replacement molecule to bind onto the exposed substrate surface. As the underlying layers of the substrate are exposed, the target analyte diffuses to the patterned region and immediately fills in the exposed area. Nanofeatures of 3-5 nm in width have been developed using this method.[33] It is for this purpose AFM-based nanopatterning was implemented in this research to develop nanoscale wires selectively places on silicon substrate surfaces coated with self-assembled monolayer resists.

Not only is it important to be able to make patterns of small dimensions in resist layers for surface-attached nanowire fabrication, but it also is necessary to be able to deposit metals successfully within the patterned regions for uniform nanowire formation without deposition within the resist-coated surface. Electroless metal deposition is an

easy method for metallic plating into small nanoscale patterns.[34] The experimental procedure includes simple exposure of the nanopatterned region to an electroless deposition solution for a specified amount of time. It does not require heating of the substrate or expensive vacuum chamber apparatus, such as with vapor deposition methods. However, the electroless plating solution may be harmful to resist regions of the sample surfaces, and destabilize the resist region over time, causing metal deposition within the resist area at defect areas as well as the nanoscale pattern.[35] Thus, it is crucial to utilize resists systems that can withstand electroless deposition solutions long enough to promote sufficient metal plating within the AFM patterns to produce adequate nanowires. Self-assembled monolayers (SAMs) are a promising tool to provide a resist monolayer for AFM patterning and subsequent electroless metal deposition. They are a molecule-thick coating on the sample surface created by simple exposure of the target substrate to a solution containing the SAM molecules. They are advantageous for resist applications for their ease of fabrication as well as their thin coatings with thickness values of a few nanometers or less. Polymeric resist coatings have inherent thicknesses that are normally much larger, and the AFM tip would need to penetrate deep into the polymer resist to expose the underlying substrate. This would lead to significant broadening of the patterned line, seeing as the AFM tip gets wider as one moves from the tip end towards its base. Patterning in thin SAMs would prevent the need for the AFM tip to dig into the surface to such a large depth, thereby lessening pattern width. There are several monolayer systems available to act as a reasonable resist layer against electroless copper deposition on silicon substrates. Alkenes, alkynes, and silane monolayers on silicon substrates present viable options seeing as vast amounts of

research have been performed on their chemical resistance capabilities.[35,36] Furthermore, the capability of the AFM to pattern through these robust monolayers has been confirmed by Headrick *et al*.[37] and Sung *et al*.[38] The ability for alkyne, alkene, and silane SAMs on silicon to withstand harsh chemical conditions in conjunction with their capacity to be adequately patterned with AFM shows great potential for the possibility of fabricating surface-attached metallic nanowires with controllable dimensions via AFM patterning and subsequent electroless metal deposition.

AFM patterning followed by electrochemical metal deposition has been performed previously, but most involve electrodeposition of metal with an externally applied voltage to drive metal depositon.[39,40] However, Zhang *et al*.[41] has successfully shown electroless copper deposition within AFM-patterned lines made in organic monolayers on silicon substrates. Furthermore, their research included some optimization experiments of the electroless deposition solution to form uniform copper nanowires. However, their optimization experiments were very limited, and lacked a thorough understanding of how adjustments in solution conditions and patterned line characteristics may influence electroless metal plating and nanowire fabrication. In addition no characterization of the electrical properties of the manufactured nanoscale wires was performed.

It is the aim of this research to thoroughly examine how changes in the resist monolayer, solution conditions, patterned line features, and substrate doping may influence copper nanowire fabrication via AFM patterning and subsequent electroless copper deposition. First, AFM patterns were created in octadecyl SAMs on silicon, as well as octadecyltrichlorosilane (OTS) and octadecyldimethylchlorosilane (ODMS)

SAMs on silicon oxide, and their resistance capability against the electroless copper deposition solution probed. Then, the concentrations of the electroless deposition solution components were individually varied, and copper deposition with these solutions investigated within AFM-patterned lines. Through this, we were able to gather preliminary data on how changes in solution conditions may influence electroless copper deposition within AFM-patterned lines. The width and depth of AFM-patterned lines was varied as well, and the electroless copper plating within these lines of variable dimension studied. Additionally, SAMs on doped and intrinsic silicon were produced, and the electroless deposition behavior examined on bare silicon wafers as well as within AFM-patterned lines. It is the hope that with this knowledge it would be possible to control nanowire size through manipulation of these parameters as well as optimize them for creation of uniform, well-connected nanowire features. Furthermore, copper nanowires were fabricated within gold microelectrode arrays and their electrical properties examined to investigate their potential for nanoelectronics applications.

4.3 Materials and Methods

4.3.1 Nanopatterning and Electroless Copper Deposition of Octadecyl, ODMS, and OTS SAMs

Octadecyl, ODMS, and OTS Monolayer Formation

Octadecyl, ODMS, and OTS monolayers were formed on phosphorous n-doped Si (100) substrates (Resistivity: 2-6 Ω-cm, Virginia Semiconductor, Inc). Initially, silicon wafers ~1cm^2 in size were cleaned with exposure to a piranha solution (15 mL H_20_2 and 35 mL H_2SO_4) for 10 minutes, and rinsed excessively with Nanopure water (18 MΩ). For the octadecyl monolayer, wafers were then subject to a 40% NH_4F solution for 3

minutes to produce H-terminated silicon samples, and rinsed with Nanopure water. The samples were thoroughly dried with nitrogen gas, and placed in pure octadecene under bubbling nitrogen. After a 30 minute nitrogen gas purge, the octadecene was heated to 180°C with further nitrogen bubbling. After 2 hours, the samples were allowed to cool to room temperature, and the nitrogen flow stopped. Following a rinse with chloroform, acetone, and ethanol, the octadecyl SAMs on silicon were stored in atmospheric conditions. For the OTS and ODMS SAMs, following piranha cleaning, the silicon samples with native oxide were thoroughly dried with nitrogen gas and placed in 2.5 mM solutions of either octadecyltrichlorosilane (OTS) or octadecyldimethylchlorosilane in a toluene solvent. After 24 hours, the silane-coated samples were removed from the solutions in toluene, and sonicated for 30 minutes in pure toluene. Then, samples were rinsed with toluene, chloroform, acetone, and ethanol, dried with nitrogen gas, and stored in atmospheric conditions.

Octadecyl, ODMS, and OTS Monolayer Characterization, AFM Patterning, and Electroless Copper Deposition

In order to characterize the octadecyl, ODMS, and OTS SAMs, contact angles and thickness measurements were obtained with a Ramé-Hart, Inc. NRL C.A. Goniometer and Rudolph Auto EL III ellipsometer. The presented values are averages calculated from 5 or 6 sample measurements.

Additional characterization of the SAMs included collecting surface morphology data, which was performed via atomic force microscopy (AFM) with a Digital Instruments Nanoscope IIIa Multimode AFM and Nanoscope E with Lateral Force Mode.

Imaging was either performed in contact mode with silicon nitride tips (NPS, Bruker, force constant = 0.06 – 0.35 N/m) or in tapping mode with diamond-like carbon coated tips (Tap 300DLC, NanoAndMore, force constant = 40 N/m). Contact mode included deflection set points in the range of 0.5 - 1.5 V, and scan rates of 1.0 – 2.0 Hz. Parameters for tapping mode comprised of drive frequencies of approximately 300 kHz, amplitude setpoints of 0.5 – 0.8 V, and scan rates of 0.3 – 0.8 Hz.

The AFM microscopes were also implemented in contact mode to pattern the SAMs. The two AFM tips implemented for patterning included diamond-like carbon coated tips (Tap300DLC, NanoAndMore) and silicon nitride coated tip (NSC35, Mikromasch). Patterning of the SAMs was performed by increasing the deflection setpoints in the AFM Nanoscope software and scanning the sample surface. AFM-patterned line widths were controlled by adjusting the aspect ratio parameter. The force applied by the AFM tip while patterning was determined by the following equation:

$$F_n = k_n S_n I_n$$

where F_n is the normal force applied by the tip on the sample, k_n is the tip force constant, S_n in the deflection sensitivity, and I_n is the photodiode response signal, or the deflection setpoint.[42] The force constant for the diamond-like carbon coated tip (Tap300DLC) was 40 N/m, and the silicon nitride coated tip (NSC35) was 16 N/m. Deflection sensitivities were determined by the value of the contact slope in the force curve for each tip.

After patterning within the octadecyl, ODMS, and OTS SAM systems, the samples were exposed to a standard copper deposition solution containing 0.27 M NH_4F,

0.13 M $CuSO_4$, 18 mM sodium tartrate, and 14 mM ascorbic acid. The octadecyl SAM was exposed for 45 sec, the ODMS SAM for 35 sec, and the OTS SAM for 1 minute.

4.3.2 Electroless Copper Plating within AFM-Patterned Lines - Dependence on Solution Conditions and Patterned Line Characteristics

Variation of Solution Conditions with Electroless Copper Deposition within Patterned Lines

The electroless copper deposition solution conditions were changed by varying the concentrations of $CuSO_4$, sodium tartrate, and ascorbic acid, as well as varying the type of copper sulfate used in the deposition solutions. The control experiments were conducted with the optimized electroless copper deposition solution, or termed "standard plating solution" in this work, obtained from the research described in Chapter 3 of this dissertation. Then, for each experiment involving concentration change, the concentration value for one solution component was varied and the concentrations for all other components remained at the values of the standard plating solution. The effect on the electroless copper deposition within AFM-patterned lines on OTS upon solution condition changes was then investigated via AFM characterization. All solution condition studies incorporated AFM-patterning using a diamond-like carbon coated AFM tip (Tap300DLC, NanoAndMore) of OTS SAM samples on n-doped silicon (Resistivity: 2-6 Ω-cm, Virginia Semiconductor, Inc.). Patterned lines were of similar width and depth. After electroless copper deposition, the patterned line regions were then topographically mapped by contact mode AFM, whose imaging conditions are described in section 3.3.1 of this chapter.

The following paragraph describes details regarding concentration variation of the deposition solution components with subsequent electroless deposition with AFM-patterned lines. Two AFM-patterned OTS samples on n-doped silicon were used in each study. One patterned sample was exposed to a standard electroless plating solution with normal concentrations for 1 minute, and the other to a solution of variable concentration of one solution component for 1 minute. For the $CuSO_4$ study, one patterned sample was exposed to a standard electroless plating solution (0.27 M NH_4F, 0.13 M $CuSO_4 \bullet 5H_20$ (Sigma Aldrich),18 mM sodium tartrate, and 14 mM ascorbic acid) and the other exposed to a solution containing a doubled concentration of $CuSO_4$ (0.27 M NH_4F, 0.26 M $CuSO_4 \bullet 5H_20$ (Sigma Aldrich),18 mM sodium tartrate, and 14 mM ascorbic acid). For the sodium tartrate concentration variation, one patterned sample was exposed to a standard electroless plating solution (0.27 M NH_4F, 0.13 M $CuSO_4$ (old storage in lab),18 mM sodium tartrate, and 14 mM ascorbic acid) and the other exposed to a solution containing no sodium tartrate (0.27 M NH_4F, 0.26 M 0.13 M $CuSO_4$ (old storage in lab), and 14 mM ascorbic acid). Lastly, the ascorbic acid concentration changed from 14 mM in a standard copper deposition solution (0.27 M NH_4F, 0.13 M $CuSO_4$ (old storage in lab),18 mM sodium tartrate, and 14 mM ascorbic acid) for one patterned sample to 42 mM in the second deposition solution (0.27 M NH_4F, 0.13 M $CuSO_4$ (old storage in lab),18 mM sodium tartrate, and 42 mM ascorbic acid).

The variation of solution conditions also involved changing the copper sulfate source used in the electroless copper deposition solution. Three types of copper sulfate sources were implemented to investigate how differences in the source of copper sulfate may influence electroless copper deposition within AFM-patterned lines. The primary

source incorporated in a majority of electroless copper deposition studies was anhydrous copper sulfate purchased at least 5 years prior to a significant portion of the electroless deposition studies presented in this work. The two other copper sulfate sources were newly purchased $CuSO_4{\bullet}5H_20$ (Sigma Aldrich) and anhydrous $CuSO_4$ (Sigma Aldrich). Three OTS samples on n-doped silicon (Resistivity: 2-6 Ω-cm, Virginia Semiconductor, Inc.) were patterned with the AFM to produce lines of similar width and depth. Following patterning, the samples were exposed to a standard electroless copper deposition solution (0.27 M NH_4F, 0.13 M $CuSO_4$, 18 mM sodium tartrate, and 14 mM ascorbic acid) for one minute. The difference in molar mass was accounted for in the concentration determination of $CuSO_4$ from $CuSO_4{\bullet}5H_20$, and the old copper sulfate was assumed to be anhydrous. Contact mode AFM was used to characterize these samples, with the experimental imaging parameters described in section 3.3.1 of this chapter. Additionally, UV-Vis spectra were obtained with a Cary 300 UV-Vis Spectrometer.

Variation in Line Width and Depth with Electroless Copper Deposition within AFM-Patterned Lines

The AFM-patterned line width and depth were varied, and the subsequent electroless copper deposition on these samples probed by AFM microscopy. All patterning and imaging by AFM is described in section 3.3.1 of this chapter. OTS monolayers were formed on n-doped silicon (100) (Resistivity: 2-6 Ω-cm, Virginia Semiconductor, Inc.). Electroless copper deposition conditions were 0.27 M NH_4F, 0.13 M $CuSO_4$, 18 mM sodium tartrate, and 14 mM ascorbic acid for all of these experiments. The exposure time for electroless copper deposition was 1 minute.

Doping of Si (100) Substrate with Electroless Copper Deposition within AFM-Patterned Lines

OTS monolayers were formed on n-doped silicon (100) (Resistivity: 2-6 Ω-cm, Virginia Semiconductor, Inc.) as well as intrinsic Si (100) (Resistivity: >20,000 Ω-cm, ElCat, Inc.) All patterning and imaging by AFM is described in section 3.3.1 of this chapter. Electroless copper deposition conditions were 0.27 M NH_4F, 0.13 M $CuSO_4$, 18 mM sodium tartrate, and 14 mM ascorbic acid for all of these experiments. The deposition solution exposure time was 45 seconds.

The research including doping of the silicon substrate and its influence on electroless copper plating was also performed on bulk silicon substrates. Wafers ~ 1 cm^2 in size of intrinsic Si (100) (Resistivity: >20,000 Ω-cm, ElCat, Inc.) and n-doped Si (100) (Resistivity: 2-6 Ω-cm, Virginia Semiconductor, Inc.) were piranha cleaned for 10 minute and rinsed thoroughly with Nanopure water (18MΩ). They were then exposed to an electroless copper plating solution consisting of 0.27 M NH_4F, 0.13 M $CuSO_4$, 18 mM sodium tartrate, and 14 mM ascorbic acid for various time segments. The samples were then characterized by tapping mode AFM as described in section 3.3.1 of this chapter. Seed densities were calculated using the particle analysis in Nanoscope Software v 5.3.1.

4.3.3 Nanowire Formation within Gold Microelectrode Arrays and Resistance Measurements

Nanowire fabrication between microelectrodes in an electrode array was performed in order to characterize the electrical properties of the electrolessly deposited copper nanowires. Gold microelectrode arrays were fabricated by the Judy Wu Research Group in the Physics Department at the University of Kansas. Their fabrication on intrinsic silicon (100) (Resistivity: >20,000 Ω-cm, ElCat, Inc.) included

photolithography to deposit large parts of the electrode arrays and electron beam lithography to pattern the microelectrodes onto the substrate surface. The arrays consisted of a 10 nm thick layer of evaporated titantium with an overlying 70 nm layer of evaporated gold. The microelectrodes were developed with a 20 μm length and 2 μm width, with the distance between microelectrodes ranging from 1 – 5 μm. AFM imaging and patterning of the gold microelectrode arrays is the same as described in section 3.3.1. I-V curve measurements were obtained with a two-point probe apparatus.

To understand how bulk resistance values change with copper film thickness, copper films of varying thickness were electrolessly deposited on intrinsic silicon (100) and their electrical properties examined. Intrinsic silicon (100) wafers were placed in an electroless copper deposition solution with 0.27 M NH_4F, 0.13 M $CuSO_4$, 18 mM sodium tartrate, and 14 mM ascorbic acid for times ranging from 30 seconds to 4 minutes. They were then rinsed with Nanopure water (18 MΩ). Parafilm was used to cover approximately one half of the samples' surface area, and the uncovered regions exposed to a 1 M solution of $FeCl_3$ for approximately 30 seconds, with a subsequent rinse of Nanopure water. AFM in contact mode described in section 3.3.1 was then used to collect step height data at the edge of the dissolved copper-copper film region.

4.4 Results and Discussion

4.4.1 Nanopatterning and Electroless Copper Deposition of Octadecyl, ODMS, and OTS SAMs

Nanopatterning and electroless copper deposition for nanowire fabrication requires a robust resist coating covering the substrate surface to prevent bulk metal deposition over the entire sample. Not only does this resist need to be adequately

impervious to metallic plating, but have the capability to be patterned by scanning microscopy methods to activate localized regions for metal deposition. It is for this purpose AFM patterning and electroless copper deposition was studied for three different types of monolayers on silicon, which is an active material for electroless copper plating. The three SAMs include an octadecyl functionality on silicon, octadecyldimethylchlorosilane (ODMS) on silicon oxide, and octadecyltrichlorosilane (OTS) on silicon oxide.

Before patterning and plating, the monolayers were characterized via goniometry, ellipsometry, and AFM imaging to probe the packing structure of the molecules on the silicon substrate surfaces. The packing structure of the molecules could indicate how effective the monolayer may perform as a resist against electroless plating. The higher surface coverage and tighter packing of the SAM molecule aids in its capability to resist penetration of solution species through the monolayer to the underlying substrate.[48,49] Representative values of contact angles and monolayer thicknesses for the three monolayer systems are displayed in Table 4.1, as well as their characteristic literature values. Most contact angle and thickness measurements are close to their respective literature values. Comparing contact angle values, it can be seen the ODMS monolayer possesses a contact angle and thickness that are significantly smaller than the octadecene

Monolayer	**Contact Angle (°)**	**Lit. Contact Angle (°)**	**Thickness (Å)**	**Lit. Thickness (Å)**
Octadecene	100.1 ± 1.7	103[43]	23.9 ± 0.9	19.5[44]
ODMS	72.8 ± 1.2	65-75[45]	11.3 ± 0.5	9.2[46]
OTS	109.0 ± 1.4	112[47]	28.2 ± 0.6	26.2[46]

Table 4.1. Table of contact angle (°) and thickness (Å) values for octadecyl group on silicon, ODMS on SiO_2, and OTS on SiO_2.

and OTS SAMs. All three molecules within these SAMs contain a hydrophobic 18 carbon chain which is approximately 2.4 nm in length[46], and would thus be predicted to depict similar contact angle and thickness values if the molecules were organized in similar manners on the silicon substrate surfaces. The only SAM that shows heights greater than this value is the OTS monolayer on silicon oxide, whose increased height is most likely due to slight polymerization of the molecules at the surface, slightly increasing the thickness of the monolayer.[50] The low contact angle and thickness values for the ODMS monolayer can be attributed to the two methyl groups terminating the molecule with the silane functionality, which create steric hindrance between attached ODMS molecules on the silicon oxide surface (see Figure 4.2). The octadecene and OTS molecule do not experience such steric hindrance at the monolayer-substrate interface, and therefore are able to pack more closely to one another and increase surface coverage. It is calculated with the steric hindrance caused by the methyl groups of the ODMS molecule, the maximum possible surface coverage with this molecule is approximately half of the maximum coverage for OTS monolayers.[49] Furthermore, the measured tilt

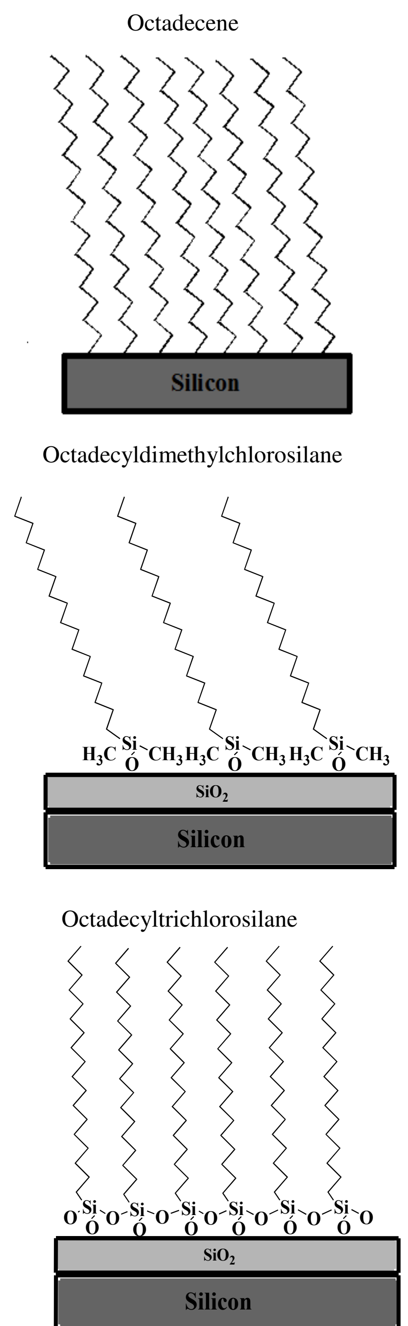


Figure 4.2. Schematic of octadecene on silicon (top), octadecyldimethylchlorosilane (ODMS) on silicon oxide (middle), and octadecyltrichlorosilane (OTS) on silicon oxide (bottom).

angles for octadecene and OTS on silicon are approximately 36°[44] and 7-8°[51] as opposed to the ODMS tilt angle which is most likely around ~45° (Note: value based upon monochloro silane with some perfluorinated moieties).[52] From the probable large tilt angle of ODMS in comparison to OTS and an octadecyl monolayer on silicon, it can be expected that the thickness of ODMS would be significantly less because the surface molecules are lying in a flatter geometry on the surface, leading to a poorly packed monolayer in comparison to OTS and octadecene. These findings are supported by Li *et al*.[49] who performed a comparison of OTS and ODMS monolayer systems on silicon oxide substrates via sum-frequency spectroscopy and contact angle measurements, and found spectroscopic behavior indicative of a high density of gauche defects in the ODMS monolayers and proposed a disordered "liquid-like" monolayer phase at the surface. However, the OTS monolayers illustrated a high amount of ordered trans configurations in the spectroscopic data, as well as signs of significant cross-linking between the terminal silane groups at the monolayer-substrate interface. It is therefore not surprising the ODMS exhibits smaller thickness and contact angle values.

Even though the SAM containing an octadecyl group on silicon displayed higher contact angle and ellipsometric thickness values in relation to ODMS on silicon oxide, these numbers were still lower than the values obtained for OTS monolayers. This may be due to the cross linking between the silane functionalities at the monolayer-substrate interface in OTS, which could help to increase the order in the SAM packing arrangement. It may also be the result of increased surface roughness of the substrate before octadecene monolayer formation due to sample preparation. Surface roughness has been linked to poor SAM quality,[53] and thus if the silicon surface was relatively

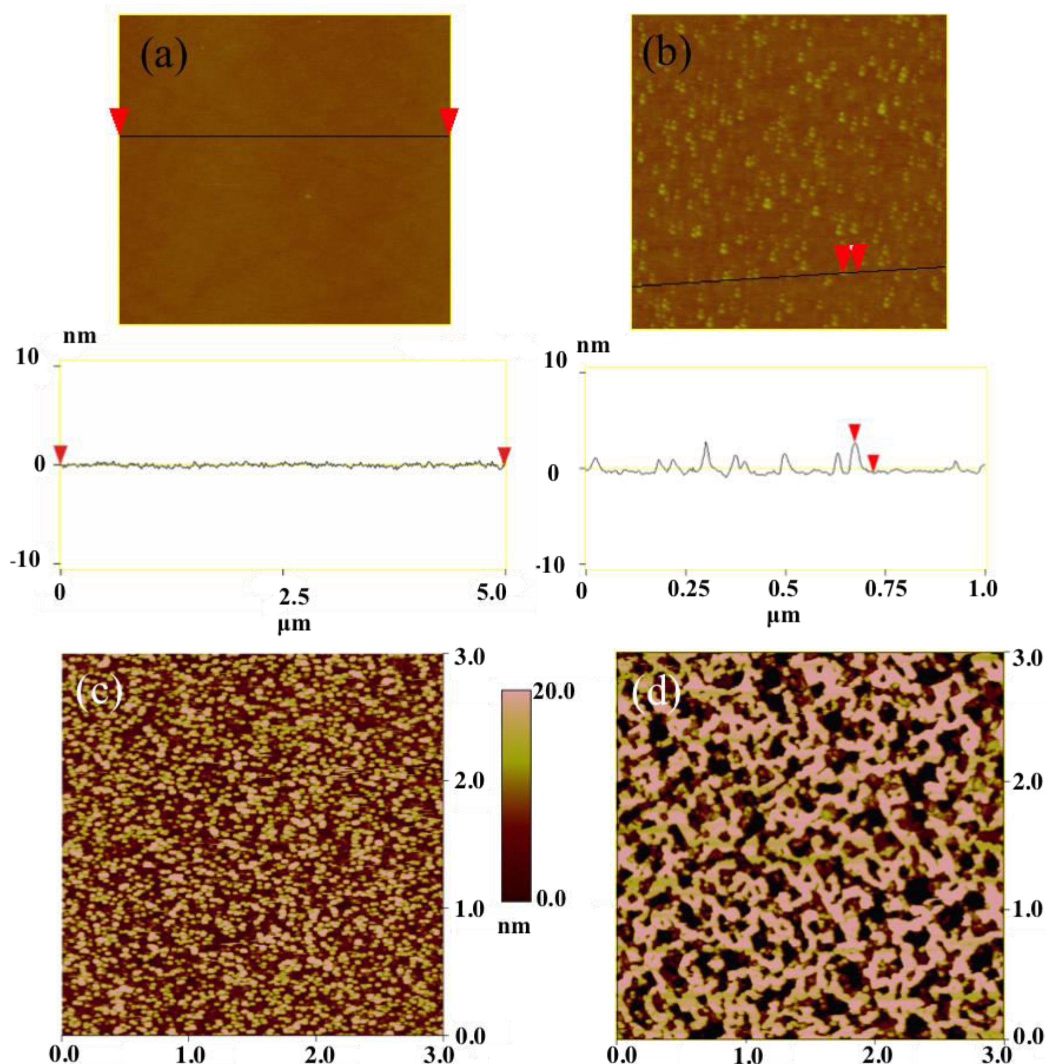


Figure 4.3. AFM images with cross sections of (a) a piranha-cleaned silicon wafer with native oxide, and (b) hydrogen-terminated silicon produced by exposure of a silicon wafer with native oxide to ammonium fluoride for 2 minutes. AFM images of hydrogen-terminated silicon produced by exposure of a silicon wafer with native oxide to ammonium fluoride for (c) 6 minutes and (d) 12 minutes.

rough before octadecene attachment, it could possibly infringe on the ability of the ODMS molecules to pack well in comparison to the OTS and ODMS monolayers, which are produced on very flat native silicon oxide.

The morphologies of the hydrogen-terminated silicon and silicon oxide before monolayer production are illustrated in Figure 4.3. As stated in the methods section 4.3.1, in order to covalently bond the octadecyl moiety to the silicon surface, a silicon

oxide surface is exposed to a 40% ammonium fluoride solution to hydrogen terminate the surface. Subsequently, the sample is heated in pure octadecene under nitrogen flow to attach the octadecyl functional group onto the silicon substrate. The initial silicon wafer with a native oxide after piranha cleaning is depicted in part (a). The cross section directly below the image illustrates a very flat surface with a surface roughness of 0.176 nm, characteristic of silicon oxide after piranha exposure. However, placing the silicon wafer with the native oxide into a solution of 40% ammonium fluoride seems to roughen the wafer surface as demonstrated by the large features that range from 1-4 nm in size across the hydrogen-terminated silicon sample in part (b) and a surface roughness increase to 0.457 nm. These surface features are similar to ones observed by Bae *et al*.[54] when exposing Si(111) to 40% ammonium fluoride for short etching times and imaging the surface morphology with a scanning tunneling microscope. Over time these small rough features shown here begin to expand to large formations across the surface, as depicted in Figure 4.3-c,d. These images show topographical maps of hydrogen-terminated silicon surfaces after a silicon wafer with a native oxide layer was exposed to 40% ammonium fluoride for 6 minutes, (c), and 12 minutes, (d). The roughening of the surface after these times further increases the roughness to 4.536 nm after a 6 minute exposure, and 9.085 nm after 12 minutes. Wade *et al*.[55] experienced similar formations when etching Si(111) with an oxygen-unpurged 40% ammonium fluoride solution, and contributed heavily pitted surfaces from dissolved oxygen which acts as an etch pit initiator. For ease of fabrication in this research, octadecyl monolayers on silicon were formed on hydrogen-terminated silicon from silicon wafers exposed to 40% ammonium fluoride for 3 minutes to remove the thin silicon oxide coating the silicon layer, but

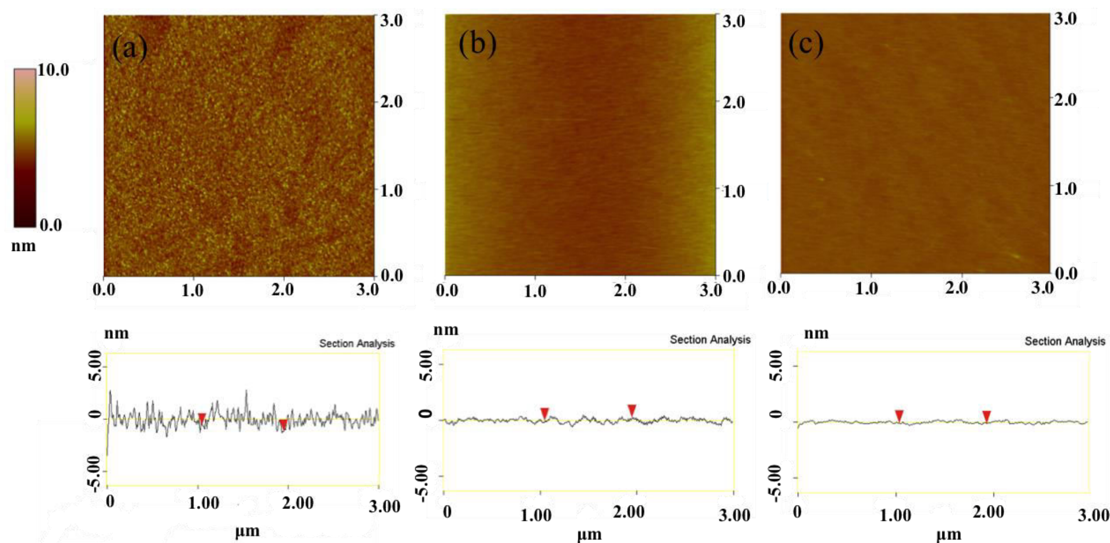


Figure 4.4. AFM images with cross sections of (a) an octadecyl SAM on silicon, (b) an ODMS SAM on silicon oxide, and (c) an OTS SAM on silicon oxide.

prevent large pit formation and significant roughening of the surface before octadecyl SAM formation.

The resulting morphology of the octadecyl SAM on silicon is illustrated in part (a) of Figure 4.4, as well as the surface morphology of the ODMS SAM (b) and OTS SAM (c) on silicon oxide. The AFM cross section for the image of the octadecyl SAM confirms a surface structure which is comparatively more rough in relation to the flat lines in the cross section for the ODMS and OTS silane monolayers on silicon oxide, and the roughness is calculated to be approximately 0.9 nm. It is likely this results partially from the rough surface of the hydrogen-terminated silicon before octadecyl surface bonding,[53] and will most likely negatively influence the capability of the octadecyl SAM on silicon to perform adequately as a chemical resist. The OTS and ODMS monolayers demonstrate flat surfaces which mirror the underlying silicon oxide film with roughness

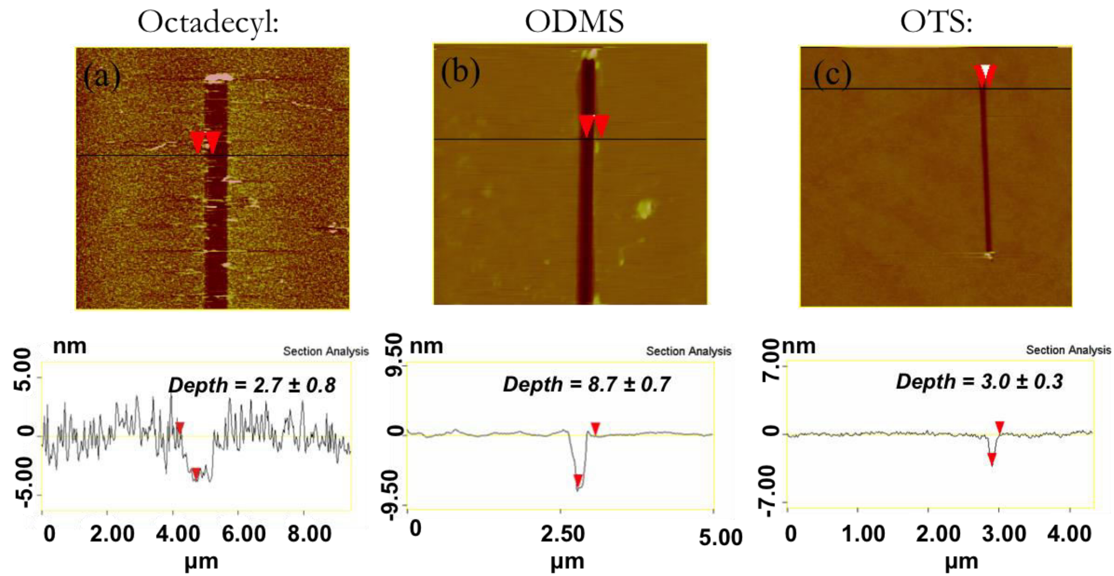


Figure 4.5. AFM images with cross sections of AFM patterned lines in (a) octadecyl SAM, (b) ODMS SAM, and (c) OTS SAM.

values of 0.167 nm and 0.189 nm, demonstrating a uniformity in surface coverage without visible defects or pinholes, as some researchers have encountered in previous studies.[50] From these findings coupled with the contact angle and monolayer thickness data, it is predicted the OTS monolayer will likely function as the superior chemical resist, surpassing an octadecyl SAM on silicon or ODMS SAM due to its high contact angle and thickness reflecting highly ordered packing.

In order for the three SAMs in this work to act as chemical resists for the formation of metallic nanowires by electroless copper deposition within AFM patterned regions, it is necessary to be able to utilize the AFM tip to remove the monolayer resist in selective regions to expose the active plating silicon substrate underlying the monolayer systems. Diamond-like carbon coated tips and silicon nitride coated tips were utilized for AFM patterning due to their high force constants (40 N/m, 14 N/m) that permit

application of high force on the substrate surface, as well as their robust nature to withstand harsh patterning conditions.[56] Applied forces here ranged from approximately 600 nN to 4300 nN. The capability for the AFM to create patterns within the SAM monolayer resists is illustrated by the AFM images and cross sections in Figure 4.5. The thin dark lines down the center of each image indicate a region of greater depth where a substantial force was applied with the AFM and scanned, demonstrating the AFM tip can pattern down into the substrate surface. From the cross section and depth values for the AFM etches in the octadecyl SAM (2.7±0.8 nm), ODMS SAM (8.7±0.7 nm), and OTS SAM (3.0±0.3 nm), it is clear the tip penetrated past the monolayer films (thickness: octadecyl SAM – 2.39±0.09 nm, ODMS SAM – 1.13±0.05 nm, OTS SAM – 2.82±0.6 nm) to the underlying silicon substrate. The depths of the AFM-etched patterns range from slightly past the monolayer for the octadecyl SAM and OTS SAM, and deep into the silicon substrate for the ODMS SAM. Patterning with the AFM tip is very sensitive to condition parameters such as the wear of the tip, scan speed, force applied, and monolayer/substrate defects.[37,56] The applied force, tip wear, and monolayer defects were variable when patterning these three monolayers with the AFM. Even though the depth of the etches is dependent upon all these parameters which may be difficult to control or effectively reproduce, most importantly these AFM images display the ability of the AFM to selectively expose the silicon substrate underneath the SAMs in localized areas for potential electroless metal deposition.

After AFM patterning, the samples with the AFM-etched lines were exposed to an electroless copper plating solution containing 0.13 M $CuSO_4$, 0.27 M NH_4F, 18 mM sodium tartrate, and 14 mM ascorbic acid. The ability for the electroless deposition

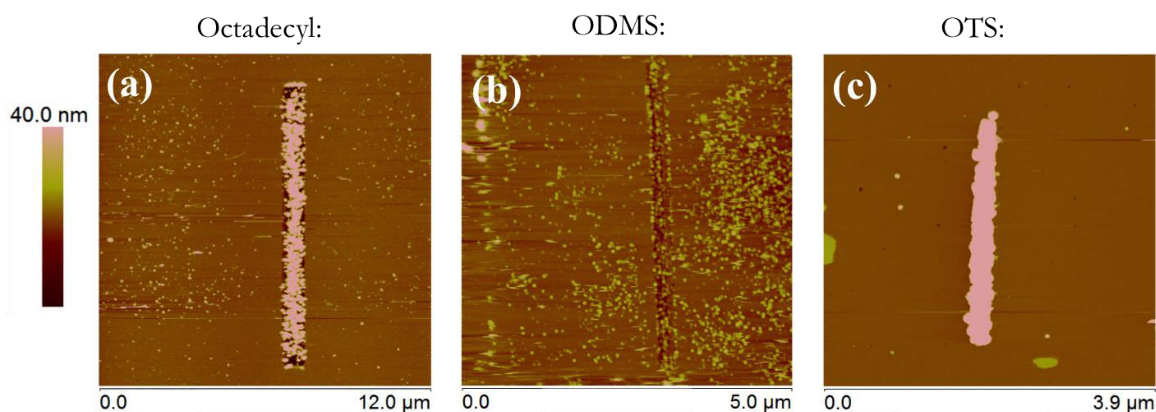


Figure 4.6. AFM images after AFM patterning and copper electroless deposition with a solution of 0.13 M $CuSO_4$, 0.27 M NH_4F, 18 mM sodium tartrate, and 14 mM ascorbic acid in (a) octadecyl SAM on silicon, (b) ODMS SAM on SiO_2, and (c) OTS SAM on SiO_2.

solution to selectively plate copper on exposed silicon surfaces is discussed in section 3.2 in Chapter 3. The exposure time for the octadecyl monolayer, ODMS SAM, and OTS SAM were 45 seconds, 35 seconds, and 1 minute. The exposure times were different due to the fact each monolayer exhibited different resistance capabilities to copper electroless plating, thus plating times were adjusted to prevent significant copper deposition within resist areas, which would make it difficult to obtain AFM images of the AFM-patterned areas. The variation in surface morphology of substrates after this deposition is illustrated in Figure 4.6. There appears to be preferential plating within the patterned region of the octadecyl SAM on silicon shown in image (a), with a majority of the raised features attributed to copper deposition residing within the AFM-etched area. However, a significant amount of small seeds with raised height above the SAM seem to have nucleated within the resist region, suggestive of solution penetration through the octadecyl monolayer with subsequent copper deposition in these areas. This penetration most likely happens at defect sites. Nucleation of silver from an electroless metal deposition solution has been used before to characterize the defect density of silane

monolayers.[35] Comparatively, there seems to be significantly less copper deposition within the patterned line on the ODMS monolayer in part (b), as the density of the nucleated seeds appears to be similar throughout the region within the patterned line and the surrounding resist area. This implies poor resistance to the harsh conditions of the electroless plating solution, and that deposition happens simultaneously within the patterned region and the surface with the SAM-coated resist. The copper deposition within the OTS pattern in Figure 4.6-c appears to be comparably specific to within the AFM-etched region, as the dark color of the deep etch is now brightly colored, representing a large increase in height to about 150 nm, and only a few copper seeds appear in the OTS resist region. Not only does most of the copper deposition happen within the patterned line, but also the copper seems to be deposited in a more uniform structure in relation to the small dispersed seeds displayed within the etched line of the octadecyl SAM. This most likely is the result of the longer one-minute exposure time of the OTS monolayer to the electroless deposition time compared to the 45-second time for the octadecyl SAM, which would allow the copper seeds to grow larger and aggregate into a more uniform formation. It should be noted the presence of a few copper seeds in the OTS resist region show the monolayer is not impervious to solution penetration and metal deposition. Longer exposure times of the OTS monolayer to the deposition solution do demonstrate increased copper plating within the unpatterned resist region. However, the OTS monolayer does provide a means to slow down the penetration and metal nucleation process enough to allow for sufficient deposition in AFM patterned regions to create a relatively uniform nanowire feature.

The ability to resist copper seed nucleation even with a more prolonged exposure time to the electroless metal deposition solution makes it evident the OTS monolayer is the best choice as a chemical resist. This is not surprising considering its higher thickness and contact angle values, which signify highly ordered packing of the OTS molecules on the substrate surface to withstand solution penetration. It is the most promising for successful copper nanowire formation via electroless plating, and the SAM implemented in the remainder of the research described in this chapter.

4.4.2 Electroless Copper Plating within AFM-Patterned Lines - Dependence on Solution Conditions and Patterned Line Characteristics

Now that it has been established that the OTS functionality on silicon oxide demonstrates the best resistance to the electroless copper deposition solution, and the production of nanowires by selective copper deposition within an AFM-patterned is possible, it is the focus of this research to be able to control the dimensions and features of the nanowires through manipulation of the electroless copper deposition components as well as the AFM patterning procedure. In order to use these nanowires for a variety of applications, especially electronics and nanodevices of precise size, it is important to be able to control the lateral size and height of the wires in addition to selectively placing the nanowires in the desired location on the substrate surface. It is for this purpose the electroless deposition of copper within AFM-patterned lines was investigated upon altering solution conditions, the patterned line dimensions, as well as the type of silicon of silicon substrate.

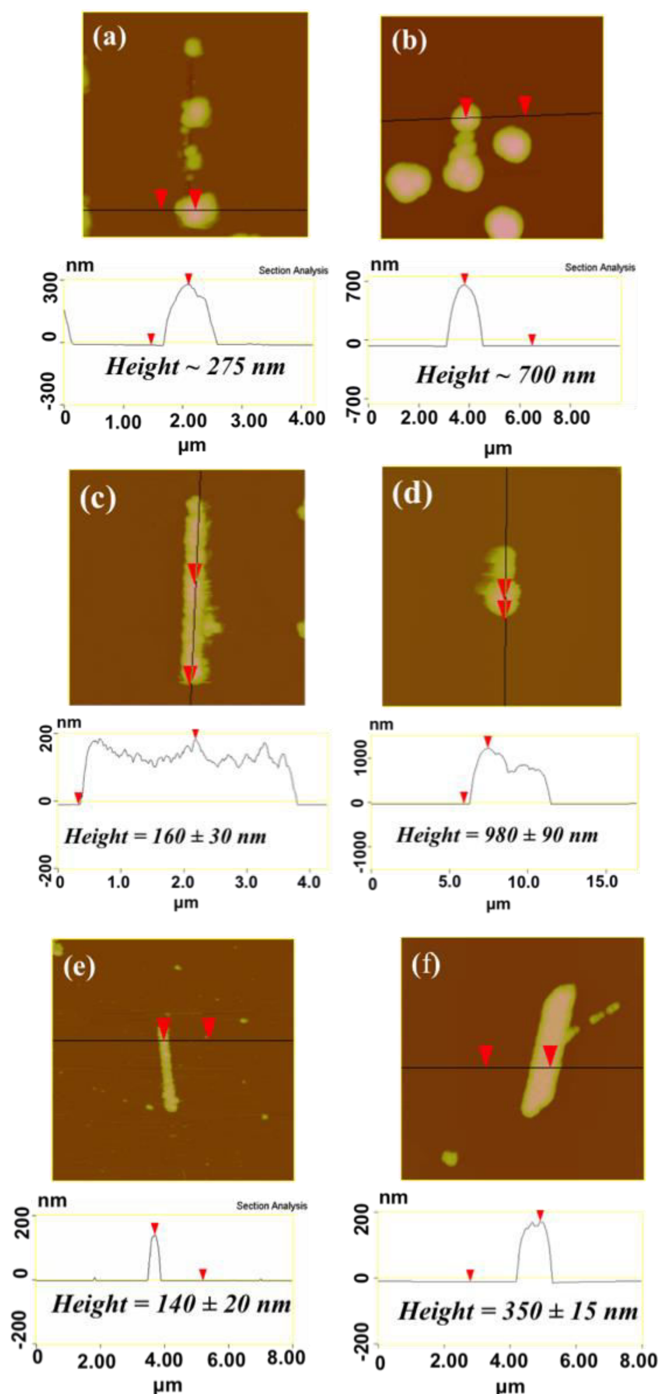


Figure 4.7. AFM images and cross sections of electrolessly deposited copper into AFM patterned lines upon varying solution concentrations. The copper sulfate concentration in a standard plating solution was changed from (a) 0.13 M $CuSO_4$ to (b) 0.26 M $CuSO_4$. The sodium tartrate concentration in a standard plating solution was changed from (c) 18 mM to (d) 0 mM. The ascorbic acid concentration in a standard plating solution was changed from (e) 14 mM to (f) 42 mM.

Solution conditions were altered by varying concentrations of the copper sulfate, sodium tartrate, and ascorbic acid within the electroless plating solution, and the subsequent influence on nanowire dimensions investigated by AFM. It should be noted the electroless plating took place for a 1-minute deposition time within AFM-patterned lines of similar lengths, widths, and depths, as well as similar silicon substrate doping and crystal lattice orientation, to discount deposition variations resulting from these factors. The results from solution concentration changes are depicted in Figure 4.7. In part (a) of this figure, which displays an AFM-patterned line after exposure to a standard plating

solution, the height of the deposited copper features reaches approximately 275 nm, with a small number of large seeds sparsely dispersed along the patterned line. The heterogeneity of the deposition is most likely a consequence of the type of copper sulfate implemented in the electroless copper deposition solution for this particular experiment involving variation in copper sulfate concentration, which will be discussed later. The other two experiments involving the change in concentration of ascorbic acid and sodium tartrate utilize a different copper sulfate source. More importantly, though, as the copper sulfate concentration is doubled, the height of the deposited metal increases by more than a factor of two as seen in Figure 4.7-b. Clearly as the copper sulfate concentration changes, so does the amount of copper deposited within the AFM-patterned line. Additionally, changes in the sodium tartrate concentration demonstrate the capability to influence the dimensions of the fabricated nanowire as observed in parts (c) and (d) of Figure 4.7. Without the addition of sodium tartrate within the deposition solution, the plated metal reaches heights of around 980 ± 90 nm (image (d)) within the AFM-patterned area, far surpassing the height of 160 ± 30 nm (image (c)) when a concentration of 18 mM of sodium tartrate is present in the solution. This is no surprise considering sodium tartrate is believed to complex with copper ions in solution to prevent copper reduction and precipitation within the bulk solution, as well as slow down the deposition rate to relieve compressive stress within electrolessly deposited metal films.[57,58] Lastly, there additionally seems to be a significant change in the copper nanowire height upon change of the ascorbic acid concentration. Increasing the ascorbic acid concentration to 42 mM (f) from 14 mM (e) present in a standard plating solution changes the height of deposited metal from around 150 nm to about 350 nm. The ascorbic acid is considered to

aid in adhesion of the copper film,[57,59] and it was previously discussed in section 3.4 of Chapter 3 that ascorbic acid can increase the deposition rate and induce significant stress into electrolessly deposited copper films. The copper sulfate, sodium tartrate, and ascorbic acid all directly influence the amount of copper ions available for reduction at the silicon surface. The copper sulfate is the source of copper ions, sodium tartrate acts as a chelator to bind free copper ions, and ascorbic acid facilitates the reduction of Cu^{2+} to Cu^{+}, as well as chelates these ions. An increased number of available copper ions in the vicinity of the AFM-patterned line would likely lead to a larger amount of copper reduced within the pattern, resulting in the formation of larger-sized features after copper deposition. The effect of a wide range of copper sulfate, sodium tartrate, and ascorbic acid concentrations was not investigated here, and the illustrated results demonstrate preliminary data. Even though concentration effects over a large range is not depicted, it has still been shown it is possible to change the height of the fabricated copper nanowires by variation of the copper sulfate, tartrate, and ascorbic acid concentrations within the electroless deposition solution, which highlights the promise of concentration variation as an easy means to control the features of the metallic nanowires. Future studies are to be performed to gain a better understanding of the detailed control provided by a large assortment of concentrations of copper sulfate and sodium tartrate.

As mentioned, the type of copper sulfate compound incorporated into the electroless deposition solution may also play a role in the deposition of copper on exposed silicon within AFM-patterned lines. Unexpectedly, electroless copper deposition within patterned lines in an OTS monolayer demonstrated differences depending on the source of the copper sulfate, as illustrated in Figure 4.8. Images (a) –

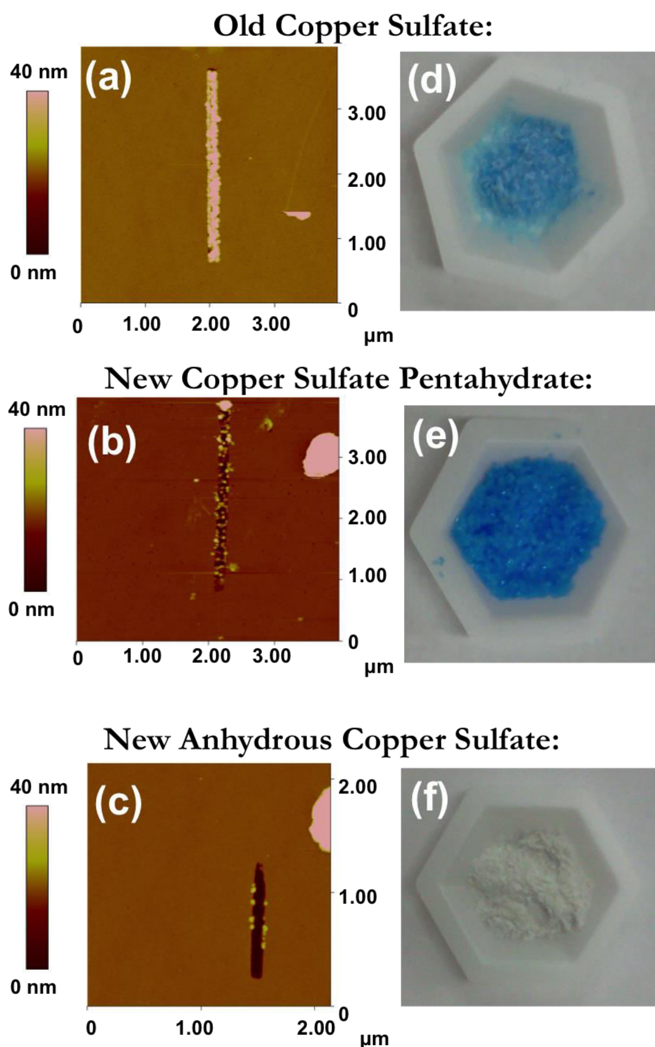


Figure 4.8. AFM images of AFM-patterned lines and 1-minute electroless copper deposition with standard plating solutions containing (a) an old storage of copper sulfate, (b) newly purchased copper sulfate pentahydrate, and (c) newly purchased anhydrous copper sulfate. Photos of the (d) old storage of copper sulfate, the (e) newly purchased copper sulfate pentahydrate, and the (f) newly purchased anhydrous copper sulfate.

(c) display AFM-patterned lines of similar dimensions after 1 minute of electroless plating solution exposure. The solution concentrations were standard with 0.13 M $CuSO_4$, 0.27 M NH_4F, 18 mM sodium tartrate, and 14 mM ascorbic acid, and the only variation was the source of the copper sulfate. The AFM image in (a) exhibits rather uniform copper plating along the AFM etched line with copper sulfate used from an old storage source, whereas (b) and (c) show small, dispersed seeds along the AFM-patterned line when newly purchased copper pentahydrate and anhydrous copper sulfate were used in the deposition

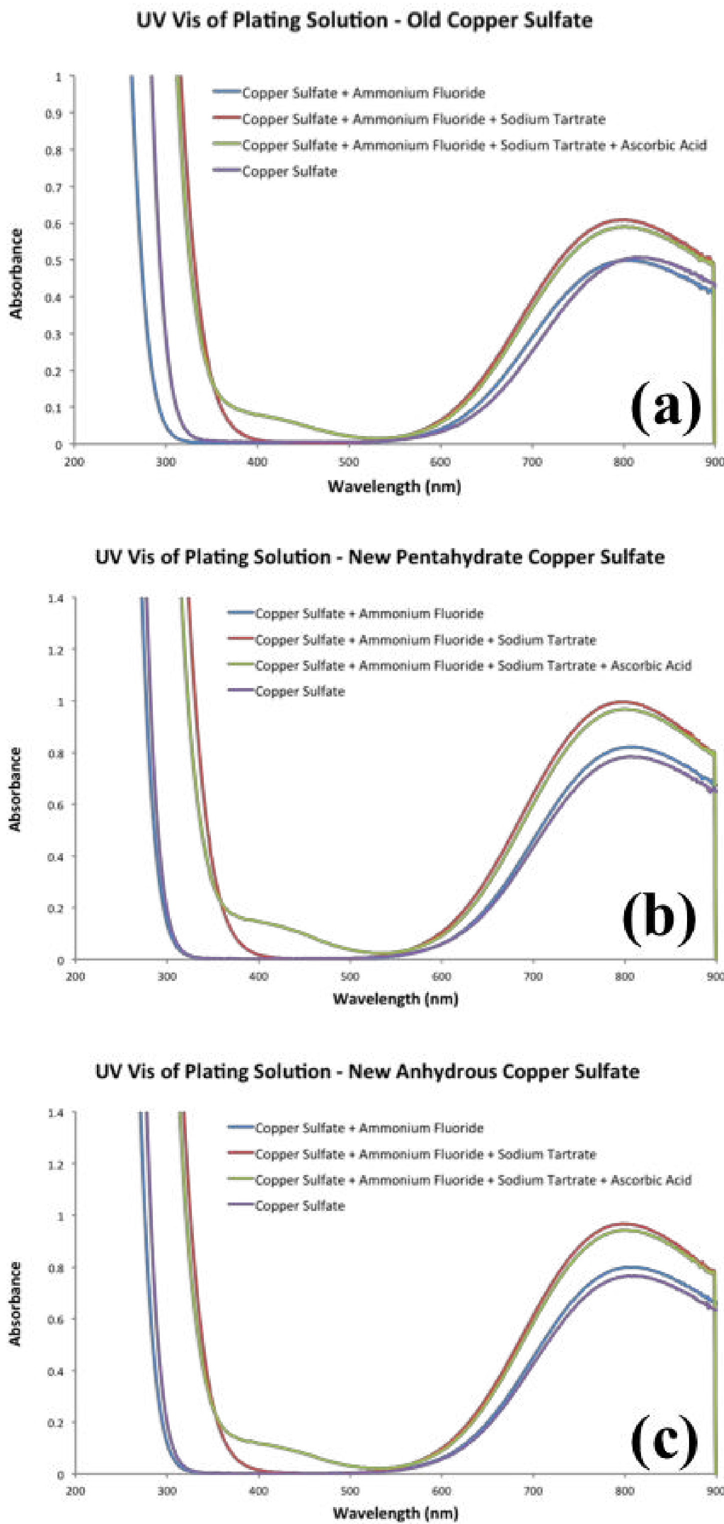


Figure 4.9. UV-Vis spectra of electroless copper plating solutions with (a) old copper sulfate, (b) newly purchased copper sulfate pentahydrate, and (c) newly purchased anhydrous copper sulfate.

solution. Copper sulfate is stable in air, and only undergoes hydration in ambient conditions. Its anhydrous form, the white powder depicted in (f), is hygroscopic and absorbs water from the atmosphere to create a deep blue copper sulfate pentahydrate,[60] as shown in (e) of this figure. The old copper sulfate source clearly depicts a hydrated mixture somewhere in between that of the anhydrous and pentahydrate compounds, with a mixture of light blue color in image (d). Seeing as all the copper sulfate compounds become dissolved in aqueous solution, it is expected the initial amount of copper sulfate hydration would not effect electroless copper

deposition behavior. Experiments were performed to account for potential concentration differences due to differences in hydration, however the same behavior is still observed. To investigate possible differences in coordination surrounding the copper ions in solution for these three compounds, the absorption spectra in the visible region were collected for these copper sulfate chemicals with and without the other electroless deposition components. The spectra do not show any detectable variations as demonstrated in Figure 4.9. All show the characteristic water-solvated Cu(II) absorption peak at approximately 800 nm[61] for the solutions containing copper sulfate, with the subsequent additions of ammonium fluoride, sodium tartrate, and ascorbic acid. Upon addition of the ascorbic acid, all three further display a shoulder formation around 400 nm.[62] Since there are no detectable differences in the absorption spectra, it is believed some type of impurity in the old, or newly purchased copper sulfates is contributing to the differences in electroless plating behavior. Previous studies have shown that trace amounts of metal in addition to copper have led to significant etching of the silicon substrate immediately surrounding nucleated copper in fluoride-containing solutions, even at ppb quantities.[63] The newly purchased copper sulfates do contain trace amounts of iron, so these variations in plating could potentially result from metallic impurities that exist in the newly acquired copper sulfate compounds, or at least differences in the amount of metallic impurities in the old stored copper sulfate in relation to the newly purchased copper sulfates. Future studies are currently underway to purify the old copper sulfate storage and perform similar electroless copper deposition experiments to confirm impurities are the true cause of the variation in copper deposition behavior within the AFM-patterned lines. Though the specific source of deposition differences for various

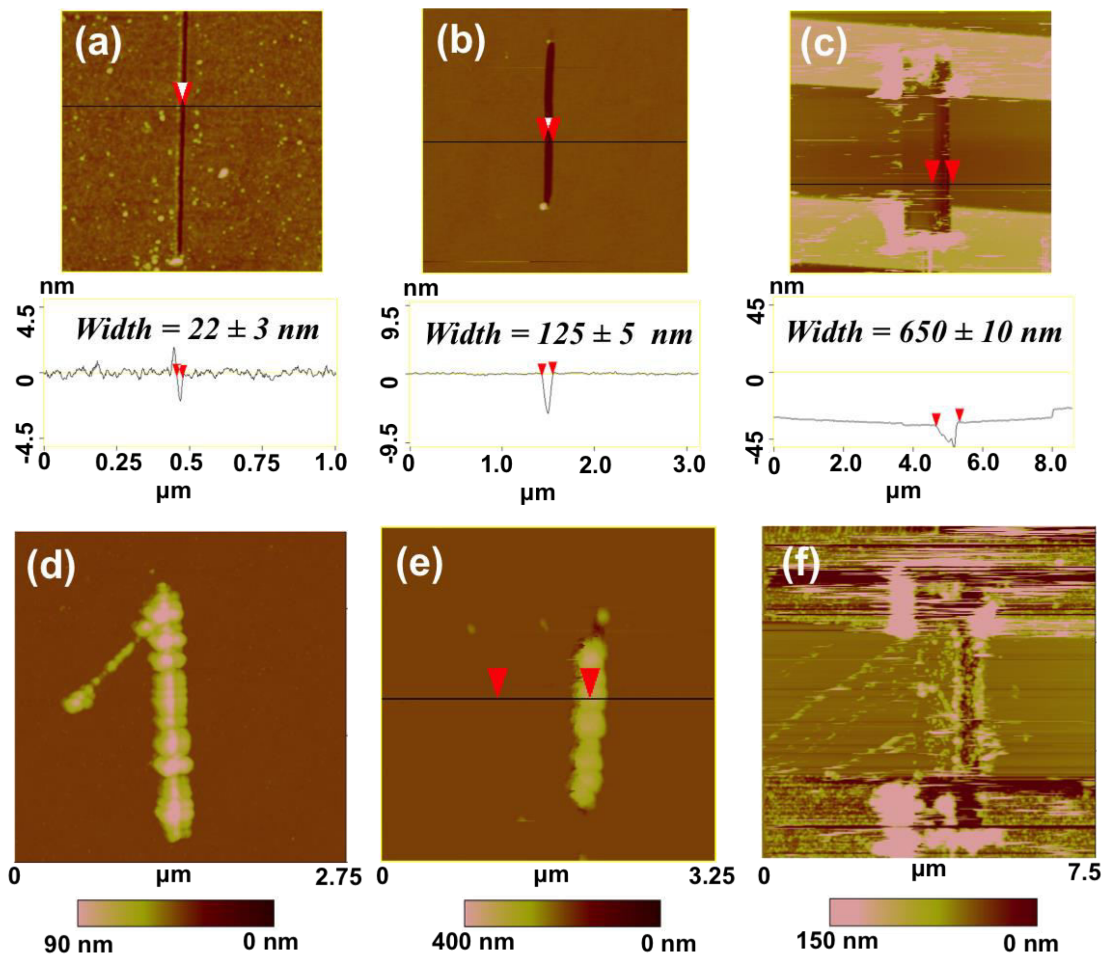


Figure 4.10. (a) – (c) AFM images and cross section of AFM-patterned lines different widths in an OTS SAM. (d) – (f) AFM images of the patterned lines in (a) – (c) after exposure to a standard electroless deposition solution for 1 minute.

copper sulfates is still undetermined, it is still evident that the type of copper sulfate utilized can influence the electroless deposition of copper within AFM-patterned lines, and the purity of the copper sulfate added to the electroless deposition solution may be a significant factor in uniform metal deposition.

Thus far only changes in solution conditions and the resulting effect on the electroless copper deposition within AFM-patterned lines has been discussed. There is also the potential for the deposition to be influenced by characteristics of the AFM-patterned lines themselves. The contact area between the AFM tip and the sample limits

the lateral dimensions of the patterned lines, and patterns within SAMs from scanning probe lithography have reported line widths down to approximately 10 nm.[27] Here, it has been possible to pattern lines down to an approximately 20 nm width, and demonstrate sufficient copper electroless plating within these lines to form copper nanowires. Figure 4.10-a shows an AFM image with accompanying cross section of a patterned line within an OTS SAM that is approximately 20 nm in width. After exposure to a standard copper electroless deposition solution, relatively uniform plating can be observed in image (d) throughout the etched lines, with its height ranging from 50 – 70 nm, and its width around 450 nm. The width increases significantly after metallic deposition, which is undesirable for the application of these nanowires into small nanoelectronic devices, but the height and width of the metallic nanofeature may be manipulated by changes in the electroless deposition solution, as been shown previously within this chapter. Increasing the patterned line width to slightly over 120 nm, as illustrated in image (b), produces similar results after electroless metal deposition, seen in Figure 4.10-e. A continuous well-formed nanowire was created with a width of approximately 500 nm and a height of about 200 nm after copper metal deposition (see Figure 4.10-e). However, further expansion of the line width may have adverse effects on the formation of a well-connected, uniform nanofabricated line after metal plating. Image (c) of Figure 4.10 displays a line patterned between two gold microelectrodes, which possesses a large width of approximately 650 nm. Upon exposure to the electroless copper plating solution, copper seeds do appear to have nucleated along the entire length of the patterned line as observed in image (f), but the seeds do not display sufficient growth to produce a well-connected metal nanowire of uniform dimensions as seen in images (d)

and (e). Evidently, AFM-patterned lines with significantly increased widths, on the order of hundreds of nanometers, do not provide enough confinement to promote significant copper seed growth to fill in the large patterned region under these plating conditions. Thus, further adjust of the plating conditions would likely permit improved seeding and growth of copper within lines of large widths, considering the previous Figure 4.7, which demonstrates copper nanowire growth with and without any sodium tartrate present in the electroless copper plating solution. With the absence of sodium tartrate in solution, very large copper features over a micron in height are observed, whereas most other copper features in this work display heights of 300 nm or less. More importantly, though, it is clearly demonstrated this method is practical for patterning wires down to approximately 20 nm followed by successful electroless copper deposition within these line patterns. Future studies are underway to develop AFM-patterned lines with smaller widths to investigate any potential limitations in electroless copper plating in patterns of decreased line width.

Another parameter of the AFM-patterned line to potentially influence electroless copper deposition would be the depth of the patterned line. In order to expose the underlying silicon surface for electroless copper plating, it is imperative to pattern past the OTS SAM, whose thickness is approximately 2.6 nm.[46] Figure 4.11-a shows an AFM image of an AFM-patterned line within an OTS monolayer with a depth of 2.5 ± 0.5 nm, which is barely through the monolayer coating on the silicon surface. It can be observed in image (d) that the depth is significant enough to permit electroless copper deposition within the AFM-patterned line. However, if the depth of the patterned line does not reach through the monolayer, as in image (b) illustrating an AFM-patterned line

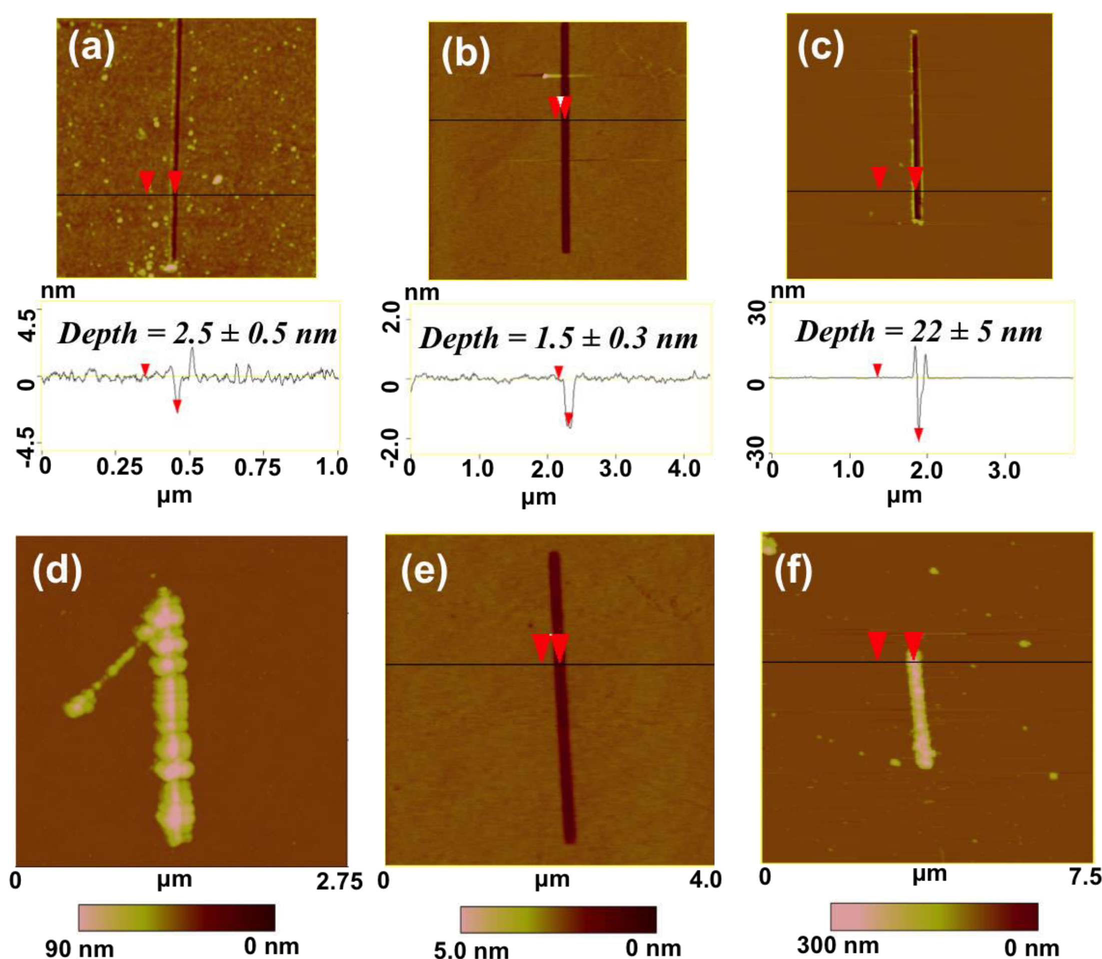
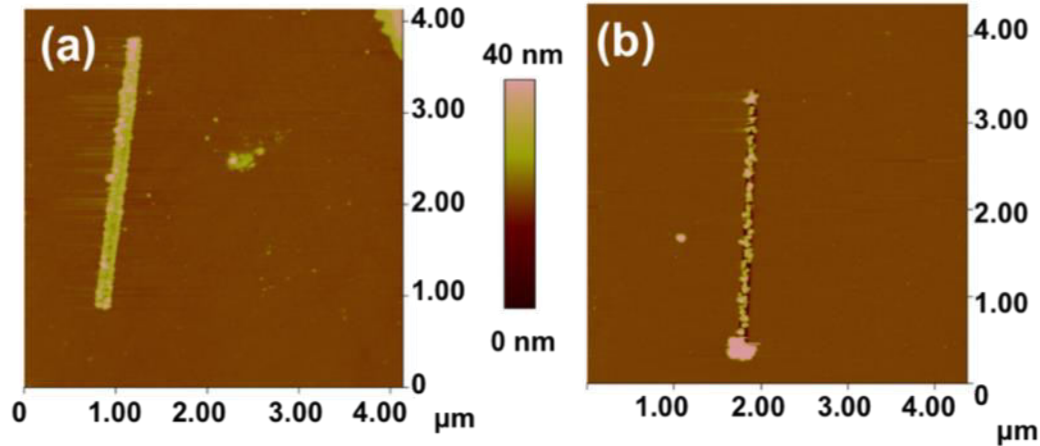


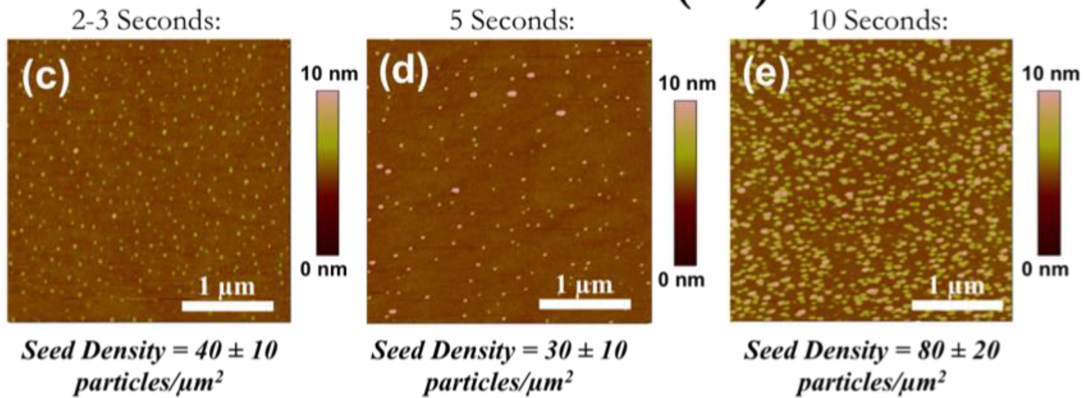
Figure 4.11. (a) – (c) AFM images and cross section of AFM-patterned lines different depths in an OTS SAM. (d) – (f) AFM images of the patterned lines in (a) – (c) after exposure to a standard electroless deposition solution for 1 minute.

possessing a 1.5 ± 0.3 nm depth, electroless copper plating does not occur within the patterned line of insufficient depth. Image (e) depicts the patterned line from (b) after exposure to the electroless copper deposition solution. No raised features from copper deposition appear and the depth of the patterned line remains consistent at 1.7 ± 0.5 nm with the depth before electroless copper plating. Evidently, partial removal of the OTS SAM does not disrupt the monolayer enough to promote copper plating within patterned lines, and the remaining components of the SAM can act as a sufficient chemical resist under these copper plating conditions. Even though it is necessary to AFM-pattern deep

enough to pass through the OTS SAM coating to allow electroless copper deposition, there seems to be no threshold on a maximum depth for successful electroless copper plating. For example, Figure 4.11-c depicts an AFM-patterned line in an OTS SAM with a large depth of 22 ± 5 nm. Image (f) confirms electroless copper deposition within this line, demonstrating uniform deposition and a well-filled line with large copper features. Clearly, it is crucial to surpass the 2.6 nm thickness of the OTS SAM for sufficient copper plating within AFM-patterned lines, but there is no limit on the depth of the AFM-pattern for effective metal deposition once this threshold is exceeded.

The dimensions of the AFM-patterned line within the OTS SAM on silicon may not be the only sample factor to impact electroless copper deposition, but the doping of the underlying silicon may affect the plating as well. A majority of previous studies utilize heavily n or p-doped silicon with low resistivity values,[59,57] and consequently most of the research detailed in this work thus far was performed with highly doped n-type silicon (2-6 Ω-cm). These doped silicon substrates with small resistivities would significantly interfere with resistance measurements of the electrolessly deposited copper nanowires. The current between the two electrodes connecting the wire could easily flow through the copper nanowire as well as the conductive doped silicon, leading to largely inaccurate conductivity values. For this reason, it is desired to develop these electrolessly deposited copper nanowires on intrinsic silicon, which contains no dopant and has large resistivity values surpassing 20,000 Ω-cm. The current resulting from an applied voltage would primarily remain within the fabricated copper nanowire on undoped silicon, seeing as the resistivity of copper is much lower than that of intrinsic silicon with a value on the order of μΩ-cm.[64,65] Furthermore, investigations in current literature have not been





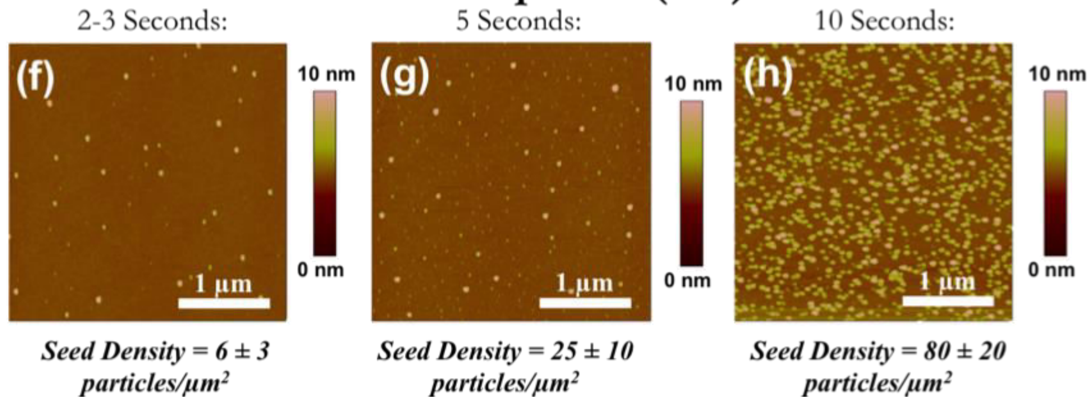


Figure 4.12 AFM images of AFM-patterned lines and 45-second electroless copper deposition with standard plating solutions on (a) intrinsic Si (100) and (b) n-doped Si (100). AFM images of bare intrinsic Si (100) wafers with native oxide after electroless copper deposition for (a) 2-3 sec, (b) 5 sec, and (c) 10 sec. AFM images of bare n-doped Si (100) wafers with native oxide after electroless copper deposition for (a) 2-3 sec, (b) 5 sec, and (c) 10 sec.

performed probing the potential influence doping of the silicon substrate may have on electroless copper deposition. In view of the fact electroless copper deposition occurs

with a transfer of electrons at the silicon-metal interface from the silicon to the copper ions for copper metal reduction,[66] there is possibility for the conductivity of the silicon substrate to play a role in facilitating this electron transfer, resulting in potential differences in electrolessly plated copper morphology.

To study this hypothesis and the effect of silicon doping on electroless copper deposition, OTS monolayers were developed on both intrinsic Si (100) and n-doped Si (100), patterned with AFM to produce lines of similar dimensions, and the patterned regions exposed to similar electroless deposition conditions for a 45 second period. The experimental results are displayed in Figure 4.12-a,b. The electroless metal deposition within the patterned line on intrinsic silicon (100) illustrates rather uniform metal seeding throughout the patterned line, with seed dimensions in the range of 80 to 100 nm, showing promise for the production of a well-connected, continuous metallic nanowire. Conversely, the plating within the patterned line on n-doped silicon shows a lower density of larger seeds, with sizes in the range of 140-160 nm in size, in relation to the nucleated metal with the AFM-pattern on instrinsic Si (100). To further investigate this variation in metallic plating behavior between these two silicon samples, electroless copper deposition was performed on bare substrates of intrinsic Si (100) and n-doped Si (100), and the metal deposition probed over a period of time. The surface morphology of deposited copper on bare intrinsic Si (100) for the first 10 seconds of deposition are depicted in Figure 4.12 parts (c) – (e), and the surface structure of nucleated copper on bare n-doped Si (100) for the same time range illustrated in images (f) – (h) of the same figure. Comparing (c) and (f), it can be seen the initial stages of copper nucleation on bare intrinsic Si (100) are different in relation to bare n-doped Si (100). The seed density

within the first few seconds of deposition is significantly higher on intrinsic Si (100) at 40 ± 10 particles/μm^2 as compared to the 6 ± 3 particles/μm^2 on n-doped Si (100), and furthermore the majority of seeds on the n-doped Si (100) are larger in size than the ones found on intrinsic Si (100) in the same time range. After approximately 5 seconds, the seeds on the bare intrinsic Si (100) begin to grow larger in image (d), and an increased amount of smaller seeds begin to appear on the bare n-doped Si (100) surface amongst large nucleated seeds in image (g). The seed densities for both the bare instrinsic Si (100) and bare n-doped Si (100) reach similar values at 30 ± 10 particles/μm^2 and 25 ± 10 particles/μm^2. The similarity in seed density is a result from the appearance of new, smaller seeds on the bare n-doped silicon surface, but there is still a noticeable difference in the distribution of seed sizes within the two AFM images in (d) and (g). It is important to note the copper seed density seems to decrease on the intrinsic Si (100) from the 2-3 second time period onto the 5-second image in (d). The data was collected on different silicon wafer samples, and the decrease is likely due to sample variability. Upon reaching the 10-second deposition time, there is no evident difference in surface morphology, seed density, or metal seed size between the deposited copper on intrinsic Si (100) in image (e) and the n-doped Si (100) in image (h). Evidently, copper nucleation on the bulk silicon substrates shows smaller seeds depositing in large density upon the intrinsic silicon, whereas the doped silicon illustrates nucleation of large copper seeds with a decreased density. However, this difference appears to diminish after 10 seconds of electroless copper plating on the bulk intrinsic and n-doped silicon. It is possible the confined, nanoscale dimensions of the AFM-patterned lines on these silicon substrates allows for this difference in copper nucleation and growth to be evident even after a 45

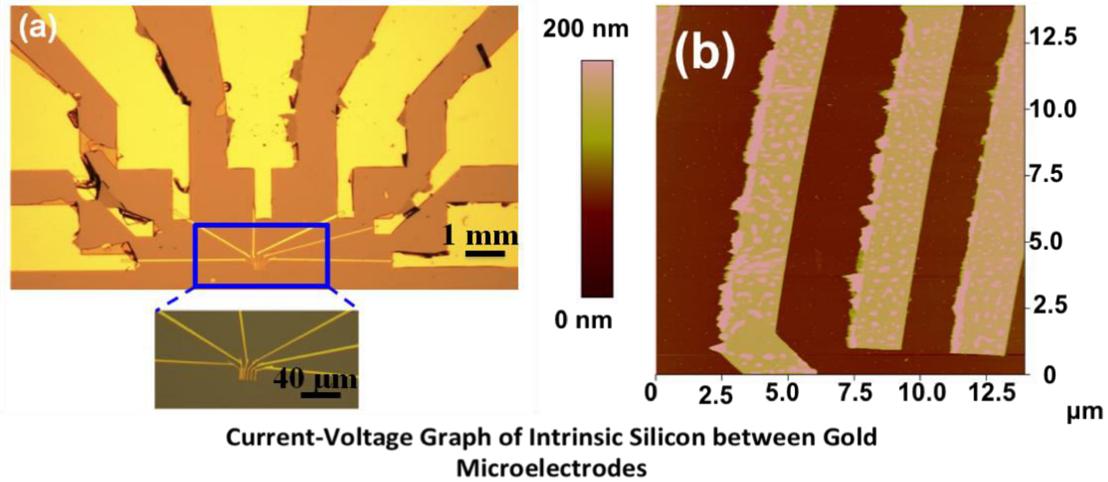
second exposure time to the copper plating solution. The contrasting behavior of metal deposition within AFM patterned lines on instrinsic Si (100) and n-doped Si (100) could potentially be the result of their conductivity differences. Yae *et al*.[67] has shown metal nucleation on silicon in HF solutions causes increased etching of the silicon immediately surrounding the nucleated metal due to the formation of a localized galvanic cell. The etching depended upon the metal, the presence of the dissolved oxygen oxidizing agent, and the photogenerated electrons and holes in the silicon. If the amount of available holes and electrons are different due to contrasting doping levels of the silicon substrate, it would most likely lead to a change in etching around the copper nucleated seeds. Consequently, the ability of the copper to nucleate and grow may alter if the silicon is being etched in a significantly different manner around the nucleated metal seeds. The more limited number of holes and electrons in the intrinsic silicon with high resistivity could possibly lower the silicon etch rate around the nucleated copper seeds in relation to the n-doped silicon, potentially allowing for more seeds to nucleate to form within the patterned region. Most importantly, it is evident a larger density of copper seeds forms within the AFM-patterned lines on intrinsic silicon in comparison to n-doped silicon, which is promising to form uniform, continuous copper nanowires on a largely insulating substrate.

In summary, it has been shown through manipulation of several factors including the electroless copper plating solution conditions, AFM-patterned line dimensions, as well as the doping of the underlying silicon substrate, one may significantly influence the characteristics of electroless copper deposition within AFM-patterned lines made on silicon substrates possessing a SAM resist coating. Changes in copper sulfate and

sodium tartrate concentrations can be used to directly affect the size of the fabricated metal nanowires, most likely because they control the amount of available free copper ions for reduction at the silicon surface. Additionally, potential metal impurities in the copper sulfate source may negatively influence the ability to uniformly deposit copper along AFM-patterned lines. The uniformity of copper deposition is also adversely impacted when the width of the AFM-patterned lines exceed values of a few hundred nanometers, however this may likely be overcome by adjustment in plating solution parameters, and in addition it is possible to successfully electrolessly deposit copper within lines reaching down to an approximate 20 nm width. The only limitation on the depth of the AFM-patterned lines seems to be a minimum threshold that needs to exceed the thickness of the OTS SAM, sufficiently exposing the silicon substrate for electroless metal deposition. Lastly, metal deposition on samples with an intrinsic Si (100) substrate seem to show increased nucleated copper seed densities in comparison to n-doped Si (100) samples, illustrating a promise for fabrication of uniform copper nanowires on insulating substrates. All these considerations may be used to develop copper nanowires on silicon surfaces of good quality and controllable dimensions.

4.4.3 Nanowire Formation within Gold Microelectrode Arrays and Resistance Measurements

In order to implement these copper metallic nanowires into electronic applications, it is imperative to characterize their electrical properties. For this reason, copper nanowires were produced within gold microelectrode arrays via AFM patterning and electroless copper deposition, and their resistance values measured by collection of current-voltage curves. Gold microelectrode arrays were manufactured in collaboration with the Judy Wu Research Group in the Physics Department at the University of Kansas.



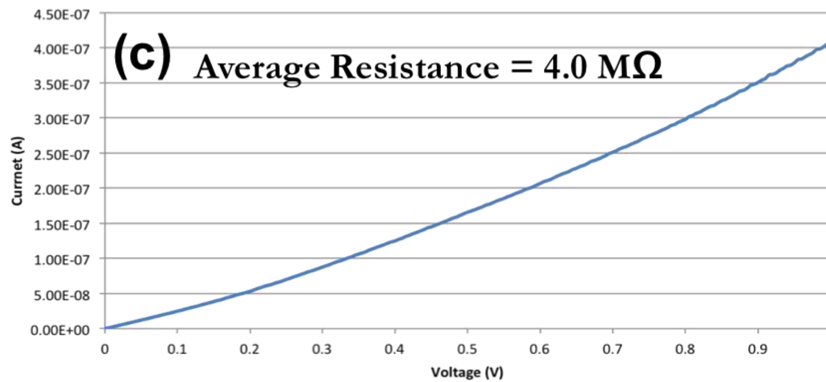


Figure 4.13. (a) Optical image of gold microelectrodes array comprised of a 10-nm thick layer of Ti and 60-nm thick layer of Au on intrinsic Si (100). (b) AFM image of gold microelectrode array. (c) I-V curve between gold microelectrodes with a 4 µm separation before nanowire fabrication.

Their fabrication included photolithography and electron beam lithography to deposit 10 nm layer of titantium followed by 70 nm of gold in microelectrode patterns onto intrinsic Si (100) with its native oxide. The microelectrodes were 20 µm in length, 2 µm in width, and the electrode separation was in the range of 1 – 5 µm. An optical image of the array is depicted in Figure 4.13-a. The large gold pads for I-V curve measurements are visible in the large-scale image, and are connected to the smaller microelectrodes evident in the zoomed-in area within the smaller accompanying optical image. The AFM image in (b) of the same figure shows the microelectrodes on a micron scale, and that the regions around the microelectrodes are relatively flat with little variation in color. To

characterize the electrical properties before nanowire fabrication between these gold microelectrodes, I-V measurements were collected and the resistance values calculated for the bare intrinsic Si (100). The resulting I-V curve for an electrode separation of 4 μm is displayed in Figure 4.13-c. The curve exhibits relatively linear behavior over the range of 0 – 1 V, which is similar to characteristics shown for intrinsic silicon nanowires,[68] and a large average resistance of 4.0 MΩ. It is supposed following copper nanowire fabrication, the resistance would drop significantly seeing as the resistivity of the intrinsic Si (100) substrate (>20,000 Ω-cm) is much larger than the resistivity of electrodeposited copper, which has resistivity values on the order of μΩ-cm.[65] It is predicted the fabricated copper nanowire would have the following dimensions: width (w) = 200 nm, length (l) = 4 μm, and thickness (t) = 200 nm. Assuming a resistivity (ρ) value of 6 μΩ-cm, the anticipated resistance value (R) after copper nanowire is approximately 6 Ω according to the equation:

$$R = \frac{\rho l}{wt}$$

The drastic resistance drop between the gold microelectrodes with a 4 μm separation from 4 MΩ before nanowire fabrication to a predicted 6 Ω following production of the copper nanowire illustrates the likelihood of measuring a resistance change if a nanowire of good quality and adequate connection is fabricated between these microelectrodes.

After the I-V measurements were obtained between the gold microelectrodes for the bare intrinsic Si (100), the sample wafer was placed in a mM OTS solution to form an OTS monolayer on the exposed silicon oxide surface. The presence of the monolayer was confirmed with a thickness measurement of 26.4 ± 0.9 nm, and a contact angle value

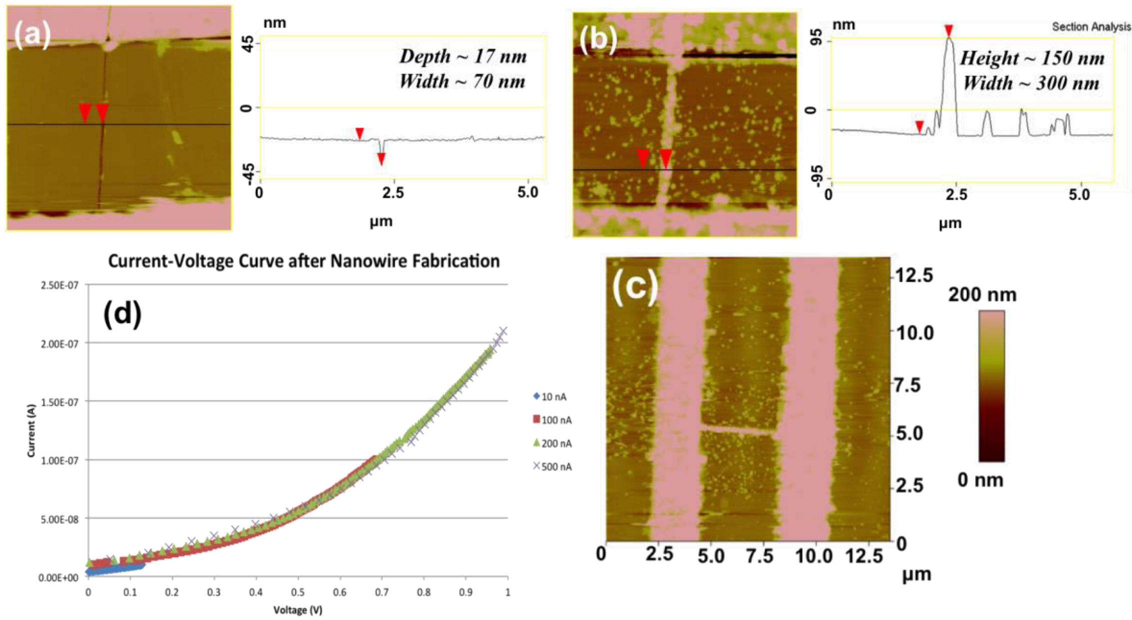


Figure 4.14. AFM image with cross section of (a) AFM-patterned line within gold microelectrode array coated with OTS SAM and (b) the patterned line after 1 minute exposure to a standard electroless copper deposition solution. (c) AFM image of the same fabricated nanowire between the gold microelectrodes separated by 4 microns. (d) I-V curve measurements of the nanowire depicted in (b) and (c).

of 110 ± 2 on the mm-size regions of the sample wafer without the gold microelectrode arrays. The AFM was then used to pattern a line between the same gold microelectrodes with a 4 µm separation, the line was exposed to a standard electroless copper plating solution for one minute, and the surface morphology characterized with AFM and resistance values determined from I-V curve measurements. The data collected is shown in Figure 4.14. Before metal deposition, it is demonstrated in part (a) of this figure that the AFM instrument can be successfully implemented to pattern lines between the gold microelectrodes, exposing silicon for selective copper deposition. The line has an approximate 17 nm depth, surpassing the thickness of the OTS monolayer, and a width of around 70 nm. Upon exposure to a standard electroless copper plating solution for one minute, it can be seen in images (b) and (c) that copper deposition occurs within the AFM-patterned line, creating metal deposition which connects the two microelectrodes.

There is some notable copper seeding in the resist region immediately surrounding the nanowire as well. Since these seeds are isolated from one another and do not form any apparent connection between the electrodes, it is believed they will not provide pathways for sufficient current to travel from one microelectrode to the other, and the bulk of the current will move through the nanowire feature. The height at around 150 nm and width at approximately 300 nm do vary from the expected dimensions mentioned previously when calculating the predicted resistance values following nanowire formation, however these changes are not significant enough to alter the expected several order of magnitude change following nanowire fabrication within the electrode array. The I-V curve in Figure 4.14-d however, does not reflect a drastic decrease in resistance values as projected, and the calculated resistances based on the graph data range from 1 – 4 MΩ. There are some key differences from the I-V curve from before and after deposition, however. The I-V in Figure 4.14-d resulting from nanowire fabrication between the gold microelectrodes displays a higher degree of exponential curvature in relation to the primarily linear I-V curve before nanowire construction (see Figure 4.13-c). These changes indicate a possible change in the I-V curve behavior due to the copper nanowire feature connecting the two gold microelectrodes, and that these high resistance values are not simply measuring the resistance of the intrinsic silicon. The current values in this voltage range are similar to those acquired for I-V curve measurements obtained by Liao *et al*. for that of a single copper oxide nanowire.[69] Copper oxide possesses a significantly larger resistivity value (about 1500 Ω-cm or greater)[70] in comparison to reduced copper, which has resistivity values in the μΩ-cm range.[65] The expected resistance value for the nanowire if it were comprised primarily of copper oxide with a resistivity (ρ) value of

1500 Ω-cm would be over 1000 MΩ implementing the equation $R = \rho\ l\ /\ w\ t$ with the following parameters: width (w) = 300 nm, length (l) = 4 μm, and thickness (t) = 150 nm. This resistance value is much more than the measured range of 1 – 4 MΩ, so if the wire is primarily copper oxide, it would probably result in I-V curve behavior which mirrors that of the intrinsic silicon. However, De Los Santos Valladares *et al.* demonstrated how the resistivity changes of thinly deposited copper films as they become oxidized. According to their research, thin films consisting of both reduced copper and copper oxide may hold resistivity values anywhere between 1×10^{-4} and 1×10^{3} Ω-cm depending on the Cu-Cu_2O composition ratio. In view of this finding, it is likely the electrolessly deposited copper here contains both copper and copper oxide. It has been well-studied copper may oxidize significantly in the presence of air,[71,72] and the prolonged exposure of the fabricated nanowire to atmospheric conditions likely oxidized part of the electrolessly plated copper to copper oxide. Lim *et al.*[72] illustrated enhanced copper oxide growth on copper surfaces with microstructures and surface defects, and thus the seed-like copper deposition within the AFM-patterned line would likely promote increased copper oxide growth. Another factor that may influence the large resistance value after copper oxide deposition would not only be the composition of the nanowire, but also its structure. In image (b) of Figure 4.14, there appear possible gaps along the nanowire feature that may not be well-connected, which could significantly hinder electron transport along the developed nanowire. From the given data, the cause of the large resistance value after nanowire fabrication between the microelectrodes remains inconclusive and could be the result of incomplete copper connection or the formation of copper oxide.

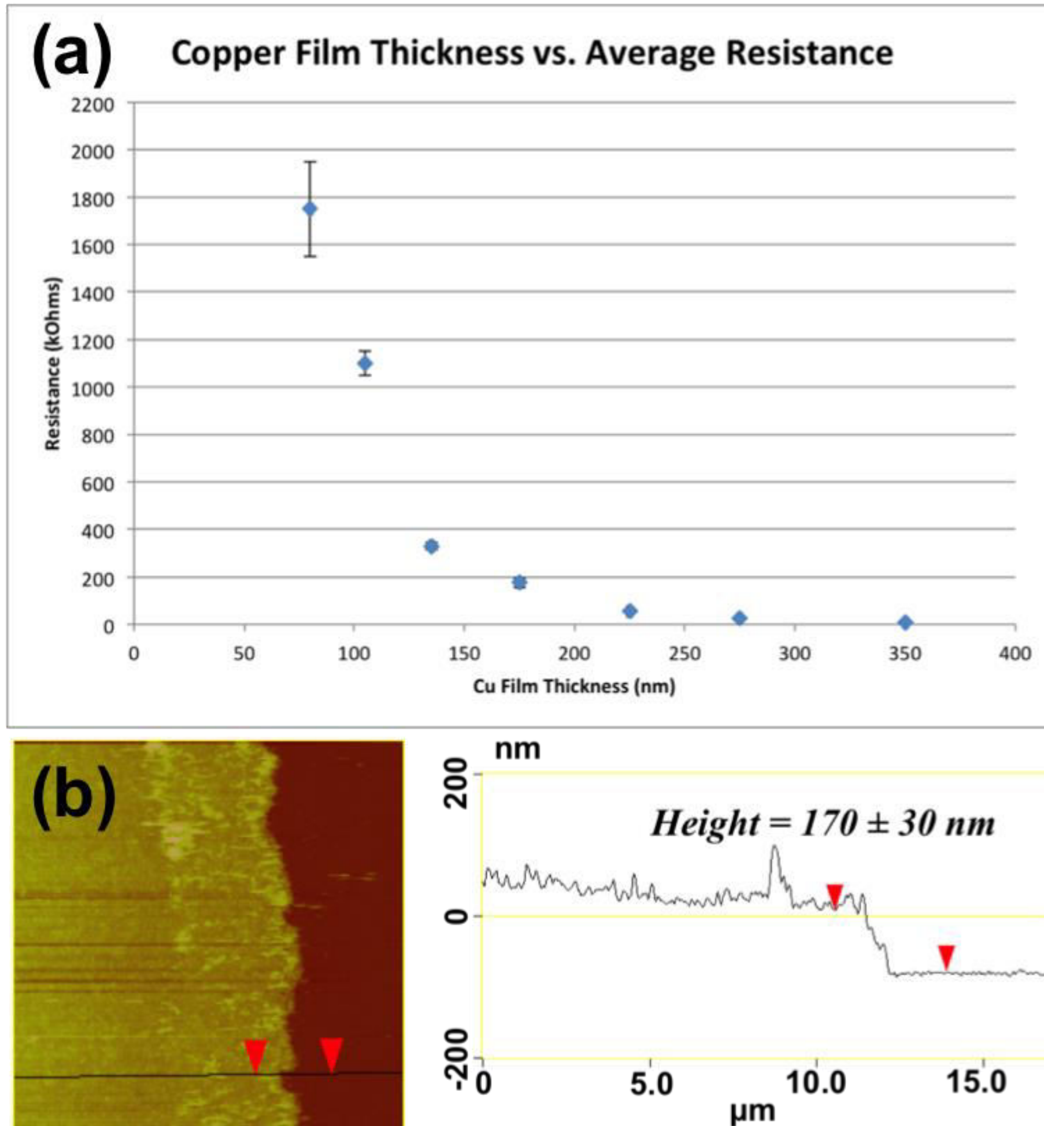


Figure 4.15. (a) Graph depicting resistance values of electrolessly deposited copper films of varying thickness. (b) AFM image and cross section of step edge from dissolving part of copper film with 0.1 M $FeCl_3$.

One way to determine if copper oxidation is behind the large resistance value following nanowire fabrication would be to develop copper nanowires with significantly larger dimensions, and determine if there is a significant change in the trend of resistivity values in relation to nanowire size. Preliminary data from experiments on bulk intrinsic silicon demonstrating how resistance values change with electrolessly deposited copper film thickness is illustrated in Figure 4.15-a. Copper was electrolessly deposited on bulk

intrinsic Si (100) to create copper films of varying thickness, and the resistance measured over a 1 cm length. Thickness values were determined by dissolving part of the copper film in a 0.1 M $FeCl_3$ solution, and measuring the resulting step edge height with AFM. An example is depicted in Figure 4.15-b. From the graph in part (a) it can be seen that copper film thicknesses smaller than about 150 nm show extreme changes in resistance with variation in thickness. However, thicker copper films of approximately 150 nm and above do not show such severe changes in resistance over the same magnitude of film thickness change. This suggests possible influence of surface copper oxides on the resistance values of deposited copper films smaller than 150 nm, significantly increasing the resistance with the enhanced presence of the oxide. However, with thicker films, the increased amount of copper in relation to the copper oxide allows for the resistance to be primarily dependent on the copper, and show smaller changes in resistance with film thickness. In order to overcome oxidation of the copper and the detrimental effect it has on resistance values of the fabricated nanowires, it may be possible to electrolessly plate other metals using this method which do not oxidize in air, such as silver or gold. Plus, their higher reduction potentials at $E^0_{Ag} = 0.779\ V_{SHE}$ and $E^0_{Au} = 1.42\ V_{SHE}$ make their plating on silicon very favorable.[66] Future studies are currently underway to examine electroless silver plating within AFM-patterned lines on silicon substrates.

It has been clearly demonstrated through AFM patterning and electroless copper deposition, it is possible to develop nanowires within gold microelectrode arrays. Resistance measurements of bare intrinsic silicon (100) between two microelectrodes demonstrate high resistance measurements, which are expected considering the high resistivity of undoped silicon. Following nanowire fabrication connecting the two

electrodes, however, does not result in a large drop in resistance as anticipated, and the resistance remains high in the range of 1 – 4 MΩ. This is likely due to oxidation of the deposited copper in air, seeing as the resistivity of copper oxide is significantly higher than reduced copper. However, it is believed only partial oxidation occurs, considering complete oxidation would likely lead to resistance values which surpass experimentally obtained values.

4.5 Conclusions

It has been demonstrated that copper nanowires can be successfully manufactured via AFM nanopatterning of organic self assembled monolayers (SAMs) followed by electroless copper deposition. Furthermore, the dimensions of the nanowire can be controlled and conditions optimized for the production of well-formed copper nanowires through potential manipulation of the resist monolayer composition, deposition solution conditions, patterned line features, and silicon substrate doping. Three different SAM systems including an octadecyl monolayer on silicon, and octadecyldimethylchlorosilane (ODMS) on silicon oxide, and octadecyltrichlorosilane (OTS) on silicon oxide were patterned with the AFM and their resist capabilities against the harsh electroless deposition solution examine. All three monolayers were able to be sufficiently patterned with the AFM to expose their underlying silicon substrates, however the OTS monolayer on silicon oxide exhibited the best capability to withstand copper metal seeding within the resist region. This is likely due to its crosslinking ability at the monolayer-silicon oxide interface, as well as its superior packing in relation to an octadecyl SAM on silicon and ODMS SAM on silicon oxide. The better packing of the OTS SAM is evident through its higher thickness and contact angle values. This packing of the OTS

molecules on the substrate surface likely aids the monolayer's capability to withstand solution penetration and metal deposition.

In addition, it has been shown that electroless copper deposition within AFM-patterned lines made on silicon substrates possessing a SAM resist coating may be manipulated through variation in solution conditions, AFM-patterned line dimensions, and the doping of the underlying silicon substrate. Changes in copper sulfate, sodium tartrate, and ascorbic acid concentrations can be used to directly influence the size of the fabricated metal nanowires. Additionally, electroless copper deposition uniformity may be negatively influenced by potential metal impurities in the copper sulfate source. Newly purchased copper sulfate did not display signs of significant copper plating within AFM-patterned lines, which could be the consequence of enhanced silicon etch rates surrounding deposited metal seeds in the presence of trace metal impurities, inhibiting sufficient metal seeding and growth.

Electroless copper deposition may also be impacted by substrate conditions, as well as solution conditions. The uniformity of copper deposition is adversely impacted when the width of the AFM-patterned lines exceed values of a few hundred nanometers, but it is probably to overcome this drawback with adjustments in plating solution conditions. More importantly, successful electroless copper deposition was shown within AFM-patterned lines in OTS SAM resists reaching down to an approximate 20 nm width. The only limitation on the depth of the AFM-patterned lines seems to be a minimum threshold determined by the thickness of the SAM resist that needs to be surpassed in order to expose the underlying silicon substrate for electroless metal deposition.

Also, electroless copper deposition on samples with an underlying intrinsic Si (100) substrate exhibit different electroless deposition behavior in relation to their n-doped silicon (100) counterpart. Intrinsic silicon (100) samples display increased nucleated copper seed densities with decreased seed size, whereas n-doped Si (100) samples show smaller densities for seed nucleation, but a larger size of seed in comparison to intrinsic silicon. This difference is likely due to the difference in electron transport at the silicon-deposition solution interface leading to a difference in silicon dissolution rates surrounding nucleated metal seeds. Most importantly, though it illustrates the promise for fabrication of uniform copper nanowires on insulating silicon substrates. All these considerations collectively demonstrate the capacity to develop copper nanowires on silicon surfaces of good quality and controllable dimensions by utilizing changes in electroless deposition solution conditions, patterned line size, and doping of the silicon substrate.

Lastly, copper nanowires were successfully fabricated between gold microelectrodes and the electrical properties probed by collection of I-V curve data. Prior to nanowire fabrication between the microelectrodes, the bare intrinsic silicon (100) had high resistance measurements, 4 MΩ for a 4 μm electrode separation, which is not surprising considering the large resistivity value of the undoped silicon sample at >20,000 Ω-cm. It was expected that following nanowire fabrication connecting the two electrodes, the resistance value would drop significantly to a value on the order of ohms. However, the experimental data did not display a significant decrease in resistance values with subsequent nanowire formation, and retained large resistance values in the range of 1 – 4 MΩ. It is believed the copper surface of the nanofabricated wire is oxidized upon

exposure in air, creating a copper oxide coating surrounding a copper core. Full oxidation of the copper is proposed not to occur, seeing as the experimentally obtained resistance values would likely mirror that of the intrinsic silicon. Future studies are currently being performed to further investigate the potential oxidation of the copper nanowire upon exposure to air, as well as the potential to electrolessly deposit other metals within AFM-patterned regions that do not exhibit the problem of oxidation in air, such as silver and gold.

4.6 References

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Chapter 5: Graphene Growth on Copper Substrates

5.1 Abstract

The manufacture of large-area graphene with high conductivity and optical transparency is imperative for its potential application as a transparent electrode in photovoltaic devices. Chemical vapor deposition of graphene on copper substrates is a promising method to produce single-layer graphene with large lateral dimensions, however current CVD methods produce graphene exhibiting inferior conductivity and transparency to other fabrication methods. Low conductivity is attributed to the increased presence of misaligned grain boundaries and point defects in these CVD graphene films. To overcome these drawbacks, there is substantial interest in understanding the role the copper substrate plays on the graphene deposition process. With this understanding it may be possible to manipulate features of the copper substrate to directly influence CVD graphene quality. For this purpose, CVD graphene was deposited on cube-textured (100) oriented copper (CTO-Cu) and polycrystalline copper, which possess vast differences in crystal face structure and grain alignment, and the

electrical and optical properties of the resulting CVD graphene examined. It was found that graphene on CTO-Cu depicted significantly higher conductivity, optical transmittance, and a lower defect density via observation of the collected Raman spectra. By a time-sequenced analysis for graphene on both of these substrates, it was found that the highly aligned grains on CTO-Cu produced aligned triangular-like features on the copper substrate surface, indicating a large restructuring of the copper surface during CVD graphene deposition. Graphene nucleates on the surface of these triangles, and a restructuring of the (100) surface occurs to a (111) lattice to promote this graphene deposition. These triangles grow in size as the graphene deposition time increases, and eventually cover the entire surface. A morphological restructuring on the graphene-coated polycrystalline copper surface is also evident, but these features do not exhibit any highly ordered shape or alignment, and the copper crystal structure underlying the deposited graphene remains fairly polycrystalline. These differences likely lead to the variation in graphene quality manufactured on these two copper substrates. Additionally, graphene growth within holes of graphene array templates was investigated as another potential means to control CVD graphene growth and orientation. Graphene nanohole arrays on insulating silicon substrates were fabricated, copper was deposited via evaporation into exposed hole regions within the nanohole arrays, and the samples exposed to CVD graphene growth conditions. Preliminary data suggests the deposited copper may accumulate at hole edges at elevated temperatures, and upon exposure to CVD graphene conditions, promote growth of graphene from the edge sites of the nanohole array inward. This research illustrates the potential to control CVD graphene

growth by copper substrate manipulation, as well as the possibility of developing CVD graphene on the surface of insulating substrates.

5.2 Introduction

Graphene is a promising material in the nanotechnology and materials science community for its mechanical robustness,[1] high electron mobility,[2,3,4] transparency,[5,6,7] chemical stability,[7,8] and flexibility to conform to various surface morphologies.[6,9] It has been instituted in several areas of research including transistors,[10] memory devices,[11,12] transparent electrodes,[13,14,15] photovoltaic devices,[16,17] sensors,[18,6,19] and energy storage devices.[20] There are several graphene fabrication methods, but the most common are mechanical exfoliation,[2,21] epitaxial growth on SiC substrates,[22,23,24] graphene oxide reduction,[25,26,27] and chemical vapor deposition.[28,14,29] Mechanical exfoliation involves the physical removal of graphene from a single crystal graphite substrate, oftentimes via scotch tape removal, and produces high quality pristine graphene limited to microscale dimensions and generally resulting in multi-layer graphene.[2,30] Epitaxial graphene production on SiC requires intense heating of the silicon carbide substrate under high vacuum or inert gas atmosphere to thermally decompose the SiC to graphene at its surface interface. This method is easy and allows for graphene development on an insulating substrate, however it normally creates multi-layer graphene[24] with potentially high concentrations of defects due to the SiC lattice mismatch with graphene,[31] and further is limited in size by the SiC substrate, which is very expensive.[31] Reduction of graphene oxide is a very diverse field implementing several different reduction methods including electrochemical,[27,32] photochemical,[33,34] thermal,[26] and chemical reduction methods.[25,35] Its advantages are experimental simplicity, cost, and the ability to create

reduced graphene sheets in solution for various applications.[36] However, the electrical conductivity of these sheets are normally several orders of magnitude smaller than pristine graphene due to incomplete reduction,[37] and these methods may further result in the production of excessive hazardous wastes from reducing agent materials.[38] Most of these processes are limited either in graphene sheet size, cost, or multiple layer formation. Chemical vapor deposition is a promising method to overcome most of these disadvantages.

The chemical vapor deposition (CVD) process to produce graphene involves thermal heating of a metallic substrate in the presence of a hydrocarbon gas under low vacuum conditions. At the surface of the metal, the hydrocarbon gas breaks down and the metal solubilizes the carbon. As the substrate is allowed to cool, carbon precipitates out of the metal and reforms at the metal surface interface as graphene. Several metals such as copper,[39] nickel,[40] cobalt,[41] iron,[42] and ruthenium,[43] have been used as substrate platforms for CVD graphene. Copper offers an advantage in the area of predominant production of single-layer graphene due to the low carbon solubility in copper,[39] also it has relatively low cost compared to some of these other metals. However, large copper foils commercially available on a cheap scale are principally polycrystalline copper with grains sizes on the order of microns and a variety of crystal orientations such as Cu (111), (100), and (110). It has been found that CVD deposition on these substrates leads to graphene with significantly lower carrier mobilities compared to pristine graphene, which are most likely the result of the formation of small misaligned grains and other point defects that obstruct charge transport in the graphene layer due to scattering.[28,44,45,46] A significant portion of these defects generate from graphene deposition on copper lattice

faces other than the (111) orientation, such as the (100) and (110) crystals, which have significantly different lattice constants than graphene. This lattice mismatch leads to substantial strain and thereby defects in the deposited graphene. Other researchers have demonstrated graphene deposited on these other crystal faces possess behavior of lower quality.[47,48] Comparatively, graphene deposition on single crystal Cu (111) surfaces produces graphene of high quality due to the single crystalline nature of the surface resulting in large aligned graphene grains, and the close lattice match of graphene with the Cu (111) orientation.[29] Unfortunately, single crystal copper samples are very expensive and do not come in large sizes. In order to utilize large-area production of graphene via chemical vapor deposition at a low cost, controlling grain boundaries and other defects, as well as understanding the deposition mechanism, is imperative for successful implementation of large graphene sheets into a variety of applications.

One promising alternative to the use of polycrystalline copper is cube-textured (100) oriented copper (CTO-Cu) foils. These copper foils undergo a special thermomechanical treament to create large-area smooth copper foils with closely aligned grains of a single crystal orientation, in this case the (100) lattice orientation.[49] Since it has been shown that graphene nucleation on the single crystal copper generates graphene with more desirable characteristics due in part to aligned grains, implementing a substrate with a single crystal face, such as CTO-Cu, with a high degree of grain alignment shows potential in influencing graphene grain alignment on a cheaper scale. The initial objective of this work is to compare the optical and electrical properties of graphene grown by chemical vapor deposition on polycrystalline copper as well as CTO-Cu to determine whether these properties can be improved through the use of oriented copper

foils such as the CTO copper. Through this research we are able to better understand how grain alignment and crystal lattice orientation of the copper substrate influence the defect density, conductivity, and optical transparency of CVD graphene.

An additional drawback to chemical vapor deposition of graphene on copper and other metallic substrates is the introduction of additional defects in the graphene as a result of transfer to dielectric materials. To incorporate CVD graphene into many research applications, the conductive graphene needs to be transferred to an insulating substrate, commonly silicon. The graphene transfer process involves a multitude of steps that may include polymer resist coating, thermal curing, metal foil dissolution, liquid suspension over the desired substrate, and solvent rinses to remove polymer resists. These steps can incorporate defects into the transferred graphene through residual polymer doping,[50] tears,[44] and wrinkles.[44] Thus, research has been conducted to form graphene directly on dielectric material surfaces such as SiO_2,[51] BN,[52] and Ge.[53] However, CVD graphene growth on these surfaces often results in defect-rich graphene with maximum flake size in the microns. All of these investigations have explored graphene epitaxy on insulating substrates vastly different than copper, but little attention has been paid to the use of metal oxide layers coating metallic substrates to promote CVD graphene deposition. The potential to produce graphene at a thin reduced copper interface atop a copper oxide insulating layer has not been thoroughly explored, and is investigated in this research.

It has been well-established graphene nucleates as seeds and grows to larger grains on clean reduced copper surfaces. However, most commercial copper foils have a native oxide layer approximately 3-5 nm thick due to atmospheric exposure to oxygen at

room temperature.[54] Since graphene chemical vapor deposition on copper is generally a low vacuum process, residual adsorbed oxygen on the substrate surface or oxygen within the CVD chamber coupled with intense heat could further promote copper oxide formation and increase this thickness. Copper foils heated to a 970°C temperature in air have been shown to develop copper oxide coatings on the scale of tens of microns.[55] Because of this, most copper foils undergo a prolonged annealing step with H_2 gas after reaching the CVD deposition temperature to rid of any copper oxide on the substrate surface before introduction of the carbon source gas for graphene formation. However, if it were possible to retain the copper oxide film and promote copper reduction in the first few atomic layers of the copper oxide surface, successful graphene epitaxy may be feasible on a mostly insulating surface with minimal effects from a nanoscale layer of reduced copper. Research has supported formation of thin reduced copper films overlying bulk copper oxide layers.[56] Potentially monolayer thin Cu^0 atop bulk Cu_2O can be produced under temperatures of 400 K and low hydrogen gas pressure as studied by X-ray photoelectron spectroscopy (XPS) and X-ray-excited Auger electron spectroscopy (XAES).[56] It may be promising to subsequently generate atomic layer or near atomic layer Cu^0 atop a copper oxide layer during the initial stages of graphene deposition. Furthermore, it has been demonstrated in previous studies that the presence of the copper oxide may perhaps improve graphene formation by decreasing the nucleation density during the initial stages of CVD deposition. Graphene nucleates at the catalytically active Cu^0 surface, and the predominant presence of the catalytically inactive oxide may significantly reduce the nucleation density by almost five orders of magnitude.[57] The smaller nucleation density would permit formation of larger graphene grains, and

therefore reduce grain boundaries and likely enhance electron mobility throughout the graphene layer. A second objective of this work is to investigate the CVD graphene deposition process on polycrystalline copper and CTO-Cu over shortened periods of time without extensive hydrogen annealing of the copper surface. Through this research, it would be possible to investigate the graphene deposition mechanism by watching the deposition process over time, and additionally explore CVD graphene construction on copper surfaces with a significant amount of copper oxide. It is the hope to yield graphene of high quality by understanding the graphene deposition mechanism on copper substrates, leading to potential manipulation of the mechanism to reduce defects, as well as form the graphene on insulating substrates.

Another means to produce graphene on dielectric materials is to use graphene templates as the foundation for further CVD graphene growth. The growth mechanism on bulk copper begins by graphene seed nucleation throughout the copper substrate surface, followed by outward growth of seeds into larger graphene grains. Therefore, if small structured graphene templates can be systematically arranged across an insulating surface with a small amount of catalytic copper present, aligned graphene grains in a controlled geometry may be achievable. Furthermore, graphene growth from graphene templates can provide a way to promote deposition selectivity to localized regions on a substrate surface as opposed to bulk deposition coating the entire surface. This would be a benefit for the creation of structured graphene geometries for research applications in the electronics and sensor industries.

Very little research has been performed on continued graphene growth from graphene templates atop dielectric materials. Most researchers have focused on bulk

CVD graphene deposition on insulating substrates. One promising avenue to create graphene on insulated surfaces is by CVD graphene deposition on evaporated thin-film copper substrates over a dielectric material. Thin films as small as 100 nm coated on a quartz surface show potential for adequate graphene deposition.[58] An additional advantage to this method is the partial or full evaporation of the copper substrate immediately after graphene deposition under CVD graphene deposition conditions. The high deposition temperature of approximately 1000°C and small pressures in the mTorr range promote the evaporation of the surface copper. This would lead to graphene coated on the insulating dielectic substrate. Copper thin films of a 100 nm thickness coated on quartz have shown substantial evaporation during the chemical vapor deposition of graphene with deposition times greater than 420 minutes.[58] Even though this method shows potential, it lacks the capability to control graphene deposition into structured or aligned features, as well as selectively placed graphene on localized regions on the surface. If it was coupled with a structured graphene template, these limitations may be overcome. The third objective of this research is to combine the use of graphene hole array templates on insulating SiO_2 substrates and selectively deposited copper thin films to promote and study possible CVD graphene growth from graphene edges present in the hole array template. It is desired to discover a novel means by which high quality CVD graphene can be produced on insulating substrates with the possibility for control over graphene deposition location.

In summary, there are three major objectives of this work, which are ultimately focused on improving the quality of CVD graphene on copoer substrates and overcoming the current limitations of this process. First, the morphological, optical, and electrical

properties of CVD graphene films grown on polycrystalline copper and CTO-Cu are compared to uncover how substrate characteristics may influence graphene quality. Second, sub monolayer graphene is grown on these copper substrates to investigate the initial stages of growth and elucidate the mechanism of growth. Graphene development on both of these copper foils is performed without a preannealing process to retain the likely copper oxide species at the foil surface to investigate the possibility of CVD graphene production on insulating metallic oxides. Lastly, graphene hole arrays on an insulating silica substrate are implemented as templates and joined with selective copper deposition to investigate potential graphene growth from the template edges after exposure to CVD graphene deposition conditions. The possibility to grow graphene from templates on insulating substrates reduces difficulties in the graphene transfer process, and provides a practical means to deposit graphene in selective surface locations in future research. The following sections detail the methods, results, and discussion for each of these objectives.

5.3 Materials and Methods

5.3.1 CVD Graphene Growth on Polycrystalline and Cube-Textured Oriented (100) Copper

CVD Graphene Deposition and Transfer Process

Commercial polycrystalline copper with a thickness of approximately 25 μm was purchased from Alfa Aesar. Base metal copper was thermomechanically processed to produce cube-textured oriented (100) copper (CTO-Cu) of an 100 μm thickness.[59] Each copper substrate was exposed to similar deposition procedures. First, the copper films were placed into a fused silica furnace tube and heated to 1000°C under H_2 flow (0.1 sccm). After the growth temperature was reached, CH_4 gas was introduced at a flow rate

of 3.0 sccm for 30 minutes. The furnace was allowed to cool to room temperature, and the samples removed from the fused silica tube.

In order to analyze optical and electrical properties of the CVD graphene, it was transferred to glass or a silicon substrate via the following process. First, poly-methyl methacrylate (PMMA) was spin-coated onto the CVD graphene/copper surface. The sample was placed into a solution of iron chloride (0.1 g/mL) to dissolve the copper substrate, followed by a rinse with deionized water. The remaining PMMA/graphene sample was then immersed in deionized water with the graphene-side facing down aligned directly above a silicon substrate. The deionized water was drained, and the PMMA/graphene/silicon sample heated inside an oven at 80°C for one hour to remove any residual moisture. Finally, the PMMA was dissolved by acetone.

Characterization of CVD Graphene on Polycrystalline Cu and CTO-Cu

SEM imaging was done with Joel JSM-630 and Leo 1550 FESEM instruments with the electron beam accelerating voltage at 2-25 KeV. AFM imaging was performed in contact mode under ambient conditions with a Multimode Nanoscope E Atomic Force Microscope (Bruker Instruments). The probe tip used was a silicon nitride NPS with a nomical force constant of 0.12 N/m (Bruker). All images were collected with Nanoscope version 5.13 software, and were collected with a deflection set point of approximately 1.5 V and a scan rate of 2.0 Hz. Images presented here were flattened with the Nanoscope software.

The Raman spectra for graphene on polycrystalline copper and CTO-Cu were obtained with a Renishaw InVia Raman Microprobe with a helium-cadmium laser with

an excitation wavelength of 442 nm. The laser spot diameter on the sample surface is approximately 2 microns, and its energy density is about 1 mW/μm^2. Reported spectra were signal averaged over 10 scans.

The visible transmittance spectra of the graphene films were measured with a Cornerstone monochromator (Newport 74004) with a xenon arc lamp illuminator (Newport 70611) and calibrated UV-Si photodiode (Newport 71640). The IV curves for graphene on poly-Cu and CTO-Cu were conducted with a four point probe apparatus. Gold electrodes were fabricated with a 4 mm length and 2 mm width containing 15nm of deposited titanium and 85 nm of gold on top of a silicon substrate with a 500 nm silicon oxide barrier. The voltage electrodes were separated by 0.3 mm space.

5.3.2 Time-Sequenced Graphene Growth on Cube-Textured Oriented (100) Copper

CVD Deposition and Graphene Transfer Process

Graphene deposition and transfer were performed as previously described in section 5.3.1. Briefly, cube-textured oriented (100) copper (CTO-Cu) foils were placed into a fused silica furnace tube and heated to 1000°C under H_2 flow (0.1 – 2 sccm). After the growth temperature was reached, CH_4 gas was introduced at a flow rate between 3.0 and 35 sccm for times ranging from 2 – 30 minutes, and the furnace cooled to ambient temperature. To transfer graphene from atop the copper substrates the procedure was followed as described in section 5.3.1. To remove any graphene or copper oxide from a CVD graphene/CTO-Cu sample, the sample was exposed to a 0.1 M HCl solution for approximately 2 seconds.

In order to compare the graphene-coated CTO-Cu surface with the bare CTO-Cu copper at elevated temperatures with no carbon source, a CTO-Cu substrate was heated to 1000°C under hydrogen flow (2sccm) and allowed to cool to room temperature. Another CTO-Cu foil was raised to a similar temperature and hydrogen flow, annealed for 20 minutes under hydrogen flux, and subsequently allowed to cool to ambient temperature. This was a control experiment to investigate any potential copper reconstruction at elevated temperatures without graphene deposition.

Characterization of CTO-Cu Substrates with CVD Graphene

The morphology of the copper/graphene surfaces was investigated via SEM and AFM imaging. SEM imaging was done with Joel JSM-630 and Leo 1550 FESEM instruments with the electron beam accelerating voltage at 2 KeV. AFM imaging was performed in contact mode under ambient conditions with a Multimode Nanoscope E Atomic Force Microscope (Bruker Instruments) with parameters described in section 5.3.1.

Energy dispersive spectroscopy (EDS) was performed with a Carl Zeiss Leo 1550 Field Emission Scanning Electron Microscope. The SEM has an EDAX SiLi detector and used the acquisition software Genesis. The electron beam energy was in the range of approximately 10 - 20 kV, and according to Monte Carlo simulations has an interaction volume range of 300 - 890 nm in the Z direction, and 315 – 520 nm in the X and Y directions.

Electron backscatter diffraction (EBSD) patterns were obtained by placing samples in the Leo 1550 FESEM and inclining them with a 70° angle relative to the

normal incidence of the electron beam. The detector is a camera equipped with a phosphor screen integrated with a digital frame grabber.

5.3.3 Comparison of Initial Graphene Growth on CTO-Cu and Polycrystalline Copper

CVD Deposition and Graphene Transfer Process

Graphene deposition and transfer were performed as previously described in section 5.2.1 with a 5-minute deposition time on thermally pretreated CTO-Cu with a thickness of 150 μm and polycrystalline copper commercially purchased from Alfa Aesar.

In order to compare the graphene coated polycrystalline copper sample with bare polycrystalline copper at elevated temperatures with no carbon source, a poly-Cu substrates was heated to 1000°C under hydrogen flow (2sccm) and allowed to cool to room temperature.

Characterization of CTO-Cu and Polycrystalline Copper Substrates with CVD Graphene

The morphology of the copper/graphene surfaces was investigated with the same AFM and SEM instruments and parameters as described in section 5.3.1.

The EBSD mapping and Raman spectra were acquired using equipment and parameters described in section 5.3.1 and 5.3.2.

5.3.4 Graphene Hole Array Templated Growth

<u>Graphene Hole Array Template Production</u>

Templated graphene hole arrays with deposited copper were produced according to the procedure depicted in Figure 5.1. First, mechanically exfoliated flakes of graphene were transferred to silicon substrates via scotch tape. A PMMA resist was spin-coated onto the surface. Then, a nanoimprint lithography (NIL) stamp was placed on the sample surface and was heated to 140-180°C followed by application of 20-50 bar pressure for 4 minutes, and the system was allowed to cool to room temperature. The stamp was removed, and oxygen plasma reactive ion etching (RIE) used to remove the PMMA resist

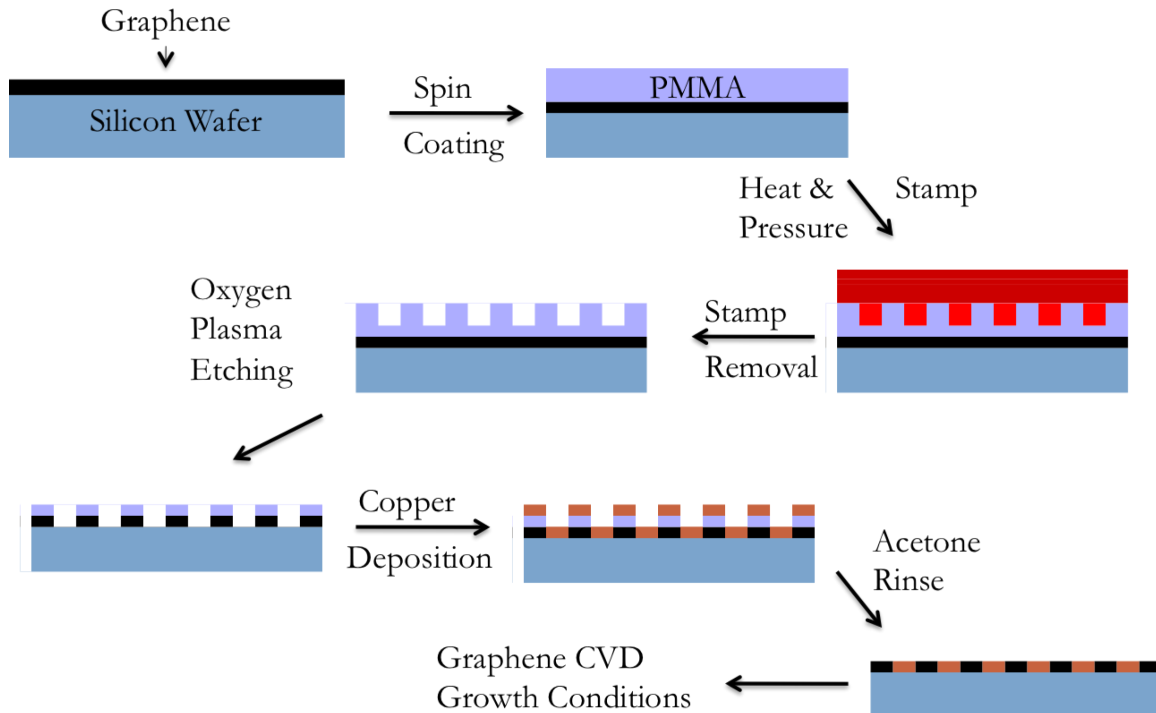


Figure 5.1. Production schematic of templated graphene hole array with deposited copper. First, mechanically exfoliated graphene is spin coated with a PMMA resist. Then, an NIL stamp is placed on the sample surface, heated and pressed. After an oxygen plasma etch to expose the underlying silicon substrate, copper is e-beam evaporated onto the surface with a subsequent acetone rinse. The remaining copper within the templated graphene holes finally undergoes CVD graphene deposition conditions.

and selectively etch away the graphene in the hole regions where the thickness of the resist was decreased due to the heated stamp process. Either 1 nm or 5 nm thick copper layers were deposited via e-beam evaporation onto the surface. An acetone rinse was used to remove the remaining PMMA resist with deposited copper. Finally, the sample underwent the same CVD graphene deposition conditions as previous samples. Succinctly, the sample was placed in a fused silica tube, heated to 1000°C under H_2 flow (2 sccm), followed by CH_4 gas (3.0 sccm) introduction for 30 minutes, and cooling to ambient temperature.

Characterization of Graphene Hole Array Template with Regrown Graphene

SEM and AFM images were obtained with the same equipment and parameters as described in section 5.3.1.

Raman mapping was taken on a confocal Raman system (WiTec alpha300) with a laser excitation of 488 nm and 200 nm resolution. For mapping, the 2D peak was monitored at 2700 cm^{-1} and the G peak at 1580 cm^{-1}.

5.4 Results and Discussion

5.4.1 CVD Graphene Growth on Polycrystalline and Cube-Textured Oriented (100) Copper

In order to study the influence of copper substrate properties on CVD-grown graphene quality, polycrystalline copper and cube-textured oriented (100) copper were exposed to similar graphene deposition conditions for 30 minutes, and the subsequent samples were characterized via several methods. Surface morphology differences before and after graphene deposition on these two copper substrates can be noted in the SEM

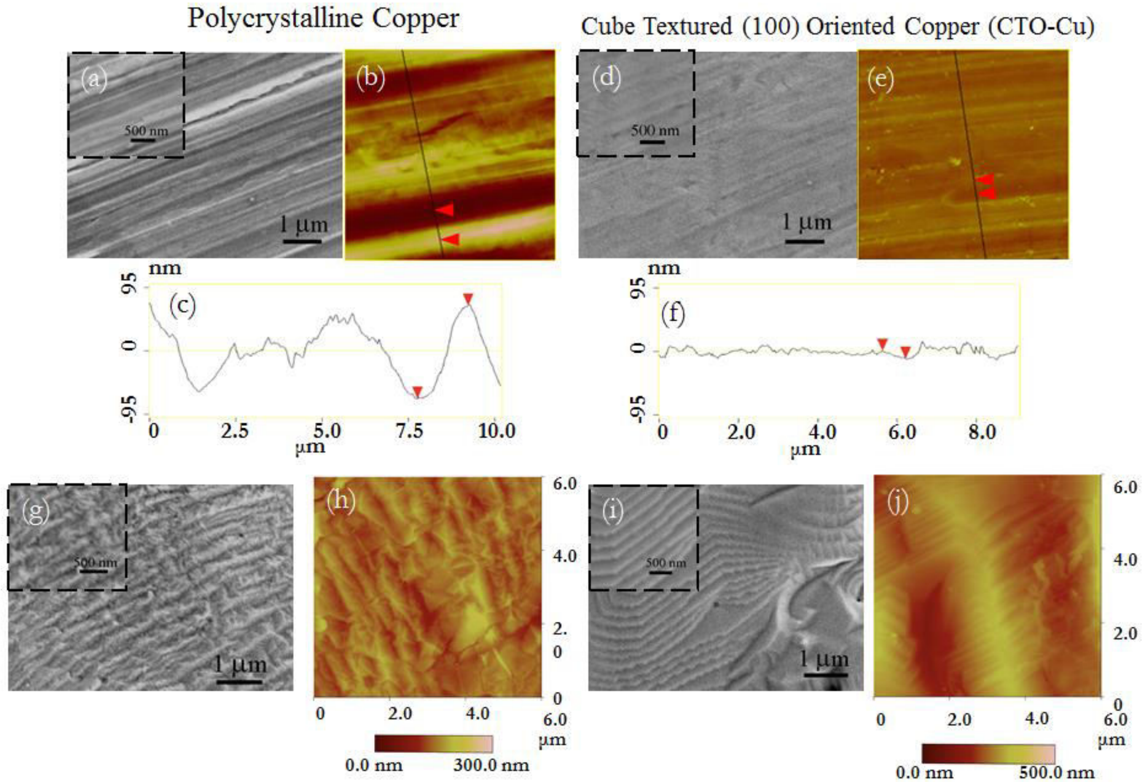


Figure 5.2. (a) SEM with zoomed in inset and (b) – (c) AFM image with cross section of bare polycrystalline copper. (d) SEM image with zoomed in inset and (e) – (f) AFM image with cross section of bare CTO-Cu. SEM with zoomed in insets and AFM images of (g) – (h) CVD graphene on polycrystalline copper and (i) – (j) CVD graphene on CTO-Cu.

and AFM images with corresponding cross sections in Figure 5.2. In parts (a) – (c), it is observed the bare polycrystalline copper has a relatively rough surface with somewhat parallel-aligned hill and valley-like features that span height and depth values of approximately 100 nm. However, the CTO-Cu comparatively demonstrates a flat surface with changes in height less than 10 nm, as seen in parts (d) – (f). Upon CVD graphene deposition, the surface structures of both the polycrystalline copper and CTO-Cu copper change dramatically to form features as shown in parts (g) - (j) in Figure 5.2. The graphene on polycrystalline copper in (g) and (h) seems to form somewhat aligned striations with a resemblance of hill and valley-like topography, slightly similar to the image before graphene deposition, but still undergoing a distinct change in structure

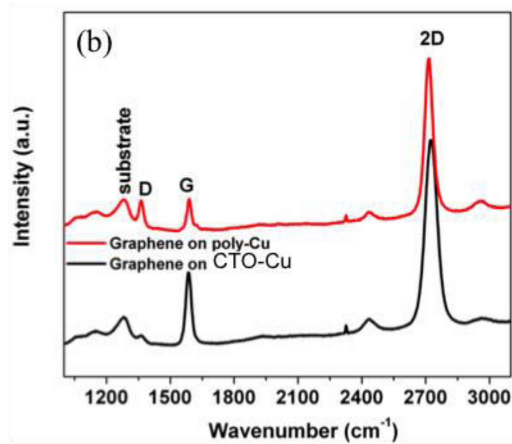
during the CVD deposition process which is much more disordered than the CTO copper. The CTO-Cu analogously experiences a surface morphology transformation upon exposure to CVD graphene growth conditions. In parts (i) and (j) there appear large, raised features on the surface of the graphene-polycrystalline copper on the order of hundreds of nanometers in height, with highly-aligned step-like features embedded within the large hillocks. It is evident that both the polycrystalline and CTO-Cu have a significant change in surface structure and it is not the graphene causing these changes itself, seeing as the features in these AFM images are tens to hundreds of nanometers in dimension, and the height of single-layer graphene on most substrates is approximately 0.5 nm.[2] The copper substrate surface must be restructuring during the graphene deposition process to create these features. It is important to note the changes in surface structure are different amongst the two copper substrates, indicating the substrate could potentially have a role in producing graphene of various quality and with different properties atop the distinct copper topography. Restructuring of the copper surface may also occur during heating without graphene deposition, and is explained in greater detail later in this section.

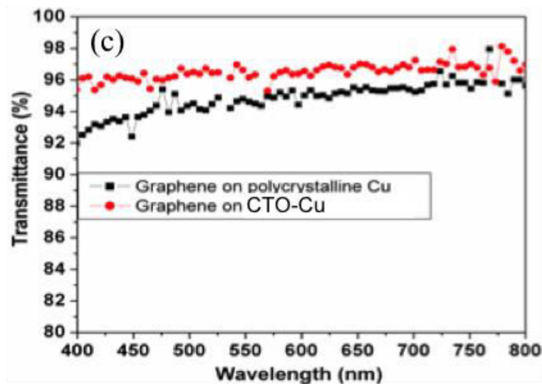
A variety of properties are compared between graphene deposited on polycrystalline copper (poly-Cu) in relation to graphene produced on CTO-Cu in Figure 5.3, and highlight distinct differences of CVD graphene formed on these two copper substrates. In parts (a) and (b) on the figure, there are clear 2D and G peaks at 2700 cm^{-1} and 1580 cm^{-1}, which are characteristic peaks of graphene due to second order zone-boundary phonons and the doubly degenerate zone center E_{2g} mode.[60] The full-width-at-half-maximum for each peak is around 50 cm^{-1}, indicating there is no coupling between

the Raman excitation wavelength at 442nm, which would result in a full-width-at-half-maximum value of 100 cm^{-1} or more. The presence of the 2D peak and G peak demonstrate the existence of graphene on the copper substrate surface, but it is the 2D/G peak intensity ratio that illustrates the number of graphene layers on the metal surface. Since the ratio of both graphene on polycrystalline copper and CTO-Cu is greater than two, as well as show typical symmetrical peak shapes, research suggests a majority of single layer graphene on the two copper samples.[44] Thus, it can be ascertained there is single layer graphene on both the polycrystalline and CTO-Cu. However, the defect density of graphene on these two copper substrates is shown to be different by comparing the D/G peak intensity ratios. The defect character

(a)

Copper Substrate	2D/G Ratio	G/D Ratio
Polycrystalline	4.5	1.3
CTO-Copper	2.8	7.7





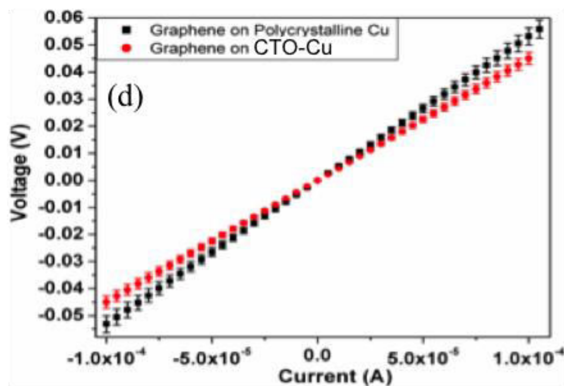


Figure 5.3. (a) Table of Raman spectra 2D/G Ratio and G/D Ratio for graphene on polycrystalline copper (poly-Cu) and CTO-Cu. (b) Raman spectra of graphene on poly-Cu and CTO-Cu. (c) Transmittance spectra of graphene on poly-Cu and CTO-Cu. (d) VI curve for poly-Cu and CTO-Cu.

of the single-layer graphene can be determined by the intensity of the D peak at ~1350 cm^{-1}, which is a consequence of breathing modes of sp^2 rings and the active phonons being excited in defective regions of the graphene, compared to the intensity of the G peak.[61] The higher D/G peak intensity ratio of 0.56 for graphene on polycrystalline copper compared to a 0.2 value for graphene on CTO-Cu suggests the graphene on the polycrystalline copper surface possesses an increased number of grain boundaries and related growth defects.

The difference in defect density between graphene on poly-Cu and CTO-Cu can significantly influence optical and electrical properties. The optical transmittance spectra of graphene transferred from polycrystalline copper and CTO-Cu are illustrated in Figure 5.3-c. Throughout most of the solar spectrum wavelength range of 400 to 800 nm, the transmittance for graphene on CTO-Cu is higher compared to the graphene produced on polycrystalline copper. At 550 nm, the transmittance of graphene from CTO-Cu is approximately 97%, which is close to the value 97.7% for mechanically cleaved pristine graphene with a closely matched theoretically predicted transmittance.[62] The transmittance for graphene on poly-Cu at the same wavelength is around 95%, which may suggest a larger amount of graphene defects. A higher number of misaligned grain boundaries and growth defects may also contribute to the difference in IV curve slopes for graphene on CTO-Cu and polycrystalline copper shown in Figure 5.3-d. From the four point probe measurements, the calculated conductivity for graphene deposited on CTO-Cu is approximately 20% higher than the conductivity for graphene grown on polycrystalline copper. It is expected a larger defect density and presence of an increased

number of grain boundaries would significantly impair charge mobility of the graphene layer, and thereby lead to a smaller conductivity.

It is evident the contrasting characteristics of CTO-Cu and polycrystalline copper influence the optical and electrical properties of graphene deposited on these copper surfaces, and potentially impact the amount and structure of grain boundaries and other defect features within CVD graphene. However, this data does not provide a clear understanding of how specific features of the copper substrates influence the organization and quality of CVD graphene on their surfaces. It is the purpose of this research to be able to manipulate the components of the copper substrate to controllably affect CVD graphene, and therefore a better knowledge of the graphene deposition mechanism on polycrystalline and CTO-Cu is imperative.

5.4.2 Time-Sequenced Graphene Growth on Cube-Textured Oriented (100) Copper

In order to understand the effect of particular copper foil characteristics on the growth of CVD graphene, CTO-Cu underwent deposition conditions for shortened time periods to study initial growth features and how those features change until single-layer graphene coats the entire surface of the copper substrates. CTO-Cu samples were heated to 1000°C under hydrogen flow followed by the introduction of CH_4 gas, and these conditions were held for times between 2 – 30 minutes before cooling to room temperature. The AFM and SEM results of a 2, 5, and 10 minute graphene deposition time on CTO-Cu are shown in Figure 5.4. In (a) and (b), you can see the initial development of small triangular features with sizes on the order of tens to a couple hundred nanometers dispersed throughout the copper surface after a 2 minute graphene

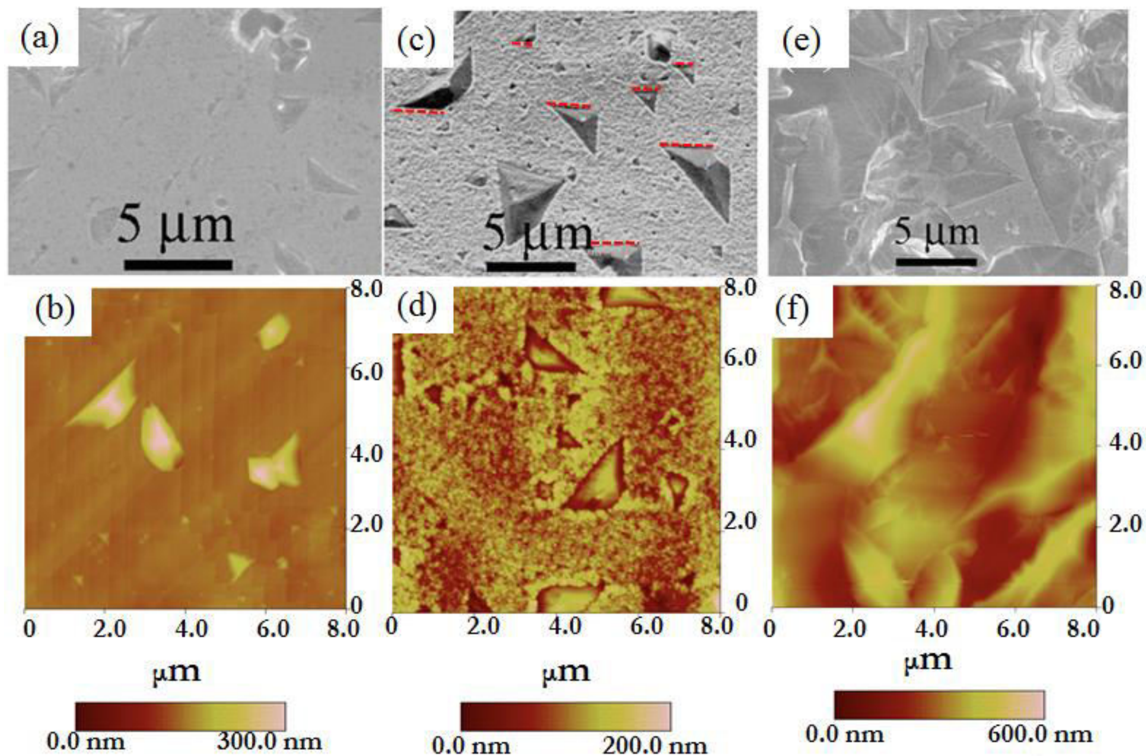


Figure 5.4. SEM and AFM image of CTO-Cu with (a) – (b) 2 minute, (c) – (d) 5 minute, and (e) – (f) 10 minute exposure to graphene deposition conditions.

deposition period, as well as a few micron-scale triangular-like structures visibly apparent in the AFM image in part (b). The background region around these geometric elements still looks relatively flat with a hint of parallel striations, comparable to the surface features of the bare CTO-Cu. After 5 minutes, however, there seems to be a greater quantity of large right triangles with dimensions on the order of several microns. One side of most of the triangles is aligned relatively along the same axis as shown with

the red dashed lines in (c). It is likely the alignment may be a result from the special processing of CTO-Cu to align its Cu (100) grains in the same orientation, demonstrating the influence of the bare copper substrate character on potentially aligning graphene grains. In the region around the triangular features appears a fairly even distribution of raised debri whose composition will be discussed later. Continuing on to a graphene

growth time of 10 minutes, in the SEM and AFM image in Figure 5.4 part (e) and (f), the triangles on the copper surface have grown in size and begin to coalesce with one another as their external edges begin to encounter one another. The substrate surface is predominantly covered with these geometric structures with heights reaching several hundreds of nanometers, and the flat region surrounding the triangles begins to diminish. Although, at this point, there are still smaller triangles less than one micron in size dotting the more flat areas in between the mountainous triangle shapes. It should be noted the deposition at this time resembles the large-featured surface observed in Figure 5.2 with a deposition time of 30 minutes in which single-layer graphene covers the entire copper foil surface. The formation of these smaller triangle features could demonstrate the initial restructuring of the copper surface to promote graphene deposition in these regions. From the collective data illustrated here, it can be concluded during the graphene deposition process on CTO-Cu, triangular features begin to form across the entire surface and grow in dimension over the course of deposition time. Initial triangles with smaller sizes begin to grow in height and lateral range and merge at the edges as they spread across the surface. Furthermore, at any point during the graphene growth process there is new triangle formation on the flatter regions of the substrate surface. The clear development of triangular features during the initial stages of CVD graphene growth could demonstrate the restructuring mechanism of the copper foil surface to promote graphene deposition in these locations.

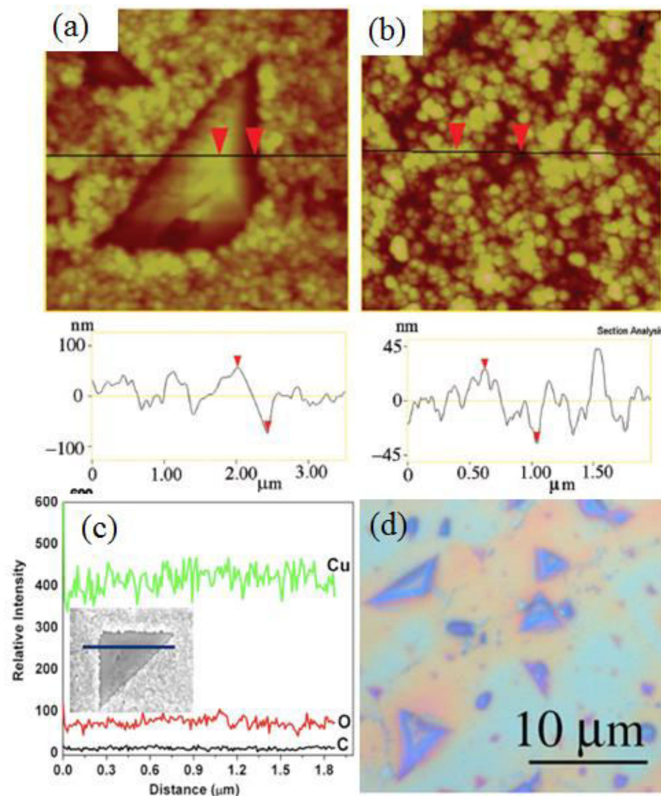


Figure 5.5. (a) AFM image with cross section analysis of single triangle feature on CTO-Cu after 5 minute exposure to graphene deposition conditions. (b) AFM image and cross section analysis of background region following 5 minute growth time on CTO-Cu. (c) EDS line scan of Cu, O and C across the line of the triangle shown in the SEM inset. (d) Optical image of transferred graphene grown on CTO-Cu with 5 minute deposition time.

A closer look at the detailed characteristics of a single triangle on CTO-Cu after a 5 minute graphene growth time is illustrated in Figure 5.5. The triangle features are on the order of 80-150 nm tall from edge to center and show clear faceting along different directions, as demonstrated in the cross section of part (a) of this figure. The area surrounding the triangle illustrated in the AFM image with cross section in part (b) shows very rough topography with a roughness on the order of 10-15 nm. It is possible an adsorbed hydrocarbon layer from methane adsorption and breakdown at the copper surface may account for this morphology, but it is unlikely because the expected thickness of an adsorbed layer would be much smaller in value. The EDS line scan in part (c) suggests the surface coating may be some amorphous copper oxide due to the presence of an oxygen signal outside the triangle area. The CVD process in this research is a low vacuum process, and it is possible for residual adsorbed oxygen on the copper surface to remain and form a copper oxide across the substrate surface. Signal from oxygen is not restricted to the area around

the triangle structure, but a comparable oxygen signal is found inside the triangle structure as well. The consistency of the oxygen amount in both of these regions suggests an evenly dispersed copper oxide layer among the entire substrate surface. Furthermore, the copper oxide layer must be relatively thick, likely on the order of tens or hundreds of nanometers, considering the interaction volume in the Z direction for the EDS measurements is believed to be in the range 300-890 nm. The copper oxide must be relatively thick in order to show a sufficient oxygen signal in comparison to copper. If the copper oxide possessed a thickness around the single nanometer scale, the oxygen signal would be significantly lower. Graphene formation can only occur at a copper interface, however, so it is predicted there is copper oxide reduction at the uppermost regions of the copper oxide inside the triangle feature to induce graphene deposition. The reduced layer may be so thin it would produce a negligible signal compared to the signal from the bulk copper substrate. From the EDS line scan it can be seen there is no change in all the Cu, O, or C signals, resulting in a uniform element distribution inside and outside the triangle formation. The Cu signal is expected to remain constant considering the large amount of bulk copper substrate. The homogenous carbon is most likely a result of adsorbed hydrocarbon species from the methane source across the entire copper surface.

To confirm the location of CVD graphene atop the triangle formations, all deposited graphene from 5 minute graphene deposition on CTO-Cu was transferred onto silicon substrates with a 300 nm-thick thermal oxide and the optical properties were investigated for any transferred material. The resulting optical image in Figure 5.5-d shows dark-colored regions in triangular geometries across the sample with a difference

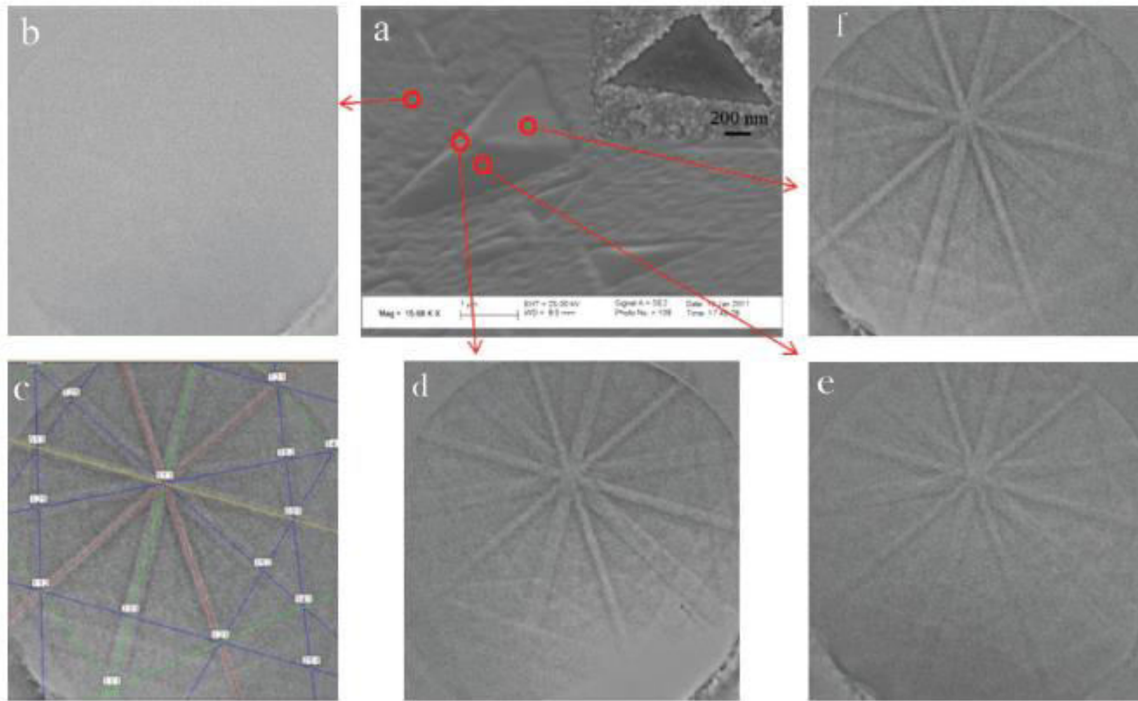


Figure 5.6. (a) SEM image of triangular features on CTO-Cu after 5 minute graphene deposition. (inset SEM image of triangle with a flat top). (b) EBSD pattern in region surrounding triangle. (d) – (f) EBSD patterns on different facets of the triangle. (c) EBSD pattern indexed to Cu (111).

in optical properties, which correspond to graphene on the silicon substrate.[2] The size and shape of the darker areas parallel the dimensions of the triangles in the previous AFM and SEM images. This indicates graphene nucleation and growth on the triangular regions of the CTO-Cu foil.

It is apparent the formation of triangular features on the CTO-Cu surface during the CVD deposition process promotes graphene growth, and it has been shown that the morphology of the copper foil changes dramatically to produce these triangular features. In order to understand further how the copper surface restructures to allow graphene deposition, electron back-scatter diffraction (EBSD) patterns were collected on the triangular formations as well as surrounding locations around the triangles. It can be seen in Figure 5.6-b that there is no detectable diffraction patterns obtained outside of the

triangle shapes, indicating an amorphous surface. Conversely, the EBSD patterns on spots within the triangle areas produce distinguishable patterns among all facets (Figure 5.6 (d) –(f)), illustrating the structures are single crystalline. All of these patterns can be indexed predominantly to the Cu (111) out-of-plane within several degrees with respect to the standard pole using TSL OIM Analysis 5 software, which may be due to the pyramidal shape of the triangles confirmed in the AFM image in Figure 5.6-a. The lattice of Cu (111) at 2.56 Å is quite similar to the lattice of graphene at 2.46 Å,[29] which would indicate a restructuring of the predominantly Cu (100) CTO-Cu surface to a Cu (111) in order for the graphene film to match the lattice of the substrate and minimize stress and defect formation in its development. It should be noted the similar lattice constants make it difficult to distinguish graphene directly from Cu (111), and both would cause comparable diffraction patterns. The penetration depth of the EBSD technique is on the order of tens of nanometers, and the average step height for graphene on silica is from 0.5 – 1 nm,[2] so the majority of the signal is likely due to the Cu (111) lattice underneath the thin graphene coating. Furthermore, the single crystalline Cu (111) lattice has a three-fold symmetry, and if the entire shape of the feature were dependent on the Cu (111) orientation it would be expected the surface would produce triangles in an equilateral geometry instead of right-angle alignment. However, this is not observed. The four-fold symmetry of the Cu (100) lattice would result in features in rectangular geometries, however. The appearance of principally (111) oriented right-angle triangles suggests not only does the copper surface restructure to a (111) lattice to initiate graphene deposition, but the substrate's initial (100) crystal face also influences the alignment of the triangles.

Another important note to discuss is that all the diffraction patterns showed behavior for Cu (111) underneath the triangular formations, and not behavior for copper (II) oxide (111). The EDS line scans showed a significant oxygen signal, denoting the presence of a copper oxide layer across the entire substrate surface, even within the triangular structures. Copper (II) oxide (111) has a notably different lattice constant of 5.96 Å[63] as compared to Cu (111) and graphene, which would result in a different diffraction pattern than Cu (111) and graphene. Additionally, if the copper oxide were amorphous, there would be no detectable diffraction pattern. Since there is not a significant signal for this diffraction pattern for copper (II) oxide (111) and the primary signal fits well to the Cu (111) and graphene lattices, there must be a reduced Cu (111) layer between the deposited graphene and copper oxide that is thick enough to be detectable by EBSD analysis. Considering the penetration depth of EBSD is on the order of tens of nanometers, it is predicted the thickness is likely at least 10 nm to produce a notable diffraction pattern signal. Further profiling XPS studies are planned to investigate the actual thickness of this reduced copper layer, and potentially manipulate deposition conditions to reduce its thickness.

To further investigate the copper structure underneath the single layer graphene, the graphene deposited on CTO-Cu after a 5 minute deposition and any surface oxide was dissolved with brief exposure to a 0.1 M HCl solution (~ 2 sec) and the resulting surface structure studied via SEM imaging. Figure 5.7 (a) – (c) shows the foundations of the large triangle features several microns in size remain with smaller irregular-shaped nanoparticles spread across the entire surface. It can be observed that many of the nanoparticles have sharp edges and vertices, suggesting they may have crystalline

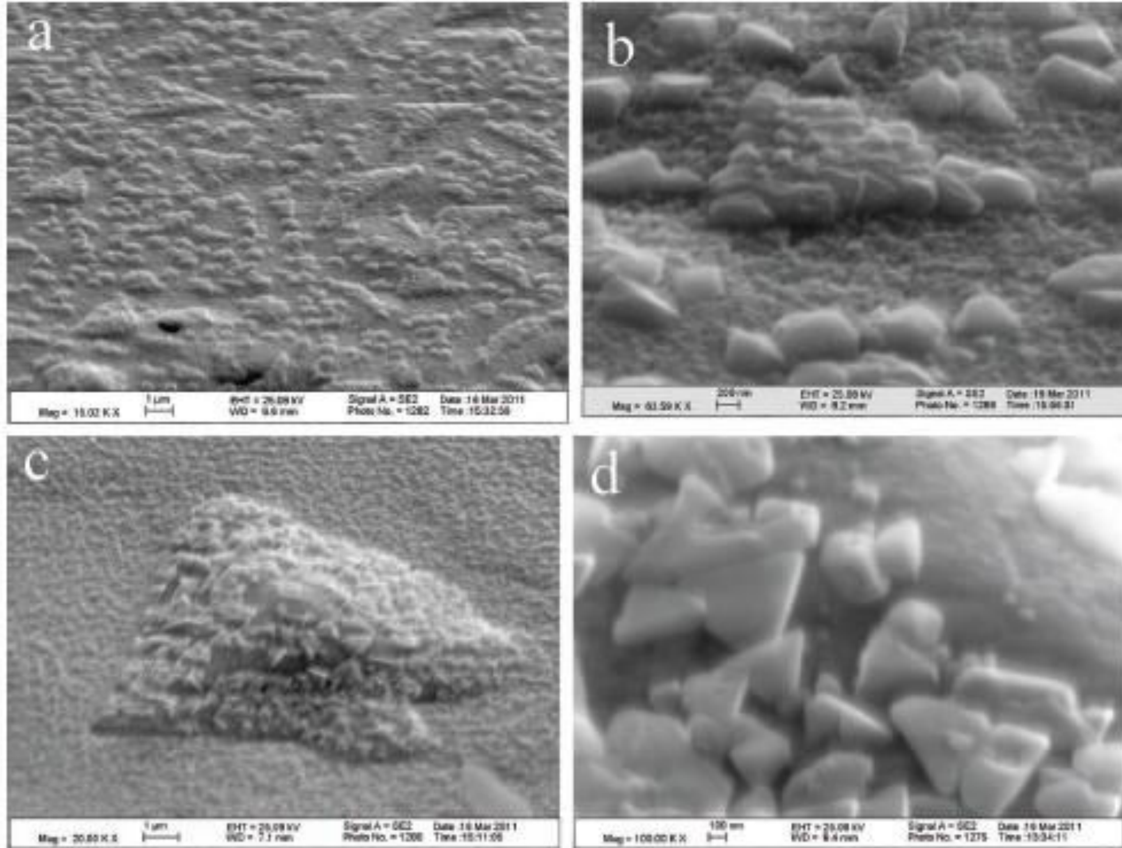


Figure 5.7. (a) – (c) SEM images of graphene grown on STO-Cu for 5 minutes and etched in the 0.1 M HCL solution for 2 secnds at different scales. (d) Zoomed in SEM images of the nanoparticles revealing equilateral triangle-shaped nanoparticles

structures. In the zoomed in view near the apex of the large triangle structure (Figure 5.7 -d), most of the nanoparticles have an equilateral shape indicating a (111) crystalline lattice as seen in the EBSD patterns in Figure 5.6. Research has shown that metal oxides may epitaxially form on (100) oriented metals, such as Ni[64] and Cu.[65,63] Specifically, a Cu_2O (111) layer tens of nanometers in thickness may nucleate in the form of nanoparticles on a Cu (100) lattice at elevated temperature due to the presence of sub-surface oxygen.[65,63] To validate the formation of copper oxide nanoparticles developing on the copper (100) surface under exposure to intense heat, CTO-Cu substrates were

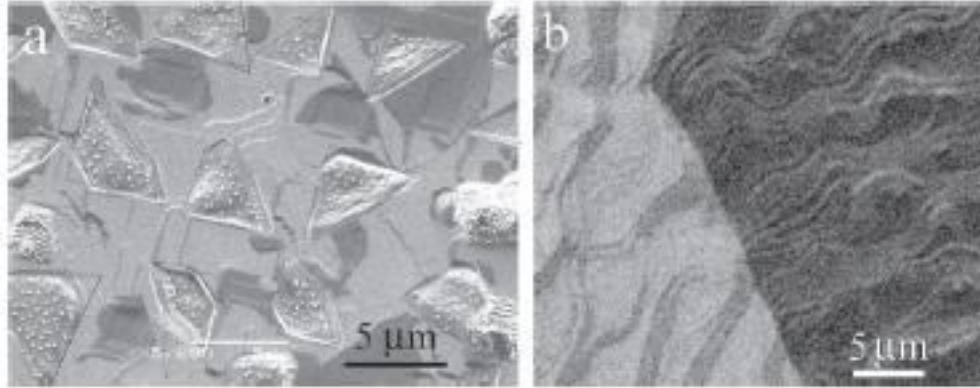


Figure 5.8. (a) SEM image of CTO-Cu heated to 1000°C under 2 sccm H_2 flow followed by immediate cooling to room temperature. (b) SEM image of CTO-Cu heated to 1000°C under 2 sccm H_2 flow, annealed for 20 minute with constant hydrogen flow and temperature, followed by cooling to room temperature.

heated to 1000°C under hydrogen flow and immediately brought down to room temperature, or annealed for 20 minutes under hydrogen flux and allowed to cool

to ambient temperature. The SEM image in Figure 5.8-a shows right-triangle shapes several microns in dimension, comparable to the geometries and sizes of the triangle formations observed under CVD graphene deposition conditions. Within the triangular features are nanoparticles similar to ones found after removal of the CVD graphene layer on copper following exposure to a hydrochloric acid etch. Upon sustained heat and hydrogen flow for an extended period of time (20 minutes), the triangle features with an EBSD pattern (not shown) indexed to Cu_2O (111) disappear from the surface structure (see Figure 5.8-b) and any notable diffraction pattern is no longer detectable. This implies the triangle features are most likely surface features of copper oxides initially formed due to residual oxygen in the CTO-Cu and in the CVD chamber, and after prolonged annealing these features disappear to form an amorphous film at the copper surface.

Based on all the information regarding the surface morphology and structure of graphene and copper during the initial stages of graphene nucleation and growth, a model of the deposition mechanism is proposed as illustrated in Figure 5.9. Research has shown the reduction rate of copper oxide lowers with decreasing H_2 partial pressure.[66] The relatively small H_2 partial pressure of 2 sccm used in this research may not be sufficient to reduce the thick copper oxide at the surface interface, leaving some remnant of a copper oxide species at the copper substrate surface. The remaining copper oxide at the surface coupled with the introduction of hydrogen gas may cause partial melting of a thin layer at the copper foil surface, as seen in the top left image in Figure 5.9. The eutectic temperatures for Cu-CuO and Cu-Cu_2O are approximately 1091°C and 1066°C, which are slightly above the 1000°C deposition temperature region. However, premelting,[67] or partial melting, of a thin layer near the copper substrate surface has been shown to occur

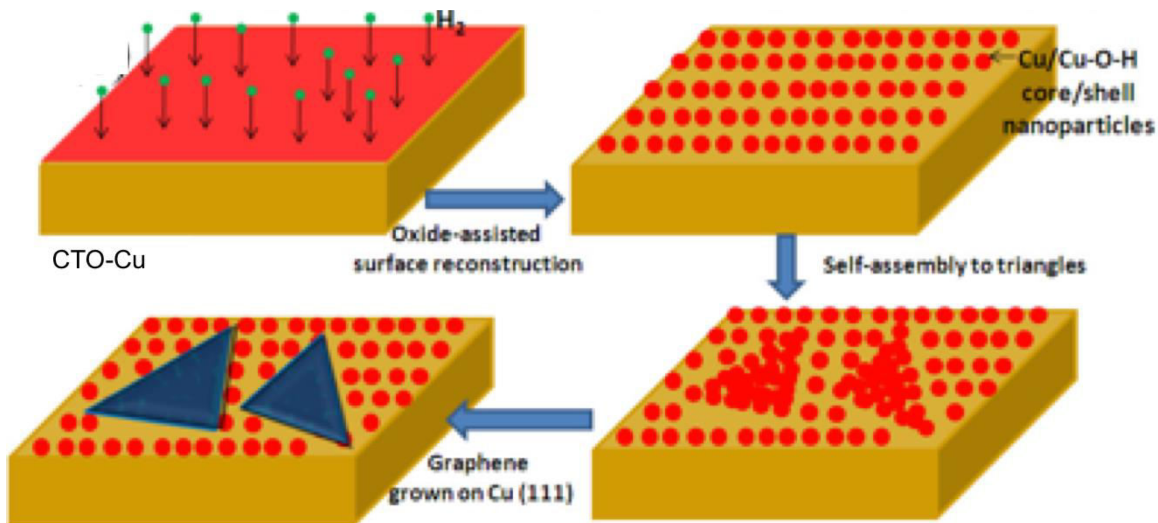


Figure 5.9. Schematic of the CVD graphene deposition process on CTO-Cu at 1000°C under H_2 flow. First, the formation of a Cu-O-H layer (red color) upon diffusion of H_2 in Cu (yellow). Then, formation of Cu nanoparticles with partially melted Cu-O-H surface layer (red sphere). Third, segregation of the Cu/Cu-O-H core/shell nanoparticles and last formation of triangle domains. Lastly, the deposition of graphene on the amassed triangular domains.

at temperatures considerably lower than the bulk melting temperature of copper (1083°C) depending on the crystallographic orientation at the surface and existence of impurities,[68] such as CuOx and H_2, whose solubility increases in Cu at elevated temperatures. The easy mobility in the thin liquid-phase layer at the surface may promote the aggregation of copper oxide species into nanoparticles within the melted Cu-O-H layer, as demonstrated in the top right picture in Figure 5.9. Since the (111) crystal orientation is the most energetically favored, the nanoparticles are very likely to assemble into the Cu_2O orientation and form equilateral triangles as observed previously in Figure 5.7. Not only could it be possible for these nanoparticles to form, but also to migrate in the partially melted Cu-O-H layer to form triangular domains (bottom right image). The right angle geometry and parallel alignment of the domains are most likely facilitated by the underlying Cu (100) beneath the melted surface layer. The nucleation and deposition of graphene can occur epitaxially on the surface of these triangle domains upon reduction at the surface layers of the Cu_2O nanoparticles to Cu^0 (bottom left image). Copper oxide reduction in the partially melted thin layer regions surrounding the triangles may occur more slowly due to the amorphous Cu-O-H composition, and the crystalline Cu_2O (111) provides an easy avenue for reduction to Cu (111).

It is clear specific characteristics of CTO-Cu significantly influence the CVD graphene deposition process. The (100) textured surface on CTO-Cu is capable of influencing the alignment of triangle features formed on the copper oxide surface, as well as their arrangement into right-angled geometries. Restructuring of the copper oxide in these regions to form nanoparticles then promote the reduction to Cu (111) with subsequent graphene deposition. The triangle formations with deposited graphene grow

in dimension across the sample surface until their edges merge and graphene coats the entire substrate. The impact the CTO-Cu has on graphene growth is promising to aid in the alignment of graphene grains, and produce graphene of high quality with increased electron mobility.

5.4.3 Comparison of Initial Graphene Growth on CTO-Cu and Polycrystalline Copper

Now that its been established that features of CTO-Cu copper can significantly influence the characteristics of CVD graphene and its deposition mechanism, it is important to study how graphene features may change and how the deposition mechanism may be modified when the copper substrate contains different characteristics than CTO-Cu, such as with polycrystalline copper. If the objective of this research is to be able to manipulate copper foil properties to produce defect-free and highly conductive single layer CVD graphene, it is imperative to know not only the details of graphene deposition on a single type of copper surface, but on multiple copper surfaces to understand how the change of copper substrate properties influences the change in graphene characteristics.

For this investigation, CVD graphene was deposited on both CTO-Cu and polycrystalline copper foils for a limited time period to examine the initial graphene deposition properties on the two copper surfaces. The copper foils to were heated to 1000°C under hydrogen flow, exposed to methane for a 5 minute period, and allowed to return to ambient temperature conditions. The contrasting surface morphologies are evident in the AFM images illustrated in Figure 5.10. Consistent with images presented in the previous section, triangle formations ranging in lateral dimensions from tens of

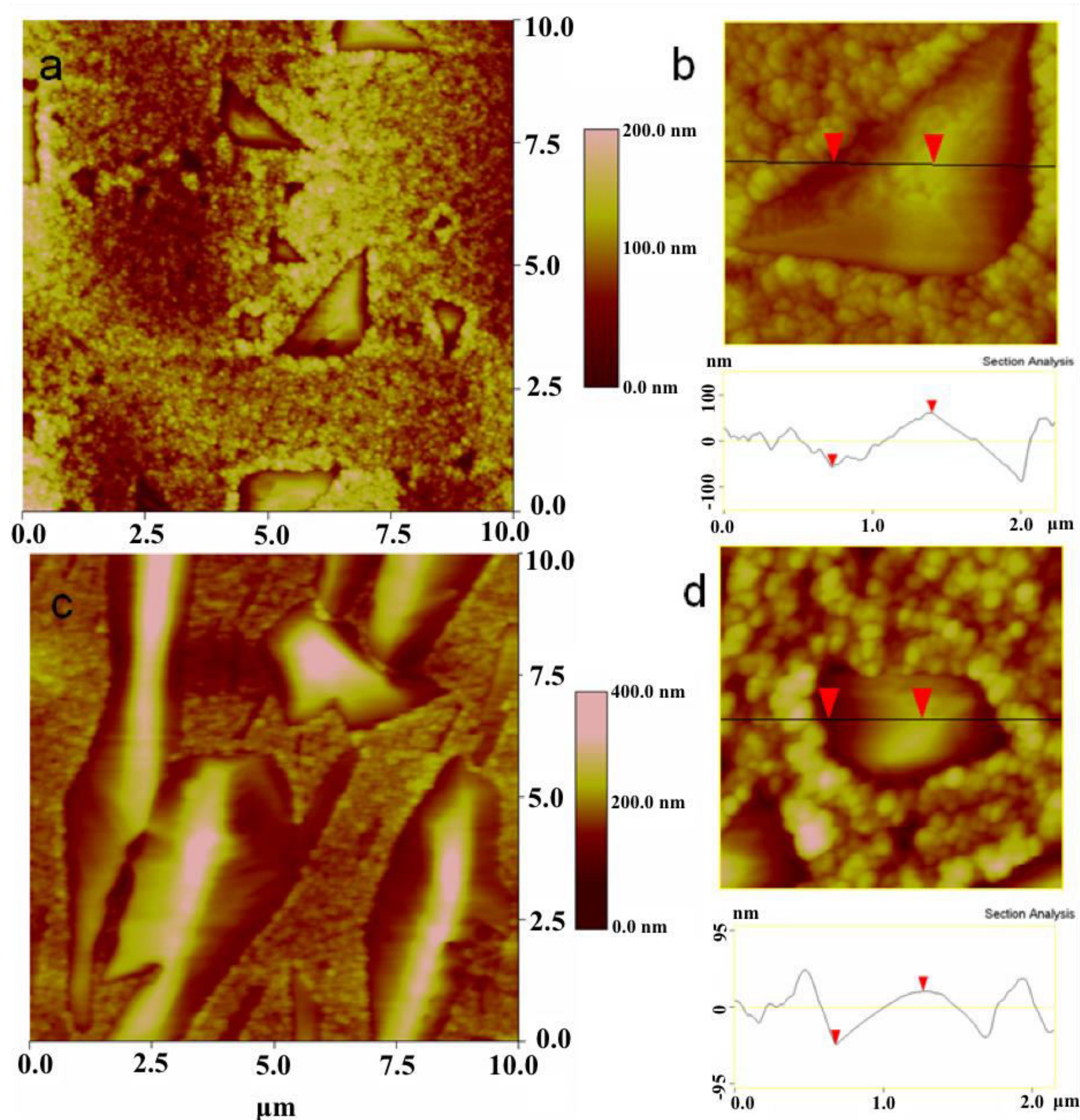


Figure 5.10. (a) AFM image of graphene on CTO-Cu after 5 min deposition. (b) Zoomed in view of triangle on CVD graphene/CTO-Cu after 5 minute graphene deposition with cross section analysis. (c) AFM image of graphene on polycrystalline copper after 5 minute deposition. (d) Zoomed in view of features on CVD graphene/poly-Cu after 5 minute graphene deposition with cross section analysis.

nanometers to a few microns are dispersed throughout the CTO-Cu surface after a 5-minute graphene deposition period (image (a)). The height of a typical triangle from edge to center illustrated in part (b) of this figure is in the range of 80-150 nm. The region surrounding the triangle shapes demonstrates a jagged topography with a roughness around 10 – 15 nm, which is mostly likely the result of an amorphous copper

oxide building up around the triangle geometries. In comparison, the surface formations on the polycrystalline copper (Figure 5.10-c) additionally show a distribution of tall faceted features in localized regions amidst a background of a somewhat coarse morphology. These large structures, however, do not show any specific geometry at their base or any clear alignment amongst their population. This was somewhat expected considering the polycrystalline copper does not have any special pretreatment as does the CTO-Cu to align its grain boundaries or to predominantly change the surface structure to a single orientation of the crystal lattice. Additionally, the minority of the large formations possess heights similar to the triangles features on CTO-Cu, with heights

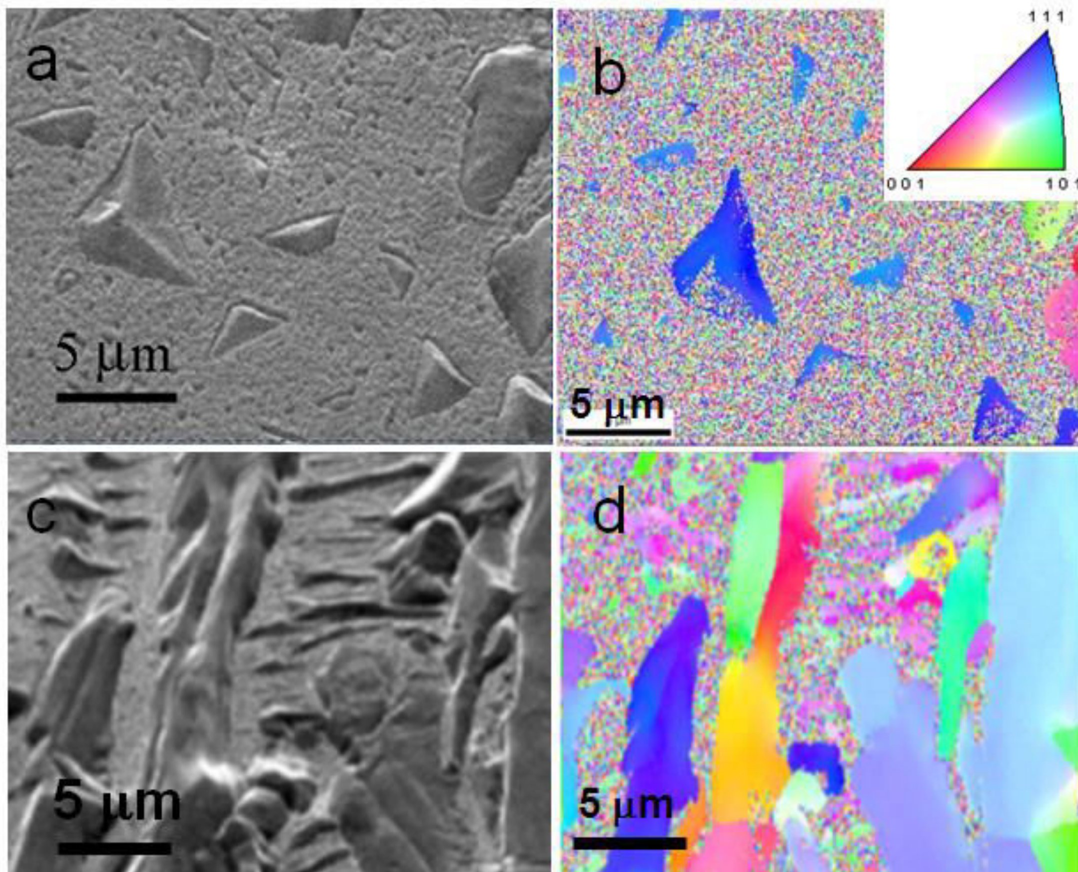


Figure 5.11. (a) SEM image and (b) EBSD OIM mapping of CVD graphene on CTO-Cu after 5 minute graphene deposition. (c) SEM image and (d) EBSD OIM mapping of CVD graphene on polycrystalline copper after 5 minute graphene deposition.

around 100 nm as shown in part (d) of Figure 5.10, however a majority of heights extend over 200 nm and lateral dimensions reaching several microns. Clearly there is different surface morphology upon restructuring of the copper surface during the initial stages of CVD graphene deposition on CTO-Cu and polycrystalline copper. These structures are validated in the SEM images displayed in Figure 5.11. Also shown in Figure 5.11 are EBSD mappings which correspond with the specific SEM images in (a) and (c). From the EBSD mapping for graphene on CTO-Cu after a 5 minute deposition time (Figure 5.11-b), it can be seen that the majority of the triangular features on the surface have a (111) crystal orientation represented by the blue color, and in the surrounding areas the spackling of a variety of colors designates some type of amorphous material. These results were confirmed in previous timed studies of graphene deposition on CTO-Cu. Comparatively, the images in part (c) and (d) of this figure highlight the morphology and lattice structure of the substrate surface upon graphene deposition on polycrystalline copper following a 5 minute growth period. The large structured features in the SEM image mirror that shown in the previous AFM images, and the areas outside of the formations demonstrate coloring in the EBSD image similar to that of the CTO-Cu/graphene sample, indicating amorphous material. But, the EBSD mapping of these sizable structured formations exhibit a variety of lattice faces among the (111), (100), and (101) orientations. The ability for CVD graphene to form on copper lattices other than (111), such as the (100) orientation have been shown in other research, however the CVD graphene produced on these other single crystalline structures have reportedly been lower in quality in comparison to CVD graphene on a Cu (111) substrate due primarily to lattice mismatch.[47,48]

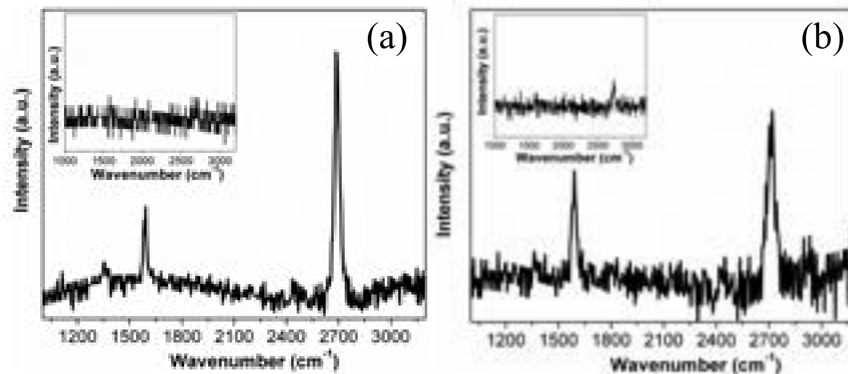


Figure 5.12. (a) Raman spectra on triangle formation on CTO-Cu with graphene after 5 minute deposition. Inset Raman spectra taken in region outside of triangle feature. (b) Raman spectra on irregular-shaped structure feature on polycrystalline copper with graphene after 5 minute deposition. Inset spectra obtained in region surrounding large faceted formations.

Raman studies performed here support findings shown in previous research. Raman spectra of graphene deposited on CTO-Cu and polycrystalline copper after 5 minutes of exposure to CVD growth conditions are displayed in Figure 5.12.

The spectra for the graphene coating on CTO-Cu was obtained atop the region of the large triangle shapes, and the CVD graphene on polycrystalline copper obtained from inside the area of large irregularly-shaped faceted formations. Both exhibit the characteristics 2D and G peaks for graphene at 2700 cm^{-1} and 1580 cm^{-1} due to second order zone-boundary phonons and the doubly degenerate zone center E_{2g} mode.[60] The intensity ratio for the 2D to G peak for the graphene on CTO-Cu (Figure U-a) is calculated to be over two, supporting the premise of single layer graphene covering the triangle structures on CTO-Cu. There is no distinguishable signal in the surface region outside of the triangle shapes, as seen in the inset of this image, confirming there is no notable graphene construction outside of the triangles. In comparison, the 2D/G peak intensity ratio for the graphene grown on polycrystalline copper does not exceed two, which may be due to either multiple layers of graphene, or significant defect development

in the CVD graphene potentially caused by strain between the mismatched lattices of graphene and the underlying variety of crystalline orientations. The presence of the D peak at ~1350 cm^{-1} would allow for a better comparison of defect density between these two graphene samples on CTO-Cu and polycrystalline copper, but the very small peak at this wavenumber in both of these spectra make it very difficult to quantify and make a comparison. It is still evident, however, the quality of graphene epitaxially grown on CTO-Cu illustrates behavior of higher quality in comparison to that of polycrystalline copper during the initial stages of CVD graphene deposition. This is most likely due to the restructuring of the CTO-Cu surface to a predominantly (111) orientation to match the lattice constant of graphene, whereas growth on polycrystalline copper occurs on a much more varied surface morphology with a variety of exposed crystal faces. Therefore, it is desirable to develop copper surfaces which may restructure primarily to a surface (111) orientation, and CTO-Cu shows a promising means to achieve this objective.

On the CTO-Cu it was shown previously that the aligned triangle structures found on its surface following CVD graphene deposition for 5 minutes were formed during the initial heating process before the introduction of a methane gas carbon source. This initial surface reconstruction influenced the location of graphene deposition on the surface, as well as potential alignment of its grains. To investigate how initial thermal heating affects potential changes on the bare polycrystalline copper surface, polycrystalline copper samples were heated to 1000°C under 2 sccm hydrogen flow, and immediately upon reaching this temperature allowed to cool back to ambient temperature conditions. The resulting substrate morphology is illustrated in the SEM image in Figure

5.13. There is no clear evidence of organized formations on the sample surface, or nanoparticle formation as demonstrated on CTO-Cu under similar treatment. Randomly aligned striations of dark color appear across the surface, and EBSD patterns (not shown) show the crystal orientation within these darker regions to be correlated to a variety of lattice structures, whereas there is no detectable signal of the lighter regions, indicating amorphous material. This matches the findings whereby the CVD graphene deposited on polycrystalline copper is atop a substrate surface with a range of crystalline lattices. These results reaffirm the distinct influence the pretreated textured (100) surface on the CTO-Cu has on the particular alignment and growth process of CVD graphene on copper substrates.

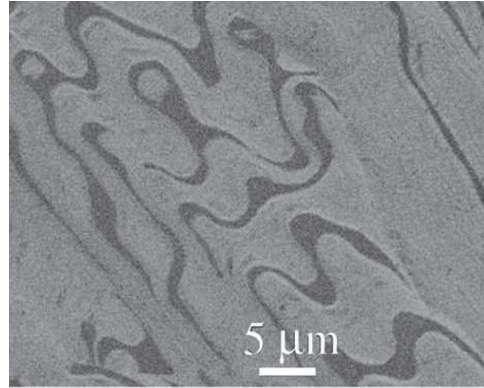


Figure 5.13. SEM image of poly-Cu heated to 1000°C under 2 sccm H_2 flow followed by cooling to room temperature.

In summary, the initial growth stages of CVD graphene on CTO-Cu and polycrystalline copper show clear differences in morphology, graphene quality, and copper substrate restructuring to form different crystalline lattices underneath the nucleated graphene regions. On the CTO copper, the morphology of the copper substrate surface displays clearly aligned right-triangle formations indicative of organization influenced by the textured (100) surface, whereas the polycrystalline copper depicts large irregular-shaped faceted features with no specific alignment. The surface on the CTO-Cu undergoes a lattice reconstruction to an (111) orientation to promote higher quality graphene deposition due to matching lattice constants, and the polycrystalline copper

surface found underneath CVD graphene areas displays a range of crystalline lattices producing graphene regions with behavior indicative of a higher defect density. Clearly, characteristics of the copper substrate play a significant role in the deposition mechanism of graphene on metallic surfaces, and the manipulation of copper substrate features can be used to improve CVD graphene quality.

5.4.4 Graphene Hole Array Templated Growth

Graphene deposited on various metallic surfaces via chemical vapor deposition presents several advantages such as low cost, large area production, and an easy production scheme. However, there are also several drawbacks to this method as well such as high defect density, multiple graphene sheet production on some metals, and graphene production on a conducting metallic substrate. It is because of this last disadvantage there has been interest in producing graphene on nonconductive substrates such as silicon, but these processes typically generate graphene flakes on the micron scale and of very low quality.[51,52,53] In order to overcome this limitation, we would like to explore the potential of growing graphene from a templated graphene scaffold on a nonconducting silicon substrate, and minimize the use of conductive metal in the deposition process. It is the hope to be able to potentially produce graphene on an insulating substrate, and investigate the possibility of controlled graphene placement on a templated graphene pattern.

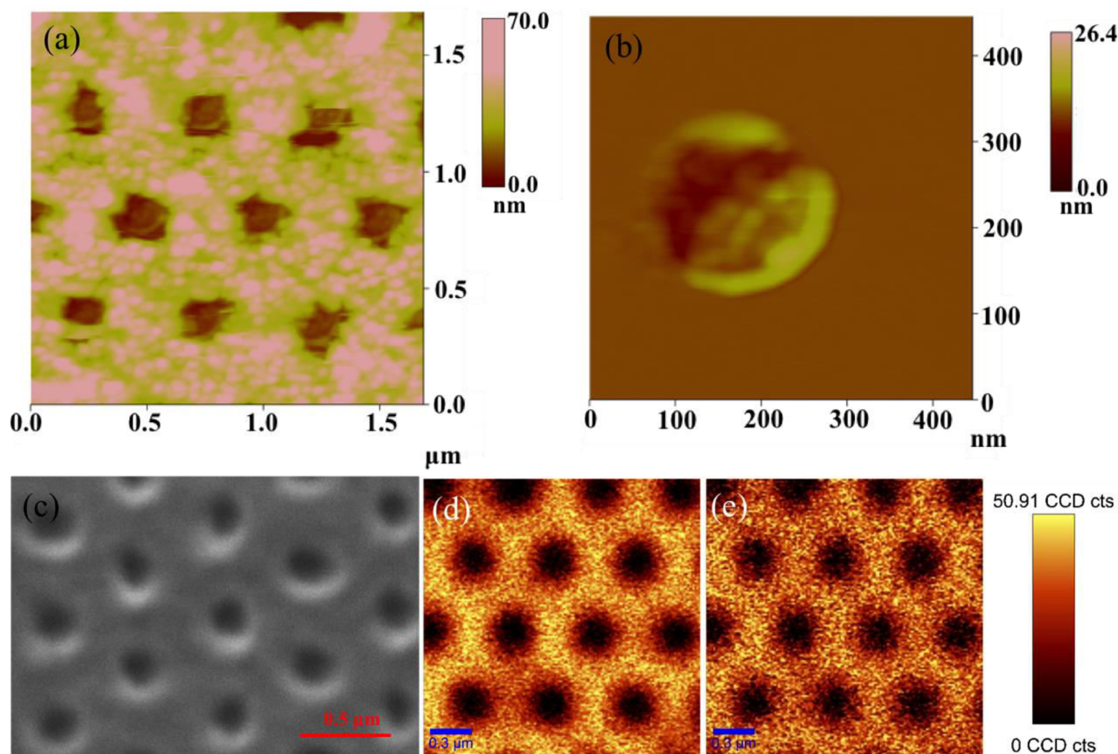


Figure 5.14. (a) AFM image, (b) zoomed in AFM image of single hole region, and (c) SEM image of graphene hole array on silicon substrate after 1nm copper deposition. Raman mapping of (d) G and (e) 2D band on graphene hole array sample on silicon with 1 nm thick deposited copper.

To perform this research, mechanically exfoliated graphene on a silicon substrate was first patterned into a nanohole array template. Then, copper was deposited inside exposed hole regions of the templated graphene hole array, and the sample exposed to CVD graphene deposition conditions. Graphene templated hole arrays were produced from mechanically exfoliated graphene, patterned with a PMMA coating coupled with heated stamp process, copper was evaporated onto the surface followed by resist removal, and the sample placed into a heated furnace at 1000°C under CVD growth conditions. Analysis of the substrate surface after 1 nm of copper was e-beam evaporated onto the sample surface followed by resist removal is illustrated in Figure 5.14. It is clear from the AFM image in part (a) a large portion of the resist surrounding the graphene patterned holes still remains. The outline of the approximately 250 nm diameter holes is somewhat

visible under the resist, but is primarily masked by the surrounding resist residue. The SEM image in part (c) shows slightly distorted outlines of these holes most likely due to the residual polymer interfering with signal collection. A clearer picture of the individual hole characteristics is exhibited in the zoomed in AFM image in part (b) of this figure, after applying a larger scanning force with the AFM tip to clear away surrounding debris. Small particles are apparent inside the hole, with a majority clustering around the outer edges. This is to be expected considering the percolation threshold, or the evaporated copper thickness needed to produce homogenous copper films on silicon surfaces has been found to be somewhere between 5 and 8 nm.[69] Below this level, thin copper films create small islands on the silicon surface due to relative surface energies and surface tension values. It is most likely these particles initially exist as reduced copper on the silicon surface due to the high vacuum conditions for e-beam evaporation. However, upon exposure to oxygen during the acetone rinse to remove the PMMA resist, they are most likely oxidized considering their small size in the range of 10-20 nm. Furthermore, the thermal heating and low vacuum conditions when undergoing regrowth of graphene inside the hole array template further promote the likelihood of copper oxidation. The Raman mappings of the graphene G and 2D peaks are illustrated in Figure 5.14-d,e for the sample surface after 1 nm copper deposition and resist removal from the graphene hole template. The maps depict strong graphene signals in the areas of the graphene hole array template, and the signal significantly drops to an undetectable amount in the exposed hole areas where only evaporated copper is present. These maps will be used for an important comparison for graphene deposition upon exposure of this sample to CVD graphene deposition conditions.

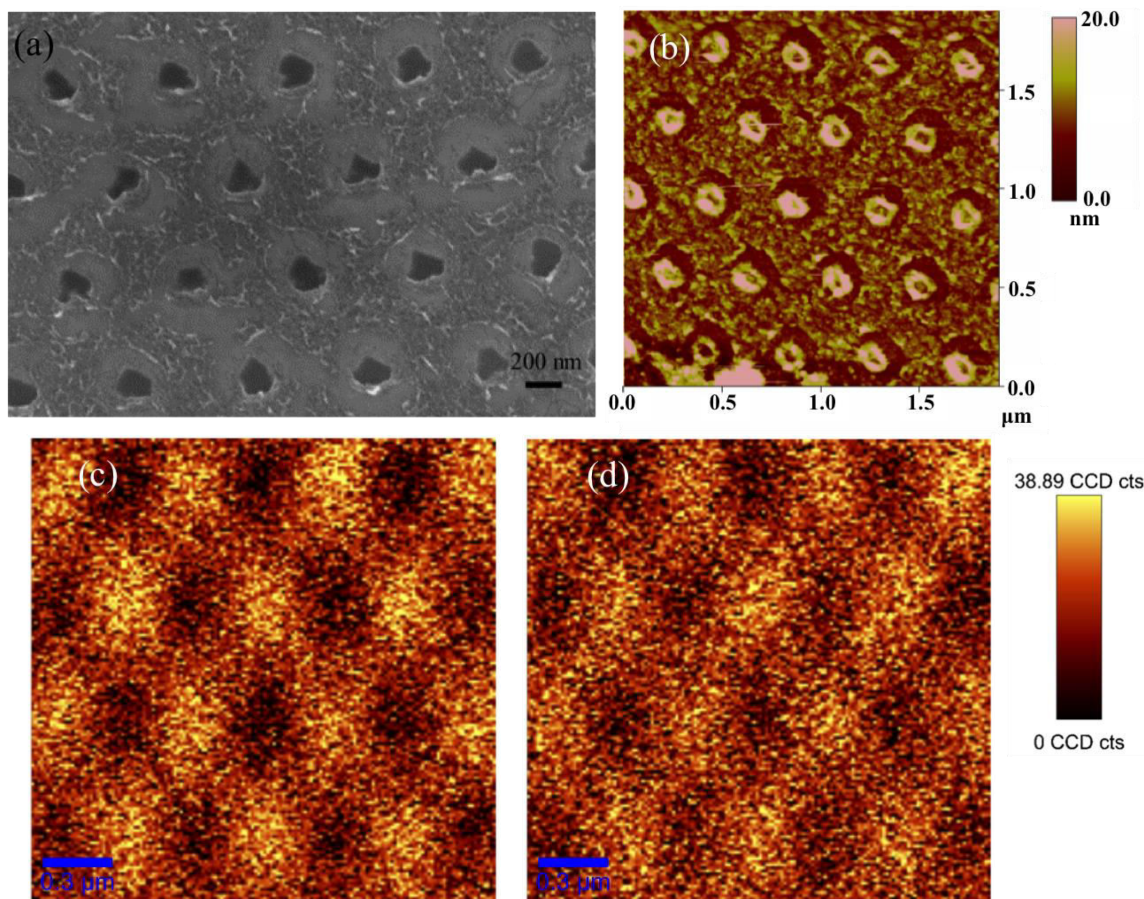


Figure 5.15. (a) SEM image and (b) AFM image of graphene hole array on silicon substrate after 1nm copper deposition and CVD graphene deposition. Raman mapping of (c) G and (d) 2D band on graphene hole array sample on silicon with 1 nm thick deposited copper and CVD graphene deposition.

The results of CVD graphene regrowth in the graphene hole arrays with 1 nm deposited copper are exhibited in Figure 5.15. The SEM image in (a) shows a change in the geometry of the dark region inside the holes to smaller irregular shapes, suggesting some sort of growth at the edge of the holes to reduce the size of the exposed hole regions. Some of these edges are faceted and form triangular formations, suggesting a possible (111) orientation around these outer edges. A clearer image of the surface morphology of this sample is highlighted in part (b) with an AFM image. In comparison to the SEM image, repeated circular shapes raised in height approximately 15 nm above the surface are found within the templated holes, centered in the middle of the hole in

relatively the same location. The repetitive pattern indicates these features are most likely not random debri on the surface, but resulting structures from the CVD growth process. The 250 nm diameter outline of the hole is evident in the image, with a very flat region inside the hole between the perimeter and the raised circular formations, suggesting potential graphene deposition in these flat spaces. To confirm potential graphene deposition, Raman mapping was again performed, investigating the intensity distribution of the G and 2D peak signals across the surface, which is displayed in Figure 5.15-c,d. The contrasting signal distribution between the graphene templated region and areas inside the holes has reduced, showing more detectable signal intensity around the outer edges of the patterned holes. This result could be from graphene deposition around the outer edges of the holes, leaving some regions of significantly reduced signal near the center of the hole region. It is difficult to pinpoint the exact region of graphene deposition considering the area of the laser light on the sample for Raman mapping is around 200 nm, which limits the resolution. However, there is some notable change in the signal around the holes, which at least demonstrates probable graphene growth.

The tall circular-shaped structures in the center of each patterned hole are quite unique, and simple solvent exposure experiments were performed to gain some insight as to the composition of these surface formations. The graphene template with 1 nm thick deposited copper with successive graphene growth was exposed to several solvents to potentially dissolve these features and observe possible changes via AFM inspection. Initially, the sample was placed into pure acetone and chloroform for several days to rid of any residual polymer remaining on the surface. From the AFM images in (a) and (b) of Figure 5.16, there is no alteration of the circular features, indicating they are not a

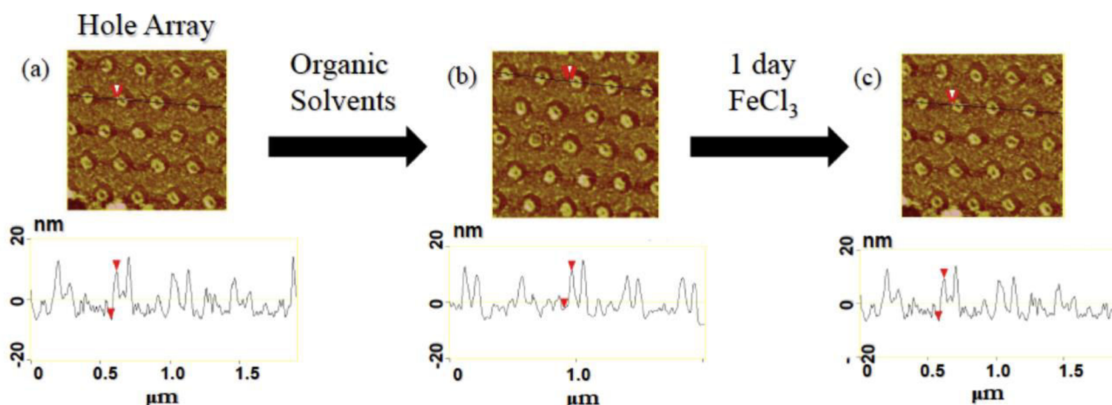


Figure 5.16. AFM images with cross sections of a graphene hole template with 1 nm thick evaporated copper, followed by (a) graphene growth and several day exposure to (b) pure organic solvents and (c) 0.1 M $FeCl_3$.

result of lingering PMMA on the substrate surface. Secondly, if the composition was of reduced copper, a 0.1 M $FeCl_3$ solution should dissolve any copper on the surface, seeing as this solution is used to dissolve the bulk copper substrate from CVD graphene in previous experiments. The AFM image in Figure 5.15-c again indicates no change in surface morphology upon iron chloride exposure over a several day period, so these features must not be exposed reduced copper. If there existed any surface copper oxide, subjection to a dilute sulfuric acid solution has been shown to easily dissolve copper oxide. After placing the sample in a 0.1 M sulfuric acid solution for a period of 2 days, again the tall circular features remained and did not disappear through dissolution. These results indicate these raised features may be potentially covered with a graphene layer which would protect them from decomposition in these solvents, or it is possibly composed of some other hydrocarbon species that is resistant to dissolution in these solvents.

For a comparison, a similar sample of CVD graphene deposition was made on a graphene hole array template instituting 5 nm thick layer of deposited copper on the surface to see how the presence of more copper would change potential graphene growth

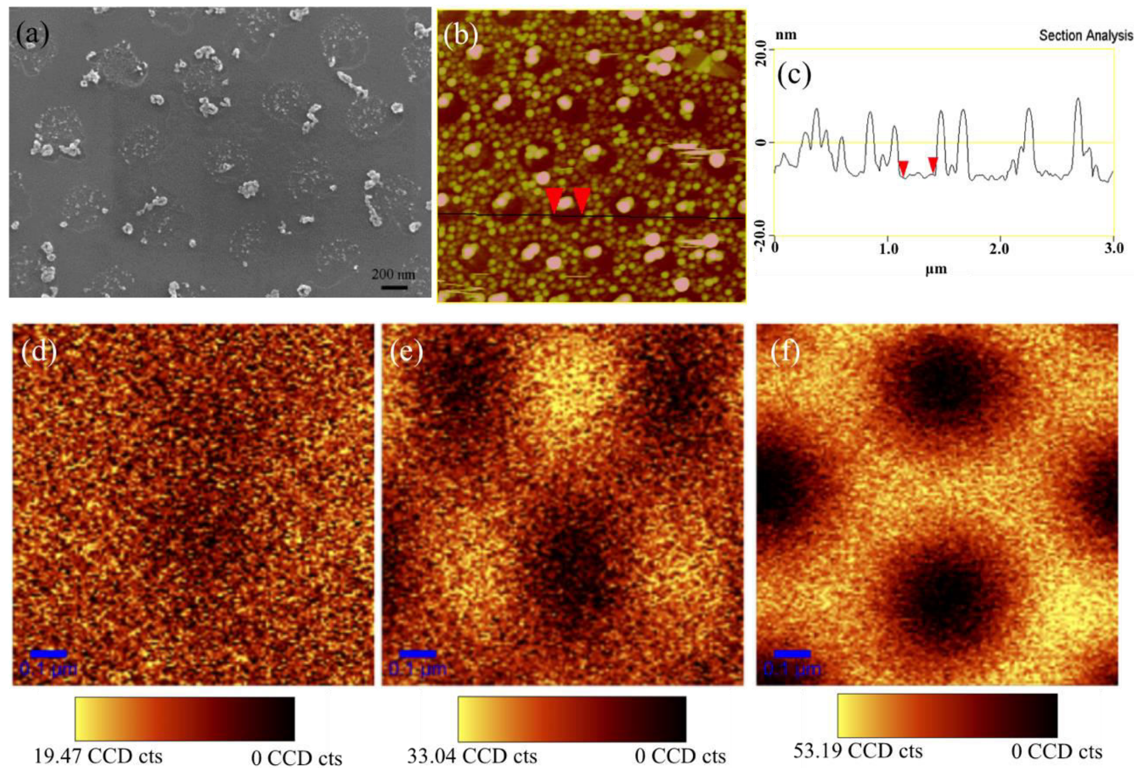


Figure 5.17. (a) SEM image and (b) AFM image with (c) cross section of graphene hole array on silicon substrate after 5 nm copper deposition and CVD graphene deposition. G band Raman mapping of templated graphene hole array with (d) 5 nm thick deposited copper and graphene deposition, (e) 1 nm thick deposited copper and graphene deposition, and (f) 1 nm thick deposited copper with no graphene deposition.

within the graphene hole template. The results are exhibited in Figure 5.17. The SEM image in (a) does not show any dark region inside the hole shapes, indicating they are completely filled with conductive material similar to the graphene template. The AFM image in (b) depicts a large globular formation in the relatively same central locale within each patterned hole. Similar to the deposition on the sample with only 1 nm of deposited copper, the region between the outer edge of the holes and the aggregated formation near its center is relatively flat. The G band Raman mapping for a single hole is illustrated in Figure 5.17-d. It is apparent the distribution of the Raman peak signal becomes more homogeneous across the hole for this sample. The G band Raman maps for zoomed in

areas on the graphene hole arrays with 1 nm thick evaporated copper with subsequent graphene growth (e) and 1 nm thick deposited copper with no graphene regrowth (f) are shown for comparison purposes. These show reduced peak intensity near the center of the holes, implying there is no graphene present near the center region of the hole.

From the accumulation of this data, it is supposed the graphene template acts as a foundation to generate further graphene growth from the perimeter of the patterned holes toward the center of the hole. At the high deposition temperature of 1000°C, the likely oxidized copper nanoparticles from e-beam evaporation of copper within the graphene template can migrate among the area within the hole, and propagate to the edge of the patterned holes. It has been extensively studied that CVD graphene deposition occurs with dispersed graphene nucleation in regions across the copper surface, followed by outward growth of these areas across the substrate surface. Thus, it is not surprising the graphene template would act similarly as a site to continue graphene deposition. The edge of the hole array would provide a lower surface energy placement for this nanoparticles in relation to a flat exposed surface, so the movement of the particles to a step-edge region is quite probable. Upon introduction of the methane gas carbon source, the copper oxide particles may become potentially reduced at the surface, initiating a graphene coating over their surface as well as promote graphene growth from the graphene template edge inward. This process would account for the tall circular features within the templated holes after graphene regrowth, and additionally the inability to dissolved these structures in a variety of solvents. It is believed the copper oxide particles may move toward the center of the hole during graphene formation because they may be extremely mobile across the surface at the elevated temperatures, allowing them

to easily move and be displaced as graphene is formed at the edge of the hole array template. Additionally, it may be more energetically favorable for the graphene to remain in a flat orientation on the silicon surface rather than be in a curved structure coating the copper particles. Graphene with high curvature has been shown to experience significant strain, even enough to induce significant defects in the graphene structure.[70] Thus, the copper could be displaced toward the center of the nanohole for the graphene to remain favorably flat. Over time, or with the presence of a larger amount of copper as with the 5 nm thick evaporated copper, graphene production from the template can cover the entire exposed region of the templated hole. Consequently, the circular-type formation will aggregate into one globular formation within the central region of the hole, and the Raman mapping of the hole region to go from a contrasting signal within and outside of the hole to a homogenous signal for the same area. Further time-sequenced studies examining how the surface of templated graphene arrays with regrown graphene change over time specific periods during the deposition process would hopefully allow better confirmation of this proposed hypothesis.

5.5 Conclusions

The research described in this chapter has focused on fundamental investigations of graphene growth that will aid in developing methods for production of high quality, continuous, single-layer graphene films over large surface areas for numerous applications envisioned for graphene. To improve conductivity and lower defect density, it is first imperative to know if differences in copper substrate features may influence graphene quality, which was the initial objective. To fulfill this goal, graphene was deposited by the CVD process on polycrystalline copper and CTO-Cu, which is copper

foil specially treated to align grain angles and produce a predominant surface orientation of (100). The morphological, optical, and electrical properties of the graphene on these substrates were then compared. Graphene on polycrystalline copper displayed a rough morphology with somewhat aligned peaks and valleys, slightly similar to the bare polycrystalline surface, but different enough to suggest a copper surface reconstruction underneath its graphene coating. The bare CTO-Cu surface was quite flat, and demonstrated a change after CVD graphene deposition to large-scale features, also strongly indicating a reconstruction of the abundant copper under the graphene film. The graphene on polycrystalline copper further showed behavior of defect-rich graphene by a comparatively large D peak in its Raman spectra, decreased transmittance across the visible spectrum, and a 20% lower conductivity value in relation to the graphene on CTO-Cu. All of these differences imply there is an influence from specific traits of the copper substrate on formation and quality of CVD graphene.

The second objective of this research was to further understand this specific dependence with the features of CTO-Cu and to elucidate details of the graphene deposition mechanism on this copper substrate. Graphene was deposited on CTO-Cu for shortened periods of time, and a multitude of properties probed. It was found during the initial deposition stages, small localized regions across the substrate surface begin to reconstruct into raised right-angle triangle structures that are principally aligned along a single axis, indicating an influence of the aligned grains of the special-treated CTO-Cu with its chiefly (100) lattice. These structures grow in size until their edges begin to coalesce, covering the entire copper substrate surface. The primarily Cu (100) surface reconstructs to a (111) lattice to initiate growth of graphene, which shares a closely

matched lattice constant with the (111) orientation. The principal component at the copper interface is believed to be a thick copper oxide considering the likely presence of oxygen and high deposition temperatures, however a several nanometer thick reduced copper layer is believed to reside between the oxide and graphene due to EBSD measurements. With all this information, the mechanism of graphene deposition is proposed to begin by formation of a thin melted Cu-O-H layer at the copper oxide surface, followed by formation and aggregation of reconstructed copper oxide (111) nanoparticles into aligned right triangles, as directed by the (100) substrate. Upon reduction at the surface regions of the copper oxide nanoparticles to a thin Cu^0 coating, graphene may deposit cover the surface of the triangle structures, and over time cover the entire substrate surface.

To expand on the second objective, graphene was deposited on polycrystalline copper by the CVD process and compared to graphene on CTO-Cu in order to ascertain how the deposition mechanism or graphene formation may change upon significant changes in the copper substrate features. In comparison to the traits of CTO-Cu, polycrystalline copper is well known for its randomly aligned micron-scale grains of several crystal orientations, such as Cu (100), Cu (111), and Cu (110). As a result, the initial stages of graphene development on this substrate did not demonstrate any specific structural alignment or organized geometric arrangement on the sample surface as found in the CTO-Cu samples, even though restructuring of the surface did take place into large irregular features with faceted characteristics. The polycrystalline copper present under the CVD graphene did not display a clear favor to reconstruct to a (111) crystal orientation on these faceted structures, and illustrates a variety of other orientations

including (100) and (110). As a result, the graphene present on the faceted formations displayed behavior of a film with a higher defect density, which is expected for graphene on crystal lattices other than (111). It is evident the special-treated CTO-Cu with its highly aligned grains and (100) orientation must promote formation of aligned triangle features on the copper substrate surface during the initial heating stages of the CVD process, since this is not observed when initially heating the polycrystalline copper. Furthermore, the thermally treated CTO-Cu surface must facilitate the reconstruction of the surface to the energetically-favorable (111) orientation, seeing as the multitude of lattice orientations still remain on the polycrystalline copper substrate after CVD graphene deposition. These differences produce graphene on the CTO-Cu foil with aligned grains, smaller defect density, and consequently higher quality. These results are promising to be able to manipulate copper foil surfaces and generate graphene with aligned grains to improve electron mobility for more successful implementation of graphene as a transparent electrode, as well as form graphene on a mostly insulating metallic oxide surface.

Another means to produce CVD graphene on insulating substrates, and the third aim of this research, was to utilize graphene templates and thin, selectively deposited copper to initiate further growth from the graphene template across an insulating material surface. Templated graphene hole arrays were produced on insulating silicon substrates, followed by selective copper deposition within the bare hole regions, and the sample exposed to CVD graphene deposition conditions. Following graphene growth when only 1 nm of copper was deposited, tall circular disk-like features were revealed near the center of all holes within the templated structure. The region between the edge of the

template hole and tall feature was very flat, much flatter than the patterned graphene, which most likely retained some residual resist from the patterning process. The Raman spectra showed an increase in 2D and G signal intensity around the outer edges of the holes after graphene deposition. In comparison, the sample with 5 nm of deposited copper and graphene deposition exhibited a large globular formation located at approximately the center of all the templated holes, and a further increase in Raman signal intensity across the hole structures. It is proposed during the exposure of the templated graphene array with copper to CVD graphene growth conditions, the deposited copper becomes oxidized and migrates to the energetically-favorable edge sites of the hole array. There, the surface of the copper may potentially be reduced and promote graphene assembly from the edge site, and the copper species at the edge site may move inward as the graphene edge closes the hole area. The chemical composition of the raised circular structures still remains undetermined and it is still unclear if this proposed deposition hypothesis is accurate, but further time-sequenced and composition experiments would allow for better clarification. The primitive initial findings still show potential for graphene deposition from graphene template edges on insulating substrates, and with further inquiry would provide a means to overcome the limitation of CVD graphene deposition on bulk metallic substrates, and the difficulties included in transfer to dielectric materials. Overall, through a detailed understanding of the graphene growth mechanism, it may be possible to manipulate the growth by controlling the substrate structure, processing conditions, or even templating the growth of graphene on insulating substrates.

5.6 References

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Liu, Jianwei; Xu, Guowei, Rochford, Caitlin; Lu, Rongtao; Wu, Judy; Edwards, Christina M.; Berrie, Cindy L.; Chen, Zhijun; Maroni, Victor. Doped graphene nanohole arrays for flexible transparent electrodes. *Applied Physics Letters* **2011,** *99*, 023111.

Chapter 6: Doped Graphene Nanohole Arrays

6.1 Abstract

Graphene nanohole arrays (GNAs) were fabricated by nanoimprint lithography and doped with thionyl chloride for potential application as a superior transparent electrode alternative to indium tin oxide. Before doping, the optical transmittance of single-layer graphene increased 2-3% across the entire visible region of the light spectrum, primarily due to the reduced surface coverage of the nanohole array structure, and only reduced slightly after doping. Graphene doping was enhanced by the exposed edge sites of the nanoholes within the array, and led to a conductance enhancement 15-18 times greater than its undoped counterpart, whereas unpatterned single-layer graphene illustrated only a 2-4 enhancement factor following dopant exposure. These data reflect the promise doped GNAs may play for improving both optical transmittance and electrical conductivity of graphene-based transparent conductors.

6.2 Introduction

Graphene is an attractive material for current implementation into several research fields due to its attractive qualities such as high charge mobility,[1,2,3] mechanical and chemical robustness,[4,5,6] high optical transmittance,[7,8,5] and flexibility to conform to a wide variety of surfaces.[8,9] In particular, the area of photovoltaics is focused on graphene incorporation into solar cells and as a replacement transparent conductor for contemporary devices. Presently, indium tin oxide (ITO) is the most commonly used transparent conductor in the market due to low sheet resistance values (10-30 Ω/square), decent optical transparency (>90% at 550 nm), a advantageous work function, and ease of fabrication.[10] However, there are several drawbacks to ITO that severely limit its widespread function as a transparent electrode. One such problem is that world's supply of indium is slowly depleting which is driving up the price of the rare element. Furthermore, the preparation of ITO thin films is costly, ITO is brittle and can easily fracture, and its optical transparency decreases dramatically at longer visible wavelengths.[10] Consequently, there is a drive to discover alternate sources for transparent conductor applications.

Graphene is a promising replacement for ITO as a result of its high electrical conductivity,[11] high optical transmittance in the visible region of the light spectrum,[12] and a favorable work function of ~4.42 eV for a suitable hole-collecting electrode.[13,14] A single layer of graphene absorbs only about 2.3% of incident white light[15] and its predicted sheet resistance is approximately 31 Ω/square,[2] which is comparable to ITO. Unfortunately, the experimentally observed range of graphene sheet resistance values is approximately 125 to 10,000 Ω/square,[10,16] which is significantly lower than the ideal

single layer graphene values. Furthermore, the most hopeful method to produce large area single layer graphene, chemical vapor deposition (CVD) on metallic substrates, falls near the higher end of this range. In order to improve sheet resist values, some researchers have attempted to stack multiple layers of graphene. The total sheet resistance was reduced by almost an order of magnitude for a 4-layer stacking, but the optical transmittance was adversely affected, and decreased by up to 10% when compared to single layer CVD graphene.[16] Another approach to improve conductivity is by chemical doping of the graphene layer. Chemical doping can be performed via various methods, including gating, substitutional doping, and chemical doping.[17] Electrical gating includes the application of bias voltages up to 100 V for device functionality, and is therefore unattractive.[18] Substitutional doping involves replacement of a carbon atom in the graphene hexagonal lattice with another atom, usually boron or nitrogen, and leds to disorder in the graphene, lowering its electron mobility.[18] Chemical doping involves interaction of adsorbed species on the graphene surface, or chemical interactions at defect sites or edges, which either withdraw or inject electrons into the graphene layer, thereby p-doping or n-doping the graphene. Chemical doping by surface adsorption of metal nanoparticles,[19,20,21] HNO_3,[16,22] NO_2,[23] and a host of other species have shown to increase the electron mobility of graphene, however these adsorbed components either negatively affect optical transparency or degrade over time.[18] For successful improvement of graphene as a transparent via chemical doping, it is thus crucial to uncover a means to enhance electrical conductivity without decreasing optical transmittance.

Research has shown doping carbon nanotubes and pristine graphene with thionyl chloride improves conductivity significantly.[24] Thionyl chloride ($SOCl_2$) is thought to break down in the vapor phase to form chlorine anions, which adsorb onto the graphene surface and further react with delocalized π electrons in the conjugated graphene lattice.[24] The reaction occurs preferentially at the energetically favorable edge and defect sites. Through this method, a piece of mechanically exfoliated graphene doped with $SOCl_2$ demonstrated a 44% reduction in sheet resistance, and no change in transmittance values as compared to undoped pristine graphene over the visible region of the light spectrum.[24] The large drawback to this method, however, is mechanically exfoliated graphene has a small defect density,[25] as thus the active doping sites are limited.

One way to build on these findings to improve conductivity without adversely influencing transmittance values would be through the implementation of graphene nanohole arrays (GNAs). Graphene nanohole arrays provide an increased density of edge sites for chemical doping[7] to take place while simultaneously reducing graphene surface coverage to lower optical absorption. Thereby, increasing the potential to tune the electrical properties of graphene more effectively and efficiently without decreasing transmittace. The research presented here investigates the impact $SOCl_2$ doped GNAs have on conductivity and optical transmittance as compared to unpatterned graphene and undoped graphene hole arrays. It is the hope to provide a means to significantly increase conductivity of single layer graphene while possibly increasing its optical transparency.

6.3 Materials and Methods

6.3.1 CVD Graphene Deposition and Transfer Process

Polycrystalline copper foils were purchased commercially from Alpha Aesar (No. 13382) with a 25 μm thickness. Chemical vapor deposition was performed on cut 2x2 cm^2 foils. The foil was placed in a quartz tube and heated to 1000°C under 0.1 sccm H_2 flow. Upon reaching the deposition temperature, CH_4 gas was introduced at a flow rate of 3.0 sccm for 30 minutes. Following graphene film formation, the apparatus with sample were allowed to cool to room temperature.

The graphene films were transferred to silicon substrates for characterization and analysis. The transfer process consisted of spin coating of poly-methyl methacrylate (PMMA) onto the graphene/copper surface. The copper component of the sample was subjected to a 0.1 g/mL solution of iron chloride to remove the copper substrate. The remaining graphene/PMMA was rinsed extensively and soaked with deionized water. The target silicon substrate with thermal oxide was aligned beneath the graphene/PMMA sample, the deionized water drained, and the sample placed in an oven for one hour at 80°C to eliminate residual moisture. Lastly, the PMMA polymer was removed with an acetone rinse.

6.3.2 Graphene Nanohole Array (GNA) Formation by Nanoimprint Lithography (NIL)

Following graphene transfer to a silicon substrate, a resist (mr-I 7030R, Microresist Corp) with a 300 nm thickness was spin coated onto the graphene surface. The sample was baked on a hot plate at 100°C for 1 minute. An NIL mold (LightSmyth Technologies) with a hexagonal array of posts with a diameter of 240 nm and a period of

600 nm was treated with FDTS (1H, 1H, 2H, 2H-perfluorodecyl-trichlorosilane) to facilitate easy release of the mold from the spin-coated resist. The NIL mold was positioned over the resist-covered graphene, and both were heated to 140-180°C with subsequent application of 20-50 bar pressure for 4 minutes. The mold/resist/graphene sample was then allowed to cool to a temperature of 50°C, whereby the mold was released from the resist/graphene component, and further cooled to ambient temperature. The sample was then etched with O_2 plasma by reactive ion etching (RIE) for 4 minutes (O_2 flow 10 sccm, chamber pressure 7.80 mTorr, RIE power 20 W). The residual resist was removed with an acetone rinse and the sample dried with N_2 gas. To further remove remaining polymer deposits, the surface was exposed to a mixture of H_2 (500 sccm) and Ar (486 sccm) gas at 400°C for 1 hour.

6.3.3 Doping GNA with $SOCl_2$

The pristine graphene or GNA samples were placed in a N_2-filled glove box face down over a vial with $SOCl_2$ and exposed to its vapor for 15 minutes at room temperature.

6.3.4 Characterization of Undoped and Doped Graphene and GNA Samples

Surface morphology was examined by SEM and AFM imaging. SEM imaging was performed with Joel JSM-630 and Leo 1550 FESEM instruments with the electron beam accelerating voltage at 2-25 KeV. AFM images were obtained in ambient conditions using a Nanoscope E Atomic Force Microscope (Veeco Instruments, Santa Barbara CA) operating in contact mode. Veeco silicon nitride tips (NSC35, Mikromasch)

with a force constant of 0.12 N/m were scanned at 2 Hz with a setpoint of approximately 1.5 V. Images were flattened before cross section analysis.

The Raman spectrum of CVD graphene was obtained with a Renishaw InVia Raman Microprobe with helium-cadmium laser. The excitation wavelength was 442 nm. The laser spot diameter was approximately 2 microns, and its energy density 1 mW/μm^2. The spectrum shown here was an average of 10 scans.

Optical properties were probed by collection of visible transmittance spectra with a Cornerstone monochromator (Newport 74004) with Xe arc lamp illuminator (Newport 70611) calibrated with a UV-Si photodiode (Newport 71640). The electrical properties were explored by sheet resistance measurements and I-V curves. The sheet resistance measurements were collected with a four-point-probe apparatus. The IV curves were collected by making electrode contacts (15 nm titanium and 65 nm gold) to the graphene samples with a 3.2 μm spacing between electrodes.

6.4 Results and Discussion

Graphene was initially deposited onto copper foils by chemical vapor deposition and characterized prior to hole array patterning and doping. A Raman spectrum and SEM

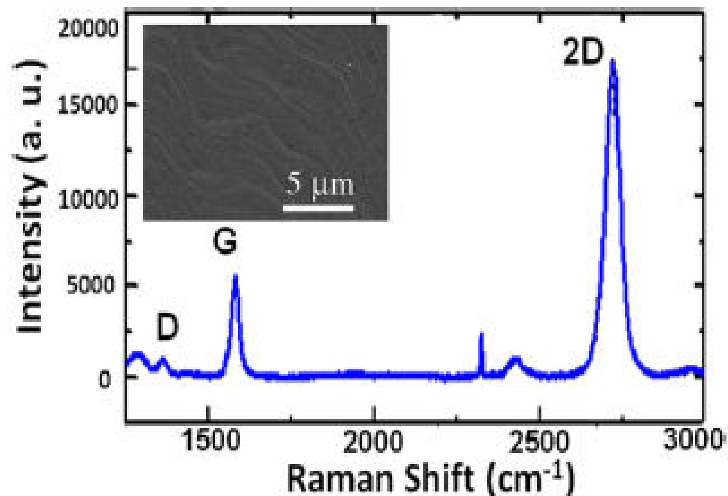

Figure 6.1. Raman spectrum of graphene on copper foil. Inset: SEM image of graphene grown on copper foil using CVD method.

image were collected to characterize the sample, and the results are depicted in Figure 6.1. The G peak at 1580 cm^{-1} is generated from the doubly degenerate zone center E_{2g} mode, the breathing mode for the rings in graphene, and the 2D peak at ~2720 cm^{-1} results from the second order of zone-boundary phonons in graphene.[26] Both of these peaks are commonly used to indicate the presence of graphene on a substrate surface, and their signal intensity ratio specifies the number of graphene layers. Here, the intensity of the 2D peak is at least 2 times greater than that of the G peak and the peaks have a symmetric shape, strongly suggesting single layer graphene on the copper substrate surface.[26,27] The D peak at the far left of the Raman spectrum is used to qualitatively determine the amount of graphene defects.[26,27] Its relatively low intensity in the figure above implies a small defect density on the graphene surface. The morphology of the graphene/copper substrate surface can be observed by the SEM image inset of Figure 6.1. The image displays some graphene wrinkles, but mostly a continuous graphene layer is spread throughout the entire sample surface.

After the single layer CVD graphene was characterized, the CVD graphene was transferred to a silicon substrate and GNAs were made by NIL. The hexagonal pattern of holes can be observed in Figure 6.2 with SEM and AFM images representing before and after NIL resist removal. The graphene surface coated with NIL resist and after stamping with the NIL mold is illustrated in the inset of Figure 6.2 -a. The image depicts a darker colored GNA template region surrounding brightly colored holes. The brightness is likely a result of the edge effect in SEM, where more secondary electrons are allowed to escape and reach the detector from the exposed step surface area, and/or charging of the insulating silicon substrate underlying the GNA template.[28] The diameter of the holes is

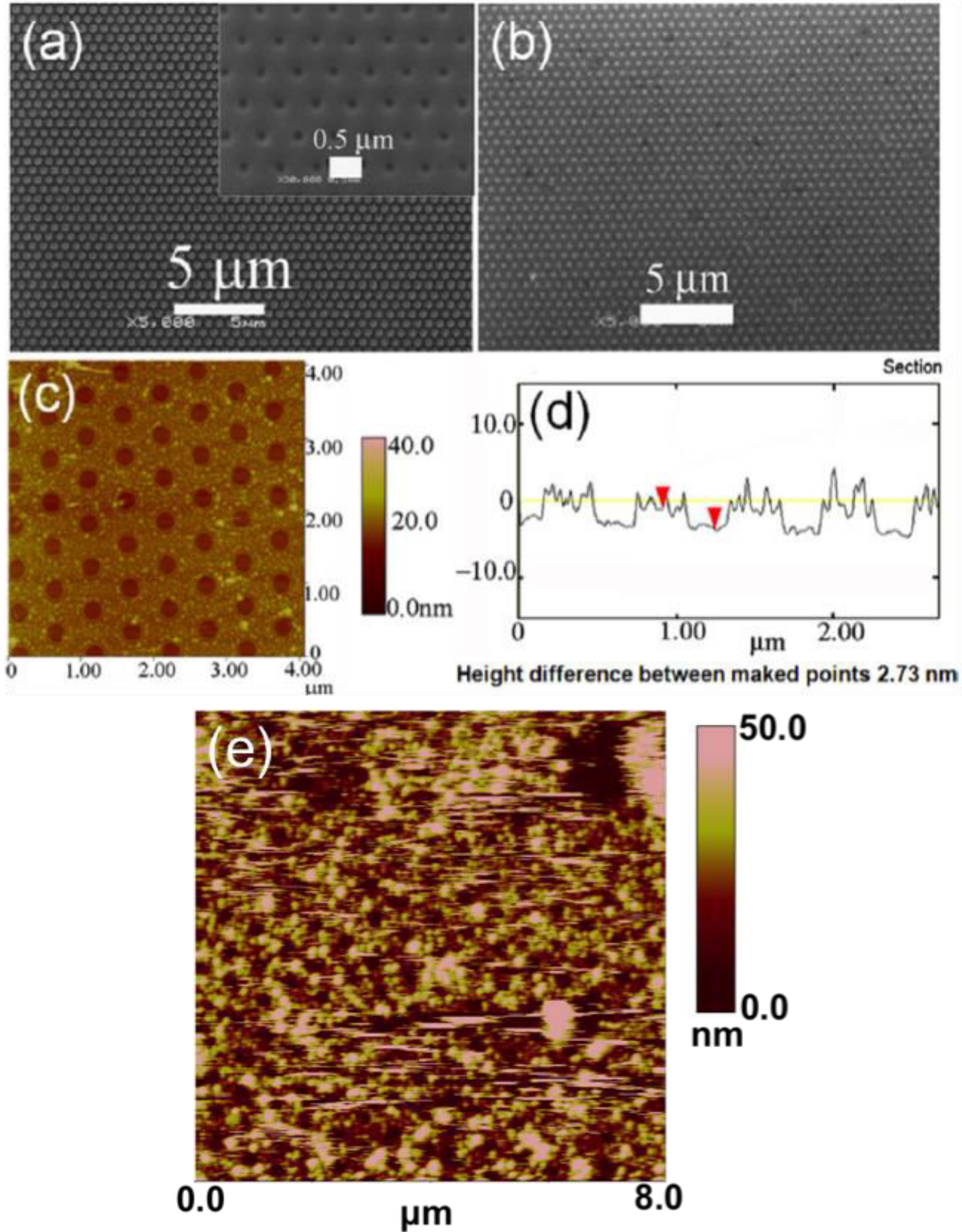

Figure 6.2. SEM and AFM images of GNAs: (a) GNAs after RIE, before PMMA removal (inset: the same sample before RIE). (b) after PMMA removal with acetone followed by hydrogen/argon annealing. (c) AFM image and (d) cross section of GNAs after annealing. (e) AFM image of GNA after acetone rinse and without hydrogen/argon annealing.

245 ± 15 nm and the hexagonal lattice constant is ~590 nm, which is in close agreement to the dimensions of the NIL stamp molding. Following stamping of the NIL resist, the

sample was subject to reactive-ion etching (RIE) with O_2 plasma to pattern the underlying graphene into a nanohole array, and the NIL resist removed by an acetone rinse. The graphene hole diameter increased to 260 ± 15 nm after RIE as depicted in the SEM image in part (a) of this figure. The acetone rinse was not sufficient to completely remove the NIL polymer resist as apparent from the prominent amount of debris remaining on the surface, as illustrated by the AFM image in Figure 6.2-e. The graphene hole template is vaguely seen amongst the significant residue in the image, however the debris inhibits the collection of a well-defined image of the GNA and the ability to observe a sharp step-edge at the perimeter of the nanoholes. A second NIL resist removal step with Ar/H_2 annealing at 400°C for one hour helped to diminish the amount of residual resist as seen in the SEM and AFM images in parts (b) – (d). This method has been established to help remove polymer residues on from transferred graphene.[29] Circular holes with distinct edges in an array pattern appear in these images, even though some roughness still remains in the regions around the holes, probably as a consequence of a small amount of residual polymer material. This also may explain the larger than expected graphene step height of approximately 2.6 ± 0.6 nm displayed in the AFM cross section in part (d), when the experimentally observed step height of clean graphene on silicon is around 0.5 nm.[1]

Optical transmittance and resistance measurements were obtained for several samples of pristine, hole-patterned, and doped single and multi-layer graphene to investigate how the optical transmittance and conductivity may change upon stacking CVD graphene layers, as well as patterning graphene with a nanohole array arrangement with subsequent $SOCl_2$ doping. The optical transmittance spectra for 1 and 4-layer

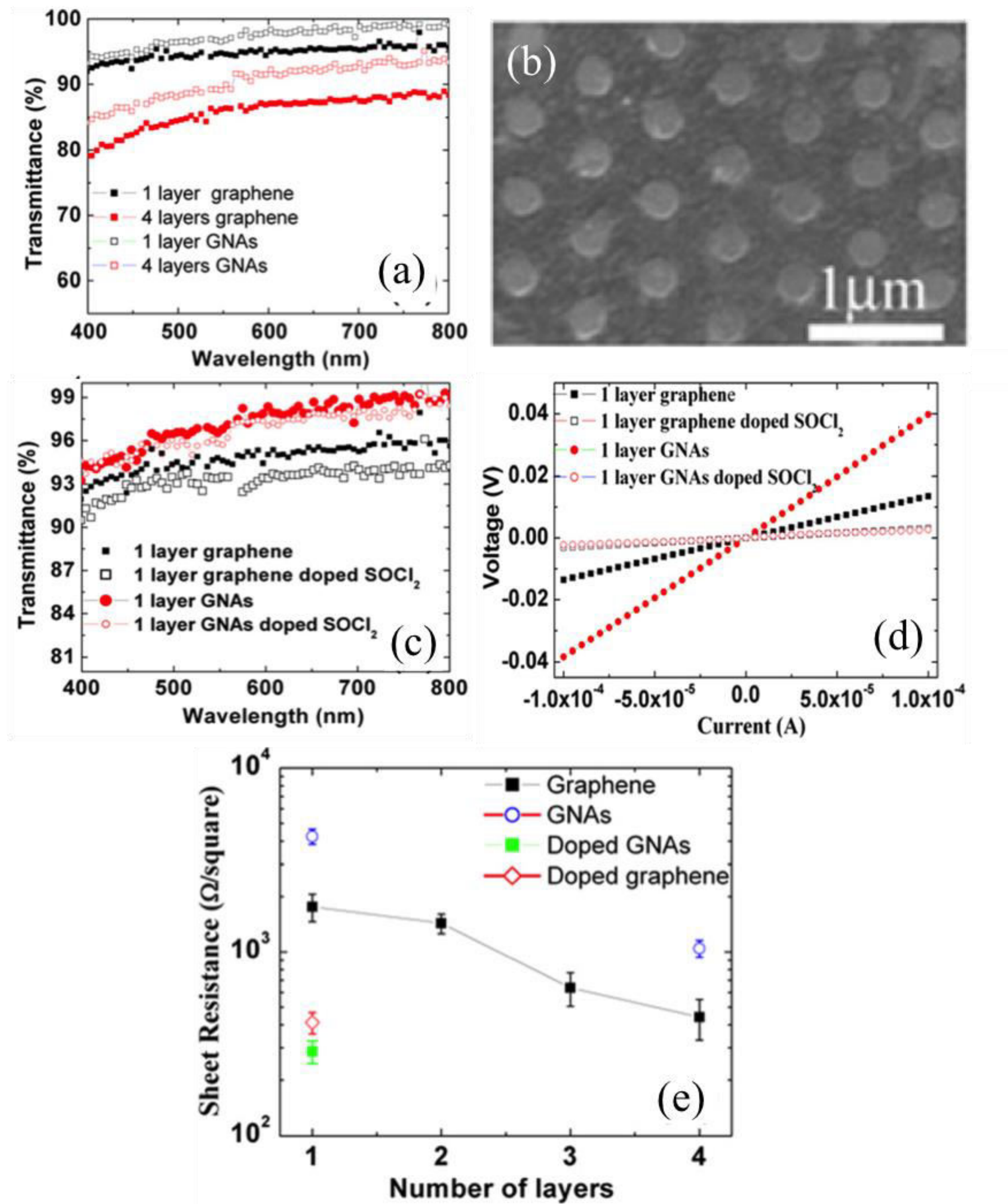

Figure 6.3. (a) Transmittance spectra of 1 and 4-layer graphene before and after GNA production. (b) SEM image of GNAs after doping. (c) Transmittance spectra of single layer unpatterned graphene and GNAbefore and after doping. (d) I-V curves of 1 layer unpatterned graphene and GNAs before and after doping. (e) Sheet resistance of undoped samples shown in Figure G-a and as well as the same samples after doping.

graphene and GNAs are shown in Figure 6.3-a. Before patterning of the CVD graphene, stacking of the unpatterned graphene layers shows a marked decrease in transmittance as expected. At 550 nm, the unpatterned single-layer graphene was found to reduce the

transmittance of the transparent silica substrate by 4.8 ± 0.6% (95.2% transmittance), with additional reductions of 3.7 ± 0.5% (91.5% transmittance) for bilayer graphene, 1.8 ± 0.3% (89.7% transmittance) for trilayer graphene, and 2.7 ± 0.5% (87.0% transmittance) for 4-layer graphene. The irregular reduction of the optical transmittance for each additional graphene layer may be a consequence of imperfections in the individual graphene films, but the overall trend of decreasing transmittance values throughout the visible spectrum as the number of stacked graphene layers increase is consistent with previous studies of optical spectra from multi-layer CVD graphene.[30] It is important to note the comparison of these results to the optical transparency of ITO. The stacked pristine graphene layers do not exhibit significant reduction in light transparency at longer wavelengths, in contrast to ITO where transmittance values can reach as low as 70% or worse at wavelengths above 750 nm.[10] This evidence coupled with the lower sheet resistance values in Figure 6.3-e for multi-layer graphene support the promise of stacked CVD graphene for improving performance of broadband optoelectronic devices by possessing better optical transparency relative to ITO and moderate sheet resistance. It is the hope, however, that further patterning of single layer graphene with a nanohole array would provide even better enhancement of the optical transparency across the visible region of the light spectrum, surpassing transmittance of ITO even at short wavelengths, and doping the GNA would produce comparable resistance value to ITO and multi-layer graphene.

Figure 6.3-a demonstrates a higher optical transparency for GNAs across the visible spectrum as compared to pristine graphene with the same number of layers. Quantitatively, the transmittance of the monolayer GNA is 97.0% at 550 nm as compared

to a reduced 95.0 % value at the same wavelength for the pristine single layer graphene. Also, the 4-layer GNA holds an 89.5% transmittance, and is significantly higher than its pristine counterpart with an 86.0% transmittance. At 750 nm, the difference between the hole-patterned and pristine 1-layer graphene increases to 3.0%, and the difference between the 4-layer GNA and stacked 4-layer unpatterned graphene increases to 5.0%. The hole array decreases the surface coverage of graphene by a factor of 0.16, which is expected to result in an improvement of less than 1% (0.16 x 5.0% absorption = 0.8% absorption reduction) in the GNA optical transmittance compared to unpatterned graphene. Since the observed transmittance improvement surpasses this expectation, it is surmised there are other factors that are influencing transmittance besides the decrease of graphene surface coverage. A potential factor could be incident light scattering or interference at the GNA hole edges in an advantageous manner. Future work is underway to determine the specific factors that contribute to this heightened increase in optical transmittance as a result of hole patterning graphene.

It is imperative for this work to not only examine the morphology and optical transmittance upon patterning to make GNAs, but to confirm doping of the GNA with $SOCl_2$ does not unfavorably influence the surface and optical transparency improvement as discussed above. The SEM image in Figure 6.3-b shows the clear hexagonal lattice of the graphene hole array remains unchanged after chemical doping of the single layer GNA. The transmittance decreased only slightly after doping of the single layer GNA and pristine graphene, as observed in the spectrum depicted in Figure 6.3-c. For quantitative comparison purposes, the transmittance decreased by 1.0% at 550 nm in the GNA after doping while it decreased by 2.0% in the unpatterned graphene. Fortunately,

there does not appear to be any significant negative effect of doping on the morphology or optical transparency of the GNA structures.

Patterning of graphene into nanohole arrays may not only change optical properties, but electrical properties, which is the main aim of this research. Sheet resistance values as well as IV curves were collected to understand how chemical doping of graphene and GNAs may impact conductivity. In Figure 6.3-d IV curves demonstrate the variations in conductivity for single layer graphene, doped single layer graphene, single layer GNA, and doped single layer GNA. The electrical conductivity increased in both pristine and patterned GNA after doping. The prior increased by only 2-4 times, and the later by 15-18 times. These results for pristine graphene doping coincide with previous findings.[24] The larger increase in conductivity for the patterned GNA after doping as compared to the pristine CVD graphene is believed to be the product of enhanced edge availability on the GNA, allowing more edge and defect sites for favorable doping injection into the single graphene layer.

A summarized comparison of sheet resistances for graphene films of various layers, patterning, and doping is displayed in the graph in Figure 6.3-e. The measurements were obtained via a four-point probe apparatus with the width between electrodes at 3.2 μm. The range of sheet resistance values for single layer CVD graphene attained here was 1450 – 2150 Ω/square, consistent with values reported by Li *et al.*[30] and Verma *et al.*,[8] but considerably higher than results acquired by Bae *et al*.[16] The difference is likely the result of a special thermal treatment and annealing step of the copper foils performed by Bae *et al*. to increase copper grain size from a few micrometers to over 100 μm. Decreased grain size and increased grain boundaries are a substantial

contributor to reduced conductivity. Furthermore, it is unclear to which substrate the graphene was transferred and electrical measurements obtained, as the graphene was transferred to several substrates in their research. It has been shown substrate interactions can act as dopants to the graphene, and transfer to a multitude of substrates can alter graphene sheet resistances almost an order of magnitude.[30]

There is a consistent drop in sheet resistance as the number of graphene layers increase of a single layer to a 4-layer stacking for both the pristine CVD graphene and GNAs, as is expected and demonstrated in prior studies.[16] As the unpatterned graphene stacking moves from a monolayer to a bilayer, trilayer, and 4-layer configuration the sheet resistance decreases by a factor of 1.2, 2.8, and 4.0 in relation to the unpatterned single layer. It would be expected after the addition of each graphene layer the sheet resistance would reduce by a factor of 2, however this is not the case. The nonuniformity in sheet resistance reduction mirrors previous findings, and is expected to be the possible outcome of defect variability of the individual graphene sheets in the stacked design, or the limited contact of the electrodes to the topmost layer of graphene forcing charge transport between graphene layers which is poorer than transport in a single graphene sheet.

The sheet resistance of the monolayer and 4-layer pristine graphene increases dramatically after patterning to form their GNA counterparts. The sheet resistance rises by 140% after hole patterning of the single layer graphene, and 100% following GNA production of the 4-layer stacked arrangement. The large difference is likely the effect of scattering at the hole edges reducing electron transport, as well as potential defect introduction during the oxygen plasma etching step. Even though there is a significant

increase in sheet resistance after nanohole patterning to ~3200 Ω/square, a substantial drop in sheet resistance occurs for the patterened single layer graphene after $SOCl_2$ doping, leading to sheet resistance value at 195 Ω/square, which resides lower than pristine doped and undoped monolayer graphene. It should be noted there is a decrease in sheet resistance between the doped pristine graphene and doped GNA, with the doped pristine graphene at 305 Ω/square and the single layer doped GNA at 195 Ω/square. It is possible considerable doping could have taken place on the CVD single layer graphene seeing as the graphene deposition took place on commercial polycrystalline copper, which is known to produce graphene with micrometer-size grains of multiple crystal orientations and a relatively large number of grain boundaries and defects. The grain boundaries may serve as defect sites in addition to other point defects for favorable chemical doping.[31] Future studies involving CVD graphene deposition on other copper substrates which produce graphene with larger grains and limited grain boundaries are promising platforms to improve conductance of GNAs and their doped equivalents on a more significant scale. However, overall, it has been shown through nanohole patterning of single layer graphene optical transmittance may be improved across the visible spectrum, overcoming absorption limitations of current ITO transparent electrodes, and this may be done while increasing doped single-layer GNA conductivity to values comparable to ITO resistance values.

6.5 Conclusions

Graphene nanohole arrays (GNA) present a promising tool to increase conductivity without diminishing optical transmittance, which is imperative for graphene's application as a transparent electrode. Multilayer stacking of graphene is a

potentially promising alternative to current ITO transparent electrodes because it displays comparable sheet resistance values and better optical transparency when 4 layers or less. The optical transmittance spectrum of 4-layer graphene does not show a drop in transmittance at longer wavelengths, and remains above 80% for the entire visible spectrum, whereas ITO transmittance has been shown to drop below this value at high wavelengths. In order to retain a high conductivity without adversely diminishing transparency, graphene nanohole arrays (GNAs) doped with $SOCl_2$ are developed and their optical and electrical behaviors studied. The fabrication of graphene nanohole arrays is possible by nanoimprint lithography of CVD graphene. The patterned GNAs decrease light absorption a small amount. Quantitatively, the single layer nanohole-patterned graphene improves light transmittance at 550 nm by 2.0 %, as well as 3.0 % at 750 nm, in relation to the unpatterned monolayer, demonstrating a slight rise in optical transparency throughout the entire visible spectrum. Doping of the GNA minutely lowers optical transmittance of single layer pristine graphene and the GNA, with the largest decrease at 2.0%. Both the single layer pristine and GNA displayed a marked increase in conductivity following dopant exposure, with their values increasing by 2-4 times and 15-18 times respectively. The larger impact of doping on the GNA is proposed to be the consequence of a heightened amount of edges from the hole array structure, which are favorable locations for doping. Even though the nanopatterning of pristine single layer CVD graphene rises the sheet resistance value to around 3200 Ω/square, doping counteracts the negative effect and lowers the sheet resistance to a minimum value of 195 Ω/square. It is clearly demonstrated both the conductivity and transparency are enhanced by nanopatterning of graphene with subsequent $SOCl_2$ doping, and such

nanohole fabrication provides a potential pathway to enhancing the performance of graphene as a transparent electrode.

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Chapter 7: Conclusions and Future Directions

7.1 Overview

The research presented in this dissertation investigated the fabrication and manipulation of materials at the nanoscale through nanopatterning and templating, specifically the production of copper nanowire features through AFM nanopatterning as well as the manufacture and manipulation of CVD graphene by substrate templating. Through these methods it has been shown that nanopatterning and templating are effective and simple methods to successfully control the dimensions of nanostructured materials, and in addition can be tools to influence the structure and properties of bulk materials developed from nanoscale and microscale templates. The ability to manufacture single nanostructured features on surfaces in selective locations and configuration, such as the copper nanowire features, illustrate advancement toward construction of nanodevices that require high selectivity over nanowire dimension and design, such as the ATP synthase nanobiodevice described in Chapter 1. The optimization of the electroless copper plating process implemented in this fabrication method is described in Chapter 3 of this work, and the details of the copper nanowire feature fabrication outlined in Chapter 4. Furthermore, through the use of copper substrate templates, as well patterned hole-array templates, it has been shown we can increase the quality of large-area CVD graphene for improved function in applications such as transparent electrodes in solar cells. This work is detailed in Chapter 5, and additional improvement of the graphene electrical properties for transparent electrode implementation is accomplished by chemical doping of graphene nanohole arrays, which is explained in Chapter 6. The ability to grow copper nanowires can be combined with

an understanding of the growth of graphene to template intricate graphene structures. The following concludes this work with summaries of the major findings included in each of these chapters, as well as the future directions envisioned for each of these research topics.

7.2 Electroless Copper Deposition – Solution Optimization Studies

7.2.1 Conclusions Summary

Electroless metal deposition shows great potential for an easy and fast means to selectively deposit copper within very thin lines. Initially, it was shown that the electroless copper plating solution presented in this work can selectively plate on exposed silicon surfaces, whereas it does not show any copper deposition behavior on SAM-coated substrates. However, most previous studies have not performed optimization experiments to determine the best concentration values for solution components to produce uniform deposited copper that is well-adhered to the surface. Furthermore, the specific roles that additives play in the metal plating process are still widely debated. Here, concentrations of each component in the electroless copper plating solution were varied, copper films deposited on bulk silicon substrates, and the properties of the deposited films probed by optical images and photographs. The following concentration values were then chosen to optimize uniformity and adhesion of copper: 0.13 M $CuSO_4$, 0.27 M NH_4F, 14 mM ascorbic acid, and 18 mM sodium tartrate. Changes in the copper sulfate concentration did not influence the uniformity or adhesion of the copper films, but simply acted as a copper ion source, and changes in its concentration led to differences in the thickness of the plated copper. Ammonium fluoride directly influences the rate of

deposition, and at higher concentrations induces large branch-like formation across the substrate surface, which are likely stress-induced restructuring of the copper films due to the high deposition rate. This same behavior is observed upon the addition of ascorbic acid, which also increases the deposition rate when added to the solution. It is necessary for addition to the electroless deposition solution, however, to promote strong adhesion of the plated copper to the silicon substrate surface. In order to overcome this drawback, sodium tartrate is added to the solution to chelate copper ions, and slow down the deposition rate to prevent formation of these stress-induced features, as well as promote uniform copper deposition across the sample surface. Clearly, the properties of the copper plated manufactured films via this method are very sensitive to solution conditions, and variation of the electroless plating solution can be used to manipulate the quality and characteristics of the copper thin films.

7.2.2 Future Directions

Even though studies have been performed here to investigate the potential role that the sodium tartrate and ascorbic acid may play in the electroless copper deposition mechanism, it still remains unclear as to how ascorbic acid promotes adhesion onto the silicon surface. Previous researchers have claimed it is because ascorbic acid acts as a hydrogen scavenger,[1] and others that it promotes enhanced localized etch rates of silicon around nucleated copper, increasing the copper-silicon contact area.[2] Experiments which replace ascorbic acid with other well-known hydrogen scavengers such as fumaric acid[1] would help to determine if the ascorbic acid acts as a hydrogen scavenger. If these experiments show the same adhesion behavior, it may support the claim that the presence of hydrogen scavengers truly does influence the adhesion of copper films to the substrate

surface, and that ascorbic acid is acting as a potential hydrogen scavenger. Also, a more in-depth analysis of the silicon surface underlying the copper films after deposition would provide information about enhanced localized etch rates of silicon, which would give support to the second claim listed above. If the silicon etch rate is truly enchanced in localized regions of the silicon surface, then the silicon surface would show large etch pits when collecting topographical maps via AFM imaging. The copper films can easily be removed with an iron chloride solution, so this investigation would be an easy means to examine the possible role ascorbic acid plays in increasing the silicon etch rate in local regions of the surface.

7.3 Fabrication of Copper Nanowire Features

7.3.1 Conclusions Summary

Copper nanowire features were fabricated by AFM patterning of self-assembled monolayers on silicon substrates, followed by selective electroless metal deposition within these AFM-patterned lines. It was also shown that the dimensions of the copper nanowire features can be controlled and conditions optimized for the production of well-formed copper nanowires. Initially, three different SAM system which consisted of an octadecyl monolayer on silicon, and octadecyldimethylchlorosilane (ODMS) on silicon oxide, and octadecyltrichlorosilane (OTS) on silicon oxide were patterned with an AFM probe tip. All three were able to be successfully patterned, showing etch depths that surpassed the thickness of the SAM. Following electroless copper deposition, however, the octadecyl and ODMS demonstrated significant copper nucleation within resist-coated areas, whereas minimal deposition was observed in the OTS resist regions. The OTS

monolayer likely acts as a better chemical resist due to its cross-linking of the silane moieties at the SAM-silicon oxide interface as well as its superior packing and surface coverage, which can help to prevent solution penetration through the monolayer to the underlying silicon substrate.

Next, it was shown that through changes in solution conditions the copper deposition within AFM-patterned lines can be significantly impacted. Variation in the concentrations of copper sulfate, sodium tartrate, and ascorbic acid all demonstrated noteable influence on the dimensions of the fabricated copper nanowire features. This shows the great potential to manipulate the size of these copper nanowires through changes in concentration of the solution components. Furthermore, the copper sulfate source surprisingly affected the electroless deposition behavior of copper within these AFM-patterned lines. It is believed potential trace metal impurities may be the cause for these differences in behavior.

Electroless metal deposition behavior can also be influenced by substrate conditions as well as solution conditions. Changes in the width and depth of the AFM-patterned lines were investigated for their possible influence on the copper deposition in these patterned regions. Utilizing the AFM for nanopatterning, it was possible to achieve line widths down to 20 nm and successfully deposit copper within these very thin lines. Increases in line width to 125 nm also demonstrated successful plating for well-connected copper nanowire features. However, plating under standard deposition conditions within large patterned line widths of several hundreds of nanometers showed lots of small and dispersed copper seeding throughout the length of the line, and inadequate copper filling of the line to form a continuous copper nanowire. Considering electroless deposition

within these AFM-patterned lines can be controlled by changes in solution conditions, though, it is believed that uniform copper deposition within patterned lines with large widths may be achievable by altering concentrations of solution components. In regards to the depth of these AFM-patterned lines, the only requirement for successful copper deposition is to pattern deep enough to surpass the thickness of the SAM coating to expose the underlying active silicon for electroless plating.

Another substrate condition that was examined for potential impact on electroless copper deposition behavior was the doping of the underlying substrate. Monolayers were formed on both n-doped silicon as well as intrinsic silicon, were subsequently patterned with AFM, and exposed to an electroless deposition solution. Different plating behavior was expected considering electroless metal deposition occurs via a transfer of electrons between species at the surface interface. It was found that plating on intrinsic silicon (100) producing a higher density of smaller seeds within the patterned lines, whereas the copper seeds appeared to be larger in size and possessing a smaller seed density within lines patterned on n-doped silicon. This same behavior was observed within the first few seconds of electroless copper deposition on bulk silicon substrates. This difference is likely due to the difference in electron transport at the silicon-deposition solution interface leading to a difference in silicon dissolution rates surrounding nucleated metal seeds. Most importantly, though, it illustrated the promise for fabrication of uniform copper nanowires on highly resistive silicon substrates, which is important for characterization for the electrical properties of these nanowires. Overall, it was demonstrated that it is possible to impact the electroless deposition of copper within AFM-patterned lines by altering solution and substrate conditions, which shows the

potential to control the size and uniformity of fabricated copper nanowires via this method.

Lastly, copper nanowires were successfully fabricated between gold microelectrodes on an intrinsic silicon surface in order to characterize their electrical properties. It was expected that following nanowire fabrication, the large resistance of 4 MΩ for a 4 μm electrode separation would significant drop several orders of magnitude considering the resistivity of intrinsic silicon (>20,000 Ω-cm) is much larger than copper (on the order of μΩ-cm). However, following nanowire fabrication, the resistance only changed slightly, possessing a value in the range of 1 – 4 MΩ. The cause of this is believed to either be inadequate connection along the copper nanowire, or oxidation of the copper nanowire surface. More importantly, it was shown that it is possible to fabricate these nanowires between microelectrodes and obtain I-V curve measurements, and coupled with the research illustrating the capacity to influence electroless deposition by changes in solution and substrate conditions, it is possible in the future to fabricate uniform copper nanowires with controllable dimensions between these electrodes and their electrical properties can be successfully studied.

7.3.2 Future Directions

Clearly it is possible to impact the electroless copper deposition behavior within AFM-patterned lines by changing solution conditions. However, in the research described above, changing the concentrations of individual components within the electroless copper deposition solution to two concentration values collected only preliminary data. In order to gain a better understanding of how changes in solution

conditions directly affect the dimensions and uniformity of copper deposition within AFM-patterned lines, a range of concentration values needs to be investigated. Furthermore, it is still unclear why electroless metal deposition demonstrates different behavior within AFM-patterned lines when the copper sulfate source is varied. For this purpose, it would be beneficial to perform experiments that could quantify the amount of trace metals within these copper sulfate compounds. This could be done by such methods as atomic absorption spectroscopy, or anodic stripping analysis. If there were significant differences in the amount of trace metals between these copper sulfate sources, it would help support the hypothesis that trace metals play a role in the electroless deposition of copper on silicon substrates.

Additionally, the cause of the large resistance values following copper nanowire fabrication between the two gold electrodes remains unclear. The large resistance values are believed to be the result of either inadequate connection of the copper along the length of the nanowire, or oxidation of the deposited copper to form the more insulating copper oxide. In regards to the first claim, this experiment could likely be repeated to develop a copper nanowire feature with more uniformity and continuity. If this experiment was to be performed and the resistance values drop significantly, it would support the claim that the connection along the copper nanowire was the cause of such high resistance values. For the second claim, it has already been shown through resistance measurements of copper films on bulk silicon substrates that the resistance is extremely high at small film thickness values, and upon reaching thicknesses of over approximately 200 nm, the resistance seems to change less sensitive to changes in thickness. This suggests that copper oxidation may be the cause of high resistance

values. Future studies are planned, however, to further investigate this hypothesis by fabricating copper nanowires of larger dimension between the gold microelectrodes and measuring their resistance values. It would be desirable to create a graph similar to the one for the resistance measurements of the bulk copper films that shows how the resistance may change upon changes in the nanowire dimensions. If the resistance shows drastic changes at smaller nanowire sizes as compared to larger nanowire sizes, it would demonstrate the high likelihood that the copper is being oxidized at the nanowire surface and adversely affecting resistance values.

In order to overcome the drawback of potential oxidation of the copper nanowire, which can severely diminish its conductivity, other metals can be investigated for possible replacements. Copper has a standard reduction potential of $E^0_{Cu} = 0.34\ V_{SHE}$. This high reduction potential relative to the reduction potential for the oxidation of silicon that occurs at the surface during electroless metal deposition is the driving force for copper deposition. There are other metals that have been used for electroless metal deposition which display even higher standard reduction potentials, such as silver ($E^0_{Ag} = 0.779\ V_{SHE}$) and gold ($E^0_{Au} = 1.42\ V_{SHE}$).[3] The higher reduction potential of these metals would make their deposition on the silicon surface even more favorable in comparison to the copper. Current investigations involving silver on silicon substrates are underway, and preliminary results indicate the ability to selectively deposit silver within AFM-patterned lines on silicon substrates. If uniform and continuous nanowires with these metals can be developed between microelectrodes utilizing electroless metal deposition, this would be a promising means to overcome the drawback of copper oxidation, and

allow for measurable changes in resistance upon nanowire fabrication between a pair of microelectrodes.

7.4 Graphene Growth on Copper Substrates

7.4.1 Conclusions Summary

Large-area graphene possessing high optical transparency and high conductivity is essential for its application as a transparent electrode in solar cells. Chemical vapor deposition is a cheap and easy way to develop graphene of large-area dimensions, however, it suffers low conductivity values primarily due to misaligned grain boundaries and point defects. The research described here focused on fundamental investigations of graphene growth that would help to overcome these limitations and improve the optical and electrical properties of CVD graphene.

First, graphene growth was investigated on two copper substrate templates of varying structure: polycrystalline copper and cube-textured (100) oriented copper. By this analysis, it is possible to examine how changes in the substrate structure can impact graphene growth and quality. Polycrystalline copper contains mainly misaligned grain boundaries of varying crystal lattice orientation, such as Cu (100), (110), and (111). Cube-textured (100) oriented copper (CTO-Cu) is a specially treated at high temperature and pressure to generate a copper foil with highly aligned grain boundaries, as well as a crystal lattice structure that is primarily (100). Initially, graphene growth was performed on both of these bulk substrates. It was found through AFM mapping that both surfaces undergo significant copper restructuring due the CVD graphene growth process, with the CTO-Cu demonstrating a more structured and aligned orientation following restructuring

as compared to the polycrystalline-graphene surface. Furthermore, the electrical and optical properties were significantly different, with the graphene on the CTO-Cu illustrating higher optical transparency and higher conductivity. Clearly, substrate features play a role in the deposition of graphene on copper surfaces.

Secondly, graphene deposition on CTO-Cu was monitored over time to elucidate how its highly structured surface may influence the mechanism of CVD graphene deposition. Graphene was deposited on CTO-Cu for shortened periods of time, and a multitude of properties probed. During the initial stages of deposition, the relatively flat CTO-Cu surface begins to reconstruct into raised right triangles that are primarily aligned on a single axis, indicating an influence of the aligned grains of the special-treated CTO-Cu with its chiefly (100) lattice. The crystal lattice orientation within these triangular structures is Cu (111), however, showing that the surface reconstructs to promote graphene deposition in these areas due to the matching lattice constants of Cu (111) and graphene. The composition of the copper underneath the deposited graphene is believed to be primarily copper oxide, considering the large oxygen signal in EDS measurements, However, there must be a layer of reduced copper that is likely several nanometers thick in between the graphene and copper oxide, seeing as EBSD measurements show a signal that is principally Cu (111), which has a significantly different lattice constant relative to copper oxide (111). With all this information, the mechanism of graphene deposition is proposed to begin by formation of a thin melted Cu-O-H layer at the copper oxide surface, followed by formation and aggregation of reconstructed copper oxide (111) nanoparticles into aligned right triangles, as directed by the (100) substrate. Upon reduction at the surface regions of the copper oxide nanoparticles to a thin Cu^0 coating,

graphene may deposit cover the surface of the triangle structures, and over time cover the entire substrate surface.

Graphene deposition on polycrystalline copper was also monitored over time and compared to the deposition process on CTO-Cu. It was found that the polycrystalline copper does undergo a reconstruction during CVD graphene deposition. However, this reconstruction does not show any significant alignment or geometric structure as does the CTO-Cu. It was shown that graphene does deposit selectively on the surfaces of these reconstructed regions. Although, the crystal orientation of the copper on these structures still retains its polycrystalline behavior, with the notable presence of Cu (100), Cu (111), and Cu (110). From this data, it can be concluded that the special alignment and single crystal structure of the CTO-Cu aids in the alignment of graphene grain boundaries, seeing as no alignment was observed for the graphene on polycrystalline copper. Additionally, the ability of the CTO-Cu to reconstruct to a primarily Cu (111) surface shows its promise to create higher quality graphene with reduced defect density, considering the polycrystalline copper retains a variety of lattice orientations, which leads to greater defect densities as a consequence of the lattice mismatches of graphene with Cu (100) and (110). These results are promising to be able to manipulate copper foil surfaces and generate graphene with aligned grains to improve electron mobility for more successful implementation of graphene as a transparent electrode, as well as form graphene on a mostly insulating metallic oxide surface.

Finally, patterned graphene templates were investigated as a means to initiate graphene growth on insulating substrates. First, graphene nanohole templates were fabricated on insulating silicon substrates, followed by selective copper deposition within

the bare hole regions, and exposure to CVD graphene deposition conditions. It was found that when only 1 nm of copper was deposited on these samples, tall disk-like features were formed in the central regions of the holes, and there was a signal increase in graphene's characteristic Raman peaks near the perimeter of the hole regions. When 5 nm of copper was deposited, large globular features were seen in the center of these holes, and Raman spectra showed the presence of graphene's characteristic peaks filling the majority of the hole region. With this preliminary data, it is proposed during the exposure of the templated graphene array with copper to CVD graphene growth conditions, the deposited copper becomes oxidized and migrates to the energetically-favorable edge sites of the hole array. There, the surface of the copper may potentially be reduced and promote graphene assembly from the edge site, and the copper species at the edge site may move inward as the graphene edge closes the hole area. The initial findings still show potential for graphene deposition from graphene template edges on insulating substrates, and with further inquiry would provide a means to overcome the limitation of CVD graphene deposition on bulk metallic substrates, and the difficulties included in transfer to dielectric materials. Overall, through a detailed understanding of the graphene growth mechanism, it may be possible to manipulate the growth by controlling the substrate structure, processing conditions, or even templating the growth of graphene on insulating substrates.

7.4.2 Future Directions

It has been shown that changes in the copper substrate structure can significantly impact the deposition and quality of CVD graphene. From the data presented above, a proposed mechanism was postulated describing the stepwise process by which graphene

may form on the CTO-Cu and polycrystalline copper. However, there are still a few aspects that remain unclear in this deposition process. For instance, it is evident from the EDS data that there is oxygen present underneath the deposited graphene as well as the areas with no deposited graphene, indicative of the presence of copper oxide across the entire substrate surface. However, the EBSD measurements reveal that the surface of the copper where graphene has deposited is Cu (111), which has a significantly different lattice constant that Cu_2O (111). Evidently, there must be a layer of reduced copper in between the graphene and the copper oxide, but the exact thickness of this layer remains unclear. For the purpose of creating graphene on mostly insulating substrates, it is imperative to determine the thickness of this reduced copper layer to understand the potential affects the copper may have on the graphene's electrical properties atop these substrates. Future studies are therefore planned to be able to determine the thickness of the reduced copper layer, as well as the underlying copper oxide layer, utilizing depth profiling techniques such as X-ray photoelectron spectroscopy (XPS) or Auger electron spectroscopy (AES). This would provide a greater knowledge of the composition and insulating capacity of these copper substrates with deposited CVD graphene.

Additional future studies include the thorough examination of the graphene deposition within the graphene nanohole templates. Preliminary data have shown the possibility of graphene nanohole templates to induce the further growth of graphene, however this process is still largely unclear. It was hypothesized that during the growth process, the deposited copper nanoparticles can migrate to the nanohole edges, and induce graphene growth from the edge toward the central region. In order to clarify this process, it would be valuable to monitor this process over time and with a larger range of

deposited copper thicknesses to see if these raised features can be observed moving from the outer hole edges toward the hole center. Furthermore, the resolution for Raman mapping is near the size of the nanoholes within these graphene hole templates. This makes it difficult to get a clear mapping of any potential graphene growth within the nanoholes. To overcome this, experiments with larger nanoholes would provide better mapping of graphene growth, and a clearer idea of how the graphene may grow from the edge of the nanoholes.

In the end, it would be the hope to merge the work on selective copper nanowire fabrication on silicon substrates and the research focused on controllable growth of CVD graphene. Clearly, copper can be used as a template to selectively deposit CVD graphene. Through the high controllability of size, orientation, and configuration provided by AFM nanopatterning and electroless copper deposition, it is possible to create highly complex designs of copper on silicon substrates. These intricate designs may then be used as templates to selectively deposit CVD graphene, and allow for the construction of complex designs of graphene.

7.5 Doped Graphene Nanohole Arrays

7.5.1 Conclusions Summary

An additional method explored in this work to improve the optical transparency and electrical conductivity of CVD graphene films was through nanopatterning and chemical doping. Graphene nanohole arrays (GNAs) were fabricated by nanoimprint lithography and doped with thionyl chloride to potentially increase conductivity while simultaneously decreasing the optical transmittance, which would beneficial for the

application of graphene as a transparent electrode. It was found that patterning graphene films with nanoholes decreased the optical transmittance of single layer graphene across the visible region of the light spectrum. Furthermore, nanopatterning provided a greater amount of active sites for chemical doping due to the exposed nanohole edges, and led to a conductance enhancement of 15-18 times greater than its undoped counterpart, whereas unpatterned single-layer graphene illustrated only a 2-4 enhancement factor following dopant exposure. Clearly through this method, conductivity of graphene films can be significantly enhanced while also enhancing optical transparency.

7.5.1 Future Directions

Chemical doping is an effective means to increase the conductivity of graphene films, as seen from the research presented in this dissertation. Only one dopant was investigated in this work, however there is a potential to explore other dopants that can also increase conductivity, such as metal nanoparticles or NO_2. Furthermore, only one nanohole size and spacing was examined in these experiments. It may be possible to tune the amount of chemical doping, and therefore the electrical properties of graphene, through changes in the nanohole dimensions and density. By alterations in the size and density, it would be feasible to control the amount of active doping sites within the graphene arrays, and therefore the doping and consequently the electrical conductivity.

7.6 Final Statement

The research presented in this dissertation demonstrates how nanopatterning and templating can be utilized to form highly ordered nanostructured material on substrate surfaces. Both of these methods provide a promising means to control the size,

orientation, and design of materials on the nanoscale. Nanopatterning was coupled with electroless metal deposition to fabricate copper nanowire features on silicon substrates. Templating was incorporated for the development of high quality CVD graphene on copper substrate templates, as well as directed growth from nanopatterned hole array templates and chemical doping. Through the improvement of nanostructured material properties and their fabrication methods as described here, it is possible to enhance their function in several application areas that possess a large demand for nanostructured materials, such as sensing, environmental sustainability and clean up, energy harvesting and storage, as well as nanoelectronics.

7.7 References

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