Analysis of Artifacts Inherent to Real-Time Radar Target Emulation

By

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Abstract

Executing high-fidelity tests of radar hardware requires real-time fixed-latency target emulation. Because fundamental radar measurements occur in the time domain, real-time fixed latency target emulation is essential to producing an accurate representation of a radar environment. Radar test equipment is further constrained by the application-specific minimum delay to a target of interest, a parameter that limits the maximum latency through the target emulator algorithm. These time constraints on radar target emulation result in imperfect DSP algorithms that generate spectral artifacts. Knowledge of the behavior and predictability of these spectral artifacts is the key to identifying whether a particular suite of hardware is sufficient to execute tests for a particular radar design. This work presents an analysis of the design considerations required for development of a digital radar target emulator. Further considerations include how the spectral artifacts inherent to the algorithms change with respect to the radar environment and an analysis of how effectively various DSP algorithms can be used to produce an accurate representation of simple target scenarios. This work presents a model representative of natural target motion, a model that is representative of the side effects of digital target emulation, and finally a true HDL simulation of a target.

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Nomenclature

A Attenuation

ADC Analog to Digital Converter

$ASIC$ Application Specific Integrated Circuit

AWG Arbitrary Waveform Generator

$AWGN$ Additive White Gaussian Noise

A_{rx} Receiver Attenuation

B Bandwidth

$BPSK$ Binary Phase-Shift Keyed

$BRAM$ Block RAM

B_{IF} Bandwidth, Intermediate Frequency

CIO Common Input and Output (memory)

CPI, T_{CPI} Coherent Processing Interval

M Number of Pulses

$R, R(t)$ Range to target

R_0 Starting range to target

R_{max} Maximum range to target

$SNR_{a,b,c}$ a = location, b = in/out, (c = min/max if applicable)

ΔR Radar range resolution

δR Minimum range step size of target generator

τB Time-Bandwidth product

τ Duration of transmitted radar pulse

$a(t)$ Pulse Envelope

c Speed of Light, $3x10^{8}$

k Boltzmann's Constant, $1.38x10^{-23}$

m Slow time sample index

t_{clk} Sample interval of target generator

t_d Delay resolution of target generator

v Velocity

v_p Velocity of propagation

v_r Radial velocity

G_{proc} Processing Gain

G_{rx} Receiver Gain

G Gain

$N_{\Delta a}$ Number of memory pointer spacing changes during the CPI

$P_{FS,x}$ Power in the Full Scale Range of x = ADC or DAC

$P_{LSB,x}$ Power in the Least Significant Bit of x = ADC or DAC

P_n Noise Power

$P_{r,ADCin}$ Received Power at the input to the ADC , MDS

$P_{r,a,b,c}$ Received Power: a = location, b = in/out, (c = min/max if applicable)

P_r Received Power

P_t Transmitted Power

$T_{e,rx}$ Receiver equivalent Noise Temperature

T_e Equivalent Noise Temperature

$T_{in,290}$ Input Noise Temperature for Free Space Receiver

T Delay to Target

W_{FC} DDS Frequency Control Word

λ_{RF} Radar transmitted wavelength

$\phi(t)$ Waveform phase modulation

σ_R Standard deviation in range measurement

σ_f Standard deviation in Doppler frequency measurement

σ Radar Cross Section

$h(t)$ Transfer Function

n_x Number of clock cycles required for a read (x = rd) or write (x = wr) operation

n Fast time sample index

$s(t)$ Radar transmitted waveform

$s_m(t)$ Mth transmitted radar pulse

t_o Delay to Target

$t_{p,i}$,$t_{p,i}(t)$ Incremental Propagation Delay

t_p Propagation Delay

$w(t)$ Additive White Gaussian Noise (AWGN)

$y(t)$ Radar received signal

$y_m(t)$ Radar received signal due to mth pulse

$D_{G,FIR}$ Group delay of a FIR Filter

D_{MEM} Delay due to memory

D_{SSB} Delay due to SSB Modulator

DAC Digital to Analog Converter

DDR Double Data Rate (memory)

DDS Direct Digital Synthesizer

DPRAM Dual Port RAM

δt_{pi} Smallest Delay Incrment in Coaxial or Optical Delay Line

$\sqrt{\varepsilon_r}$ Refractive Index

f_{clk} Clock frequency of FPGA in target generator

$f_{\Delta a}$ Update rate frequency

Δ_{addr} Memory address pointer spacing

Δf_d Radar Doppler frequency resolution

f_d Doppler frequency

Δf_{DDS} DDS output frequency resolution

f_{DDS} DDS output frequency

f_{IF} Center frequency of the radar transmitted bandwidth IF band

f_{PRF} Pulse Repetition Frequency

f_{PRI} Pulse Repetition Interval

f_{res} DDS Frequency Resolution

f_{RF} Center frequency of the radar transmitted bandwidth in the RF band

F_{rx} Radar receiver noise figure

f_s Sampling frequency of the radar

$f_{s,ADC}$ Sampling rate of the Analog to Digital Converter

$f_{s,DAC}$ Sampling rate of the Digital to Analog Converter

f_{set} Frequency Setting for DDS

f_{sw} Switching frequency of variable delay line

FCW DDS frequency control word

FFT Fast Fourier Transform

FIR Finite Impulse Response

FPGA Field Programmable Gate Array

HDLM Hardware Description Language Model

I In-phase

IF Intermediate Frequency

IIR Infinite Impulse Response

IM Interpolated Model

l Delay Line Length

LFM Linear Frequency Modulated

LO Local Oscillator

LUT Look Up Table

N Number of Bits

NM Natural Model

PRF, f_{PRF} Pulse Repetition Frequency

PRI, T_{PRI} Pulse Repetition Interval

PSL Peak Side Lobe

Q Quadrature-phase

QDR Quad Data Rate (memory)

QM Quantized Model

RAM Random Access Memory

RCS Radar Cross Section

RF Radio Frequency

S Number of FIR Filter Coefficients

SIO Separate Input and Output (memory)

SNR Signal to Noise Ratio

SRAM Static RAM

SSB Single Sideband

Chapter 1

Introduction

Radar is a technology that has been adapted to meet remote sensing and detection needs in a growing number of fields. Following its inception for military purposes, the applications for radar have expanded to include weather monitoring, geographical imaging, topography, medical imaging, subsurface analysis, and automotive anti-collision to name a few. While each application has a unique set of goals that the radar design is tailored to achieve, in all cases the radar data products are used to inform a decision regarding the radar's field of view. This decision could range from simple detection to object classification to as complicated a goal as directing autopilot maneuvers for collision avoidance. As society becomes more reliant on radar technology for increasingly critical data, the need to develop flexible calibrated testing solutions for radar systems must not be overlooked.

There are two significant approaches to radar hardware performance evaluation beyond simulation. Benchtop testing provides an easily controlled environment with a limited set of test options. Field testing, in contrast, allows the system under test to interact with a broad range of real-world variables, which can be beneficial until an unexpected result occurs without known (repeatable) stimulus. While observing an undesirable result is always useful to the altruistic goal of designing a perfect product, if field testing is introduced before rigorous benchtop testing, otherwise easily identified design flaws may compound and make the troubleshooting process tedious and ineffi-

cient.

It should be no stretch of the imagination to see the value in developing benchtop test methods that are highly representative of real world scenarios. A piece of test equipment capable of generating a synthetic target that is representative of the mission environment can give a radar designer data points that thoroughly characterize the radar's performance in response to a variety of stimulus. Synthetic target generators can be configured to test the limits of a design by presenting unexpected or undesired targets as well to verify that false detections do not occur.

What constitutes a real world scenario and what unit under test (UUT) performance parameters need to be vetted may vary depending on the use case for the radar system. An undeniably basic quality of a radar system is to identify the range to a target. More complicated tasks like discrimination between targets at the same range based on angle of arrival, Doppler processing, Moving Target Indication, target tracking, Synthetic Aperture Radar image formation, and automatic target recognition require a more capable radar design. Increased mission complexity requires more robust environment simulation during testing to fully exercise the radar's processing.

When designing, specifying, or configuring a target generator to interface with a specific radar, it is paramount to consider how various design architectures will affect the quality of the synthetic target. Compared to a real target, digitally generated synthetic targets may yield a modified signature based on factors that will become clear as the target generator architecture is developed in later sections. Whether these inconsistencies are significant enough to render the emulation of the desired target paradigm insufficient is dependent on several characteristics of the radar itself; its transmitted waveform, its receive processing, and the extent to which the emulated scenario in question strains the operating limits of either system.

1.1 Motivation

The goal of this thesis is to provide intuition regarding digital target generator performance so that a radar test engineer, knowing the parameters of their radar and the candidate target generator

architecture, could establish whether the piece of equipment in question is capable of generating suitable test targets.

It is clear that all radar systems cannot be fully vetted with the same environment simulation algorithm due to the fact that the processing that accompanies each radar is as varied as the applications mentioned previously. It is likely, however, that one piece of equipment could be used to simulate a basic environment for any radar that meets a set of criteria (transmission bandwidth, range to target, etc.). Even if only a fundamental suite of tests is considered, there are many characteristics of both the radar and the simulator that may affect the target quality including the transmitted waveform, the receive processing algorithm, and how the characteristics of the simulated targets compare to the performance limits of the radar and the simulator.

This document will invert the traditional consideration of a classic radar signal processing problem. Rather than focusing on how the radar processing can be changed to extract more information from a scene, this document will explore the fidelity with which an environment simulator emulates targets. The quality of the target simulator will be evaluated by comparing the data products generated by a common coherent pulse-Doppler processing architecture in response to a point target as represented by various target simulation algorithms.

In summary, this thesis documents the design of a target simulator, its evaluation with various radar architectures and target attributes, recommendations for improvement on basic architectures, and conclusions regarding its suitability for simulating radar environments in a testing application.

1.2 Organization of Thesis

The results of this research are presented as follows. Chapter 2 presents the radar signal model with space devoted to various target types, radar waveforms and radar processing methods. This background information is followed by Chapter 3, which provides an overview of historical radar test methods in addition to a high level overview of the digital target generator architectures considered in this work. Next, Chapter 4 provides a breakdown of the sources of error inherent in

the components that comprise the test architecture and their theoretical impact to signal integrity. This analysis is followed by Chapter 5 which delves into design details associated with specific implementations of a representative digital target generator architecture and then presents the characterization of these architectures in the context of the data provided in Chapters 3 and 4. Finally, simulation results comparing the target signature produced by the various architectures while the parameters of the simulated target and radar are varied are presented in Chapter 6 and compared with data collected from hardware-based target emulation. Conclusions and a summary of the results will be provided in Chapter 7.

Chapter 2

Radar Signal Model

Before considering the effects of various methods of radar environment emulation, a framework must be established within which the target generator architecture can be analyzed. This framework takes the form of a radar signal model that characterizes the scatterers in a scene and constrains the radar's measurements of these characteristics. These formulations are defined after the development of a representative modern Doppler radar architecture. The end of this chapter relies on an example to demonstrate fundamental radar processing methods, illustrate the expected signals, and describe the ideal target response.

2.1 Environment Model

A radar fundamentally operates by emitting energy in the form of radio frequency (RF) electromagnetic waves and processing the energy that has been re-radiated by objects in the environment and scattered towards the radar's receiver. The simplest example of a radar target is a solitary point in space such as the small reflective surface or facet [40] depicted in Figure 2.1.a. The lower part of panel a. shows a simplified representation of the received reflected signal, which is incident on the receiver t_o seconds after transmission and is notably non-zero for the same time duration as the transmitted waveform.

The diagram in Figure 2.1.b demonstrates the slightly more complicated case of a single radar

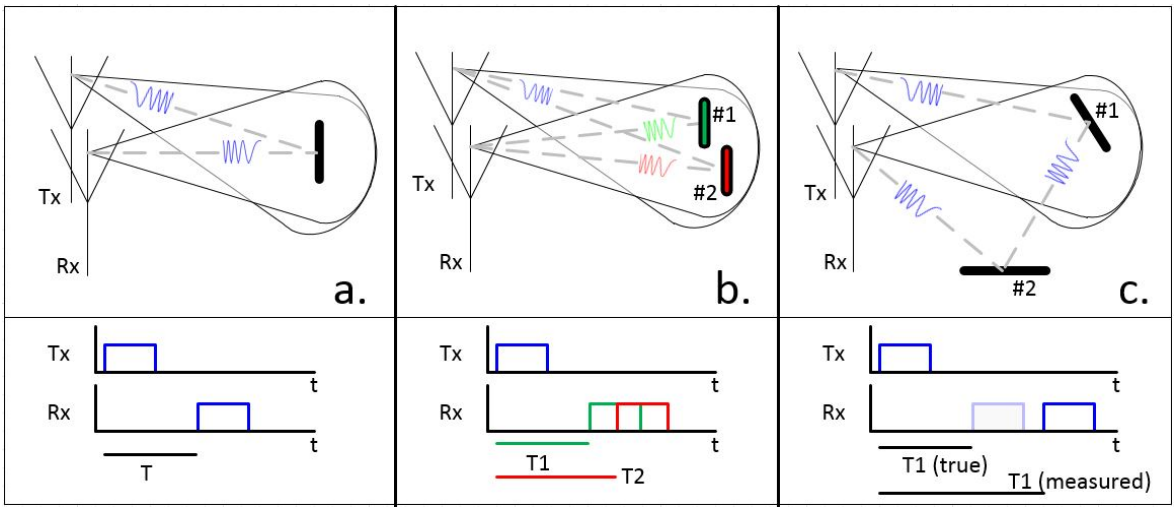

Figure 2.1: a) A single "point" scatterer in the main beam of the transmit and receive antennas. b) Two scatterers used to illustrate how superposition applies to radar. c) Two facets arranged in such a way that the received signal has scattered off of both.

pulse interacting with multiple targets and the key point that the principle of superposition applies to radar returns [30]. The composite effect of illuminating the scene is apparent after the backscatter from each independent scatterer is summed coherently in the receiver. The incident energy will add constructively or destructively based on the phase of the incoming signals. Because superposition applies, after the phenomena associated with Figure 2.1.a are understood, they can be applied independently to every scatterer that the radar will illuminate to form a backscattering model.

Finally, Figure 2.1.c illustrates a case when an echo finds its way back to the radar's receiver by a path other than the direct return path. In this case, even though facet 1 is in the antenna mainlobe, it is angled in such a way that it would not yield any backscatter if not for facet 2. The backscatter that follows the indirect return path shown in panel Figure 2.1.c would be delayed by a greater amount than the delay associated with the expected direct return path from facet 1. This phenomena may cause the radar to incorrectly report the location of the object to be at a greater range than it truly is [30]. This configuration could result in an undesirable multipath scattering condition if a direct return path from facet 1 also existed. A similar model can also be used to depict volumetric scattering from various terrain types such as foliage [40].

Objects are not guaranteed to reflect significant power to the receiver. This is due in part to

the fact that electromagnetic scattering is governed by Snell's law, which states that for a specular reflection from a smooth target, the angle of reflection is equal to the angle of incidence [19]. If the second reflector wasn't present in Figure 2.1.c., for example, no backscatter would have been incident on the receiver.

Scattering phenomena are further complicated by the fact that the illuminated surface may be electromagnetically rough, as discussed by [19] and [40]. Rough surfaces yield incoherent, diffuse scattering characterized by an unpredictable range of reflection angles. In contrast, the backscatter from a smooth surface is coherent, specular, and predictable. The scattering characteristics of most objects cover a range on the spectrum between smooth and rough that is based on their dimensions relative to the illuminating wavelength and the scene geometry [19]. In practice, objects are assigned a backscattering coefficient or radar cross section (RCS), σ that is often derived from a statistical model [40].

The comprehensive statistical modeling of scattering behavior includes characterizing regions of scatterers and volume scatter, modeling the effects of environmental factors on backscatter, and the consideration of how a non-rigid scatterer's reflectivity can fluctuate with respect to time. A region's homogeneity or lack thereof further directs the selection of a distribution. A brief yet comprehensive summary of common models and when to apply them can be found in [30] or [36].

Another time-varying aspect of target description is motion, categorized as translation or internal motion. Translation occurs when an object changes physical location relative to the radar, thereby causing the distance between the object and the radar to change. As a result of this motion, the relative phase of the received signal will change according to the varying range [30]. If the radar waveform is pulsed, a coherent receiver will measure a different phase offset between a reference waveform and each pulse in the series. In the case of constant velocity motion, a constant phase progression will occur and yield a constant Doppler shift in the processed data [30].

Internal motion, alluded to in the discussion of RCS, is a fluctuation in reflectivity created by changes in the target's orientation or location relative to other scatterers in the scene. In the case of a rigid target like a cube, rotation of aspect angle would cause the incident illumination to reflect

off of a square face of a cube at one moment versus an edge or corner the next. In the case of a non-rigid target like a tree, the randomly changing distance and relative location of the leaves will cause the backscatter to change over time [30]. This random motion causes a fluctuation in the relative phase of the scattered signal that can be characterized by a random process and will yield spreading of the reflection's Doppler spectrum. This spectral spreading can occur in addition to the deterministic 0 Hz Doppler shift of a perfectly stationary rigid reflector, or the higher frequency Doppler shift of constant velocity motion[30].

The discussion of target modeling would be incomplete without determination of whether an object in a scene is considered to be a target or clutter. The scattering of any object can be modeled using the methods described previously, but some aspects of an environment receive a designation of clutter if they are considered unwanted scatterers in a scene. This designation is arbitrary and mission dependent. A radar attempting to locate a moving vehicle, for example, would consider the ground around the vehicle to be an unwanted source of interference that is in conflict with the target of interest. To provide useful data about the vehicle, the radar's processor must have an accurate perception of the clutter characteristics and be prepared to remove their effects. An imaging radar, on the other hand, would consider the same region of Earth to be a distributed target of interest [38].

Finally, discussion of the radar range equation will connect these considerations to the following section's focus on basic radar architecture. Attributes of the target such as range and and RCS directly impact the received power and defined by the radar range equation in Equation 2.1 [19]. This formulation of the radar range equation is limited to describing the received power after the interaction between a radar and and a point target.

$$P_r = \frac{P_t G^2 \lambda^2 \sigma}{(4\pi)^3 R^4} \tag{2.1}$$

Equation 2.1 defines the relationship between key radar design parameters and the qualities of its environment including: the transmitted power before the antenna P_t, antenna gain G, radar wavelength λ, target RCS σ and range to the target R. The equation yields the amount of received

power that will be seen at the receiver, P_r. It is worth noting that the only variables in this equation that depend on the environment are the range and RCS of the target. Furthermore, the range term is arguably the most significant factor in this equation, as the received signal power is inversely proportional to the range raised to the fourth power. The dominance of the range term is especially significant in the context of modeling realistic target motion. For example, if the distance between the radar and an object is decreased by a factor of two, the power of the backscatter incident on the receiver will increase by a factor of 16. An accurate model of a target will include consideration of this amplitude factor and its rate of change.

While the radar range equation is a useful tool, due to the incredible complexity and variability of the world it is often infeasible to use received power alone to provide details of a scene. Instead, the radar range equation serves as a system design and analysis tool that is primarily used to verify to a rough order of magnitude that the received power level will be sufficiently high for processing to occur. The relationship between the received power and the receiver's thermal noise floor, referred to as Signal to Noise Ratio (SNR), will be shown in the following section and has major implications for receiver design.

2.2 Radar Model

This section will discuss the functions of the radar transmitter and receiver in detail, making frequent references to the architecture depicted in Figure 2.2.

While the research in the following chapters could be applied to variations of the system in Figure 2.2, the detailed development of an approach suitable for these cases is left as future work.

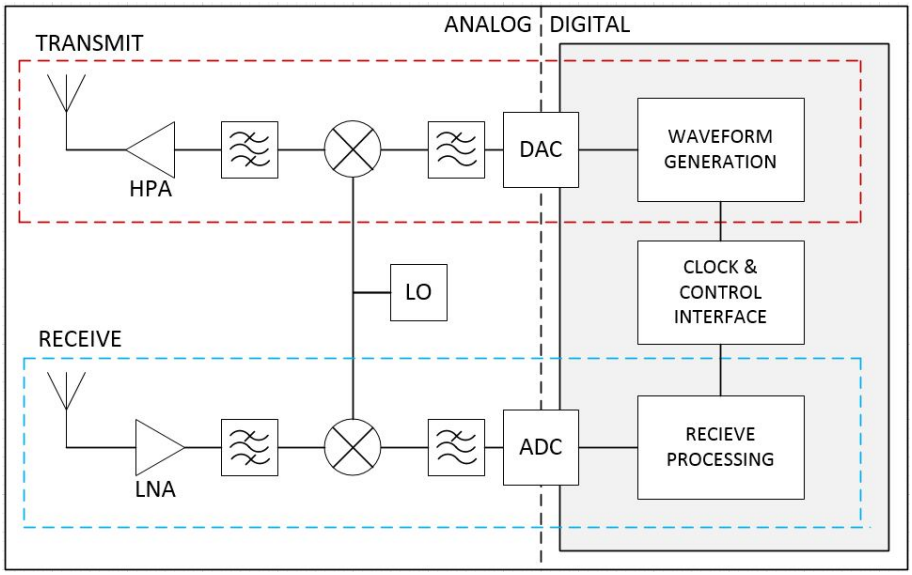

Figure 2.2: Representative radar block diagram.

2.2.1 Transmitter

The radar's transmitter subsystem as indicated in Figure 2.2 serves the purpose of generating and conditioning the waveform that will illuminate the environment. Before delving into architectural specifics, the radar's transmission scheme, including waveform duty cycle, repetition rate, and modulation type must be addressed.

Radar processing can be performed on continuous or pulsed waveforms [18]. A continuous waveform is described as having a duty cycle of 100%, while any lower duty cycle characterizes a pulsed waveform. If the transmitted power remains constant, higher duty cycle transmission schemes benefit from higher received SNR because they illuminate the target with more energy [31].

While shortening the pulse duration, τ, degrades the SNR, it yields a desirable refinement in range resolution. This trade off is due to the inverse relationship between range resolution and bandwidth of the transmitted signal, B, that will be covered in Section 2.2.4 [30]. The lost SNR could be recovered by increasing the transmitted power. Depending on how much additional power is required, this ay be difficult to achieve due to a variety of reasons from limited availability of high power RF amplifiers that meet the weight and size constraints, to overheating and dispersion

concerns, to FCC regulations on RF emissions [38].

The trade-off between high SNR and fine range resolution, two qualities necessary to the goal of making accurate measurements of a scene, is resolved in modern radar systems by a technique called pulse compression. In pulse compression, the frequency or phase of a transmitted sinusoid is modulated; dramatically increasing its bandwidth. Some examples of pulse compressed waveforms are shown in Figure 2.3. Pulse compression radars can achieve sufficient SNR even with low transmit power via processing gain realized in the receiver; the subject of Section 2.2.2 [38].

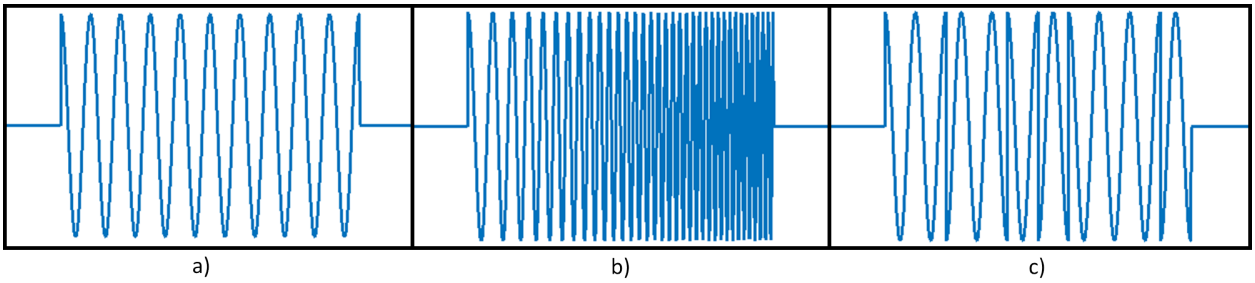

Figure 2.3: Examples of Radar Waveform Modulation: a) Unmodulated Pulse, b) Linear Frequency Modulation (LFM), c) Binary Phase-Shift Keying (BPSK)

Regardless of the specific transmission scheme chosen, the duty cycle is referenced to a regular time interval at which the waveform is retransmitted. This time interval is referred to as the pulse repetition interval (PRI), T_{PRI}, which is the inverse of a frequency domain radar metric, the pulse repetition frequency (PRF), f_{PRF}.

The PRI and PRF define the radar's unambiguous measurement limits on the range and velocity of targets respectively [38]. Fundamental radar processing is designed under the assumption that any echo that appears during the T_{PRI} following a transmission is associated with the pulse at the beginning of said PRI [38]. Therefore, any target with a round trip travel time that is longer than T_{PRI} will be associated with the following interval and be incorrectly calculated to be closer to the radar than it is. This miscalculation is referred to as an ambiguity because while the target is located at an integer multiple of the reported delay, the radar processing cannot isolate which PRI the echo belongs in without further information [30]. A similar relationship exists between the PRF and Doppler frequency. The echo from any moving target that exhibits a Doppler shift greater

than $2f_{PRF}$ will be aliased down to below the PRF. Again, the target's true Doppler frequency is an integer multiple of the reported frequency, but an ambiguity exists in the radar processing [30].

Architecturally, the transmitter in Figure 2.2 is simple; the digital waveform generation section is connected to the analog signal conditioning section by a Digital to Analog Converter (DAC). Waveform generation is typically performed using a direct digital synthesizer (DDS) [2]. While a memory-intensive arbitrary waveform generator-based (AWG) design is limited to repeating a set of stored waveforms, a DDS-based modulation method can generate phase continuous waveforms that can be changed at will with a fraction of the memory cost [9]. In modern radars, the control interface block in Figure 2.2 provides baseband data that is modulated onto the carrier by combining scaled versions of the balanced quadrature outputs provided by the DDS. The output of the waveform generation block is a real or complex waveform within the analog bandwidth of the radar's DAC. The DAC output is a real signal centered at an intermediate frequency (IF).

The first analog component in the transmitter is an anti-alias reconstruction filter to remove the contributions of the upper Nyquist zones from the output spectrum of the DAC [26]. The analog IF waveform is then upconverted to the RF center frequency via a mixer and bandpass filtered to remove undesirable mixing products. Next, the waveform is amplified to the power level P_t deemed necessary for the application by the radar range equation in Equation 2.1. At the end of the transmit chain is an antenna that spatially filters the output power by focusing it into an azimuth and elevation beamwidth in addition to applying additional gain. Finally, free space propagation occurs, and the backscatter from any object in the radar's field of view is incident on the receiver [38].

2.2.2 Receiver

The receiver completes the remote sensing process by collecting, conditioning, and processing the backscatter from the scene. The radar receive processing is the most likely to be unique to the radar's application because its capabilities define the radar's ability to make determinations about scatterers the scene [31] [38].

The fundamental architectural elements of a receiver are illustrated in Figure 2.2. The incoming signal is received by the antenna, then bandpass filtered. Filtering reduces the potentially wideband antenna response to match the transmitted bandwidth and limits the noise power. The band-limited signal is then downconverted with a copy of the local oscillator (LO) signal used in the transmitter to an IF that resides within the analog sampling bandwidth of the analog to digital converter (ADC) [25]. After the signal is sampled by the ADC, application-specific digital signal processing algorithms are executed. These algorithms could be used to make real time decisions using the data or to precondition the received data for further processing by an external computing system.

A key metric of radar system design that is inherently associated with the receiver is the SNR; a measure that describes the ratio of the power level of the received signal of interest to the power level of the receiver's noise floor over some bandwidth [20] [29]. SNR is comprehensively defined relative to the system by relating it to the radar range equation for received power, P_r in Equation 2.1. Equation 2.2 [30] introduces six new terms to facilitate the calculation of the SNR at the output of the analog receiver, $SNR_{rx,out}$. These terms are the noise power at the input to the receiver, P_n, Boltzmann's constant $k = 1.38x10^{-23}$, the noise temperature at the input to the receiver associated with free space $T_{in} = 290K$, the receiver's IF bandwidth B_{IF}, the receiver's noise figure F_{rx}, and the receiver's gain G_{rx}. Note that Equation 2.2 can be referred to at the analog receiver output SNR or the SNR at the input to the radar's ADC.

$$SNR_{rx,out} = SNR_{ADC,in} = \frac{P_r}{P_n} = \frac{P_r G_{rx}}{P_n G_{rx}} = \frac{P_r}{kT_{in}BF} = \frac{P_t G^2 \lambda^2 \sigma}{(4\pi)^3 R^4 k T_{in} BF} \tag{2.2}$$

A constraint on the receiver's thermal noise floor is established by the quantization noise associated with the ADC that is used to digitize the data at the output of the analog receive chain. The radar must be designed such that the thermal noise will be on the order of 3 dB above the quantization noise level of the of the ADC, as will be discussed in Section 4.1.2 [20]. Therefore a lower limit on P_n in Equation 2.2 is established.

As a rule of thumb, after all radar processing operations have been completed, the final power

in the signal of interest must be at least 3 dB above the thermal noise floor to be detected [20] [30]. This implies that careful design will set the final signal level at 6 dB above the power in the quantization noise of the ADC.

An important power level to keep track of in receiver design is the Minimum Discernible Signal (MDS) at the input to the ADC or $P_{r,ADC,min}$. This is a measure of the lowest magnitude the signal of interest can have for accurate detection. If no post-processing will occur after sampling, the MDS must be set to at least 3 dB above the receiver's thermal noise floor as described above. If post-processing will occur, however, the MDS could be lower than the thermal noise floor by a factor of the amount of gain to be realized in post-processing. The minimum signal levels at various points in the receiver are illustrated in Figures 2.4 and 2.5. In Figure 2.4, the noise floor is represented as unchanging throughout the receiver and especially during post-processing. This is not necessarily accurate, but facilitates the illustration of signal levels at various points relative to the noise.

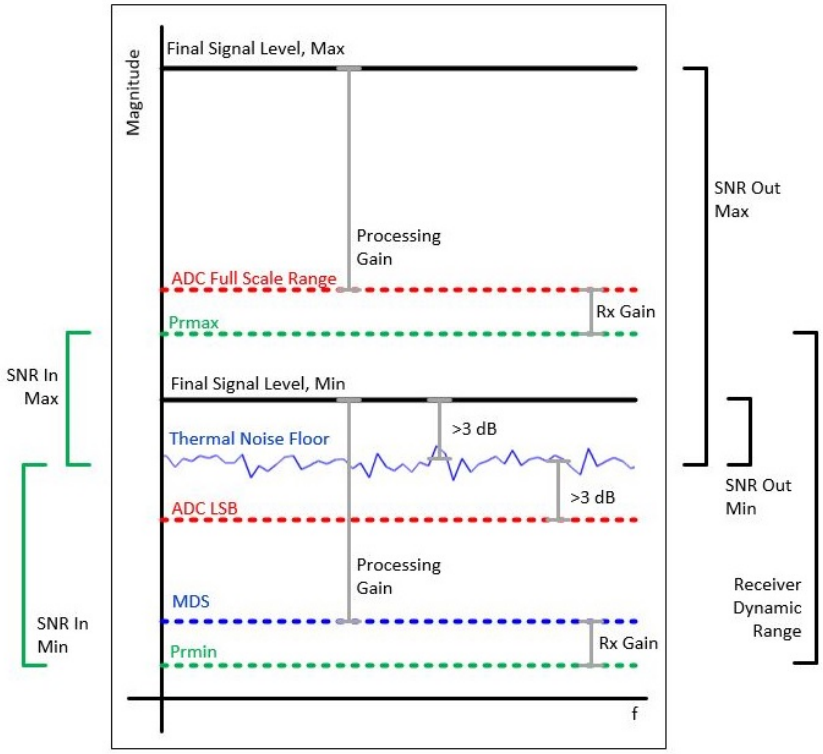

Figure 2.4: Relative Signal Levels in the Receiver

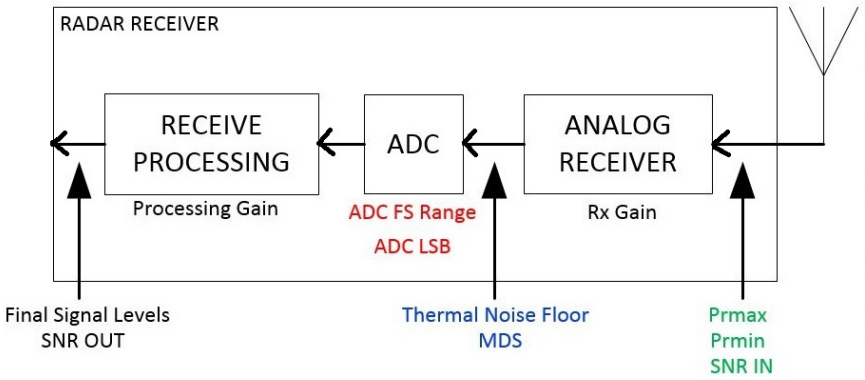

Figure 2.5: Radar Receiver Block Diagram

The purpose of computing these minimum signal levels is that when $P_{r,ADCin,min}$ and $SNR_{rx,out,min}$ are known, Equation 2.2 can be manipulated to solve for the maximum range at which a target can be sensed, R_{max}, as is shown in Equation 2.3.

$$R_{max} = \sqrt[4]{\frac{P_t G^2 \lambda^2 \sigma}{(4\pi)^3 (SNR_{ADCin,min})}} \tag{2.3}$$

In this inversion of the radar range equation, $SNR_{ADCin,min}$ would be set to 3 dB greater than the processing gain realized after sampling to represent the MDS that is associated with the maximum range. This computation is significant, because R_{max} must be greater than or equal to the maximum range target of interest for the radar design to be suitable for its mission. If the maximum range is insufficient for the mission, then aspects of the radar design such as transmitted power P_t, transmitted bandwidth B, or pulse duration τ must be increased to boost the minimum SNR at the receiver for reasons made clear in Section 2.2.3.

2.2.3 Basic Receiver Processing

Two common receive processing algorithms that will be applied in this work are matched filtering and Doppler processing [30]. These two processing methods occur in orthogonal time domains, referred to as the fast-time and slow-time domains. The first step of the receive processing is to format the received signal into what is referred to as the data cube [30], shown in Figure 2.6.

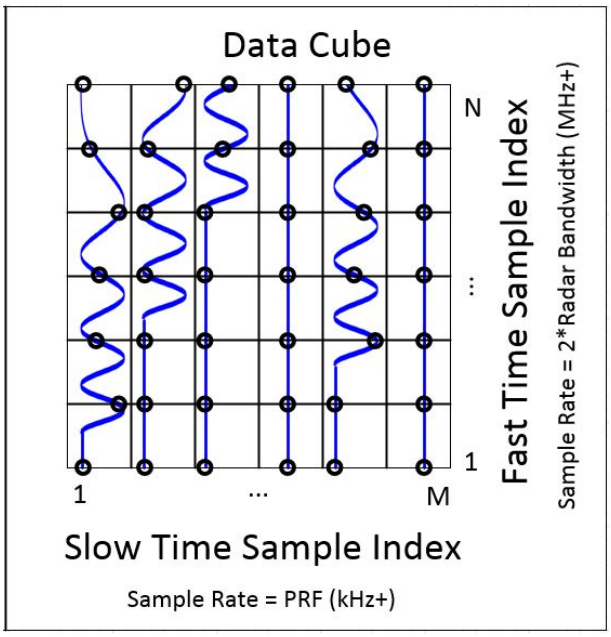

Figure 2.6: Data cube with analog data superimposed on the digital samples. Each column contains the number of samples collected during a PRI spaced at the fast time sampling rate. [31]

The fast-time axis in Figure 2.6 provides range measurements. This axis is sampled at the sampling rate of the receiver, which must be at least twice the waveform bandwidth according to the Nyqist sampling theorem [20] [31]. The number of samples along the fast-time axis is bounded by the number of fast-time sample intervals in the PRI. The slow-time axis, in contrast, is defined in terms of pulse number and therefore is sampled at the PRF. Processing the slow time axis allows the radar access to Doppler frequency information about the scene. The number of samples along the slow-time axis is equal to the number of pulses in the coherent processing interval (CPI) [31].

Matched filtering is a process in which the time reversed complex conjugate of the transmitted waveform is stored in memory and convolved with the received data and is the foundation of how individual scatterers can be identified in an incoming data stream [31]. Specifically, because the backscatter from the environment due to the radar's illuminating energy is composed of time delayed versions of the transmitted waveform, performing a cross-correlation between the received data and a stored copy of the waveform will result in a data stream with high amplitude regions associated with the scatterer's round trip delay from the radar [30]. Matched filtering is the operation that makes pulse compression effective at refining range resolution. The processing gain realized

by matched filtering is equal to $10\log_{10}(\tau B)$ dB, where τB is referred to as the time-bandwidth product [30]. The expected attributes of the matched filtered output varies depending on the modulation of the transmitted waveform and are discussed in depth in [18] and [30]. The match filtered output can be normalized by dividing the output by the scalar result of the inner product of the transmitted waveform and itself. Normalization causes the power level of the correlated signal of interest to be unchanged by the filter while the power in the non-correlated noise are suppressed by an amount equal to the match filtering gain $10\log_{10}(\tau B)$.

Doppler processing is performed by computing the Fourier Transform in the slow-time dimension along each fast-time row [31]. As was described in Section 2.1, if the relative motion between the target and radar platform is uniform, the backscatter from a single target due to successive pulses (slow time samples) will exhibit a phase progression in time. The Fourier Transform of this phase progression will result in an impulse or $\frac{sin(x)}{x}$ response centered at the Doppler frequency associated with the relative radial velocity causing the periodic phase shift. As is implied above, Doppler processing requires the analysis of multiple related pulses. The time duration over which these multiple pulses are collected is the Coherent Processing Interval (CPI), or T_{CPI}, and is simply computed as M*T_{PRI}, where M is the number of pulses as shown in Figure 2.6 [30]. The significance of the length of the CPI, especially relative to Doppler processing will be developed in Section 2.2.4. Doppler processing is also referred to as coherent integration and results in a factor of M^2 increase in the (coherent) signal level and only a factor of M increase in the incoherent noise. The total processing gain realized due to Doppler processing is the ratio of the two or simply $10\log_{10}(M)$ dB. The results of Doppler processing can be normalized as well by dividing the result by a factor of M. This would result in a constant power level for the signal of interest, thereby forcing the power in the noise down by the coherent integration gain $10\log_{10}(M)$ [38].

Finally, the match filtered or Doppler processed results can be refined by windowing; a process by which a weighting function is applied to the data with the goal of reducing the sidelobes inherent to the data products of both processing operations [30]. Windows in the fast and slow-time domains are typically applied in the receiver [18]. The fast-time taper is applied to the reference waveform

to be used in the matched filtering process while the slow-time taper is applied to the slow-time data before the Fourier Transform [18] [30]. A windowed response typically will exhibit degradation in the main lobe peak level, widening of the mainlobe, and the sidelobes will be suppressed relative to the non-windowed response [30]. The expected peak to side lobe ratio of a waveform after matched filtering is a metric associated with a research area of its own [18].

A significant consideration with respect to signal processing is the computational load required by these operations. While some applications have time for robust, time-intensive, high-fidelity processing, semi-real time systems require low latency processing. Matched filtering is usually executed in the time domain via a Finite Impulse Response (FIR) filter implemented as a copy of the sampled transmitted waveform in the digital processing. The received data stream is multiplied by a time reversed copy of the transmitted waveform. The latency of the matched filter process is equal to the waveform length. In high-bandwidth radars like SAR, this operation is referred to as stretch processing and is often done in real-time in the analog circuitry in the receiver before sampling using a mixer.

Doppler Processing can be implemented in other ways, but the coherent style discussed here must be implemented as a block processing application due to its requirement that it relies on using data from an entire CPI. After waiting to accrue the data, a Fast Fourier Transform (FFT) which takes a number of clock cycles equal to $Mlog_2(M)$ where M is the number of pulses [14]. Fourier Transform approximations have been developed that facilitate lower latency Doppler processing at the cost of sacrificing fidelity but that are not discussed here [30].

2.2.4 Basic Radar Measurements

The two fundamental radar-enabled measurements are the range to the target, R, and the relative radial velocity of the target, v_r. As the variables associated with these measurements will appear in the mathematical description developed in Section 2.2.5, this section aims to provide an intuitive understanding of how radar measurements occur and what realistic expectations for their accuracy are.

In the case of a range measurement, the radar computes the distance to the target based on how long it took for the transmitted signal to return to the receiver or the round trip delay T. For radar applications in free space, the speed of light ($c \approx 3x10^8$ [m/s]), is the velocity of propagation of the transmitted RF wave. The product of the propagation velocity and two-way travel time is divided by a factor of two to yield the one-way distance, or range to the target in Equation 2.4 [38].

$$R = \frac{cT}{2} \tag{2.4}$$

T is found by identifying the high amplitude regions in the matched filter output referenced in Section 2.2.2.

Two scatterers can be resolved if their spacing is greater than or equal to the radar's range resolution ΔR as defined in Equation 2.5, [31].

$$\Delta R = \frac{c}{2B} \tag{2.5}$$

As was mentioned in Section 2.2.1, greater bandwidths, B, result in finer range resolution. The resolution metric used in this work is the 3-dB resolution, which is to say that if two scatterers are located far enough apart that their matched filtered response can decay to 3 dB below the peak before rising for the next target, they are sufficiently resolved [30]. Because narrow mainlobes decay faster, closely spaced targets can be distinguished with higher bandwidth. As the bandwidth increases, the range resolution or width of the mainlobe decreases [30].

The accuracy of the range measurement is defined in Equation 2.6 in terms of its standard deviation σ_R. Because a small standard deviation is preferred, it is clear that a fine range resolution or large SNR improve the accuracy [31].

$$\sigma_R = \frac{\Delta R}{\sqrt{SNR}} \tag{2.6}$$

Section 2.1 established that a moving target will impart a Doppler shift on the return. The relationship between Doppler frequency, f_D, and velocity is defined in Equation 2.7.

$$f_D = \frac{-2v_r}{\lambda} = \frac{-2|(\boldsymbol{v}_{rdr} - \boldsymbol{v}_s)|\cos(\gamma)}{\lambda} \tag{2.7}$$

Note that this relationship is in terms of the relative radial velocity, v_r, between the velocity vector of the scatterer $\boldsymbol{v}_s$ and the velocity vector of the radar, $\boldsymbol{v}_{rdr}$. To compute the result in Equation 2.7 the user must know the angle between these velocity vectors, γ. Another point of interest is that because the Doppler frequency is dependent on the wavelength of the illuminating wave, the radar's transmit frequency at the time of measurement must be known to calculate the velocity of a target of interest.

A more general calculation for the Doppler frequency is the time derivative of the relative phase of the incoming pulses. Equation 2.8 computes the instantaneous Doppler frequency as a function of time and makes no assumption that the scatterer has constant velocity.

$$f_D(t) = \frac{1}{2\pi}\frac{d\phi(t)}{dt} = \frac{-2}{\lambda}\frac{dR}{dt} \tag{2.8}$$

The resolution of the Doppler frequency measurement is defined by Equation 2.9.

$$\Delta f_D = \frac{1}{T_{CPI}} = \frac{1}{MT_{PRI}} \tag{2.9}$$

This equation clarifies why the selection of T_{CPI} is significant. As the amount of time for which the target is illuminated increases, its Doppler frequency can be resolved with a finer level of precision.

Finally, the accuracy in the Doppler frequency measurement is defined in Equation 2.10. Note that like the range accuracy measurement in Equation 2.6 it is also a function of the SNR. The derivation of this Equation 2.10 is provided in [31].

$$\sigma_f = \frac{\sqrt{3}}{\pi}\frac{\Delta f_D}{\sqrt{SNR}} \tag{2.10}$$

Now that the theoretical development of these measurement fundamentals has been presented,

basic radar system design could be completed after the scatterers of interest have been identified. The next section will show how these values present themselves empirically and completes the discussion of why receive processing is required to extract these values from the measured data.

2.2.5 Mathematical Representation

This subsection will reconsider the previously developed material in a mathematical sense. For purposes of this section, the analog transmitter and receiver components are assumed to be ideal. Complex representation is used to follow the notation in [30]. The following formulations only consider purely radial velocities.

First, the m$^{\text{th}}$ transmitted modulated RF pulse can be written as Equation 2.11 [30] where $a(t)$ is the pulse envelope, f_{RF} is the RF center frequency and $\phi(t)$ represents the waveform modulation.

$$\mathbf{s}_m(t) = a(t)\mathrm{e}^{j(2\pi f_{RF}t+\phi(t))} \tag{2.11}$$

The ideal reflection from a single point target due to the m^{th} pulse, $y_m(t)$, is a time delayed version of the transmitted signal as shown in Equation 2.12 [30]. This could equivalently be computed as the convolution of the transmitted pulse with an impulse function at the target delay. Here, $R(t)$ is the range to the target, shown in Equation 2.13 as a case where the target motion is purely in the radial direction [30].

$$y_m(t) = s_m\left(t - \frac{2R(t)}{c}\right) = s_m(t) * \delta\left(t - \frac{2R(t)}{c}\right) \tag{2.12}$$

$$R(t) = R_o - v_r t \tag{2.13}$$

The echo incident on the receiver takes the form of Equation 2.14 [30] after inserting Equation 2.13 into Equation 2.12 where $a_1 \approx \frac{1}{R^4}$. Note the negligible affect of $v_r t$ on $a(t)$ is ignored [30].

$$\mathbf{y}_m(t) = a_1(t)a\Big(t - \frac{2R_o}{c}\Big)e^{-j(\frac{4\pi}{\lambda_{RF}}R_o)}e^{j(2\pi f_{RF}t+\phi(t))}e^{-j(2\pi\frac{2v}{\lambda_{RF}}t)} \tag{2.14}$$

In Equation 2.14, the phase of the last exponential can be used to compute the Doppler frequency. The time derivative of this phase results in $\frac{2v_r}{\lambda_{RF}}$ as was predicted by Equation 2.7. If a more general case had been considered where the relative motion between the target and radar had a non-radial component, the time derivative of the corresponding phase term would have yielded a time-varying Doppler frequency.

Finally, assuming an ideal downconversion process to remove the $e^{j2\pi f_{RF}}$ term, the baseband signal incident on the radar ADC is shown in Equation 2.15. This equation includes the thermal noise of the receiver, $w(t)$, modeled as an additive white Gaussian noise (AWGN) process. Equation 2.15 represents the ideal target response and will be referenced often in the following chapters.

$$\mathbf{y}_{b\mathrm{m}}(t) = a_1(t)a\Big(t - \frac{2R_o}{c}\Big)e^{j\phi(t)}e^{-j(\frac{4\pi}{\lambda_{RF}}R_o)}e^{-j(2\pi f_D t)} + w(t) \tag{2.15}$$

More completely, however, the sampled signal due to pulse m at the ADC output in response to a scene with multiple scatterers is depicted in Equation 2.16. In this case, $\mathbf{y}_m(t)$ in Equation 2.12 would have been computed as a convolution between $\mathbf{s}_m(t)$ with a series of impulses that represents a super position of the ranges to of all targets in the radar's field of view, or the range profile $\mathbf{x}(t)$. The notation in Equation 2.16 differs from that in Equation 2.15 only in the sense that it is a discrete sampled signal and superposition has been applied to sum the reflections from K scatterers in the view of the radar. The index n represents the sample time and f_s is the sampling frequency of the radar.

$$\mathbf{y}_{tbm}(n) = \sum_{k=1}^{K}\mathbf{y}_{bm,k}(n); \quad \text{for } \Big(0 \le n \le T_{CPI} * f_s - 1\Big) \tag{2.16}$$

This approach can be applied to each of the M pulses to yield the result in Equation 2.17, the received data stream over the entire CPI.

$$\mathbf{y}(n) = \sum_{m=1}^{M} \mathbf{y}_m(n); \quad \text{for } \left(0 \leq n \leq T_{CPI} * f_s - 1\right) \tag{2.17}$$

After y(n) has been sampled, an estimate of the range profile, $\hat{\mathbf{x}}(n)$, is formed via matched filtering. Equation 2.18 represents the impulse response of the ideal matched filter and defines K as a scaling factor [18]. Equation 2.19 [30] demonstrates the matched filtering process and application of a temporal window $a_{win}(t)$. The windowing operation is optional and in the case of a uniform window, $a_{win}(t) = 1.0$

$$h(t) = Ks^*(t_0 - t) \tag{2.18}$$

$$\hat{\mathbf{x}}(t) = y(t) * h(t)a_{win}(t) = y(t) * Ks^*(t_0 - t)a_{win}(t) \tag{2.19}$$

Figure 2.7 provides a visual summary of the aforementioned derivations. Note that the nature of the estimate $\hat{\mathbf{x}}(n)$ will differ from this figure depending on the modulation of the transmitted waveform and whether windowing is applied. In this case, the transmitted waveform is an LFM and a uniform window is applied.

The estimation of $\hat{\mathbf{x}}(n)$ is the goal of some radar applications, but for others, further processing is required. Doppler processing could be performed on the match filtered data output by reformatting the received data into the cube discussed in Figure 2.6 and taking an FFT in the slow-time dimension [30]. The resulting data could be compared to a threshold via a constant false alarm rate (CFAR) detector or buffered and transmitted out of the radar for more complex processing [38]. A simplified visual representation of these processing results from the perspective of the data cube is provided in Figure 2.8. This example only includes one target and neglects the effects of noise.

The first panel in Figure 2.8 shows scattering from a target that is approaching the radar and the transmitted waveform is an LFM. The second panel shows the ideal result of the matched filtering operation, where now each column of the data cube features an impulse located at the offset associated with the target. Finally, the third panel shows the result of Doppler processing in

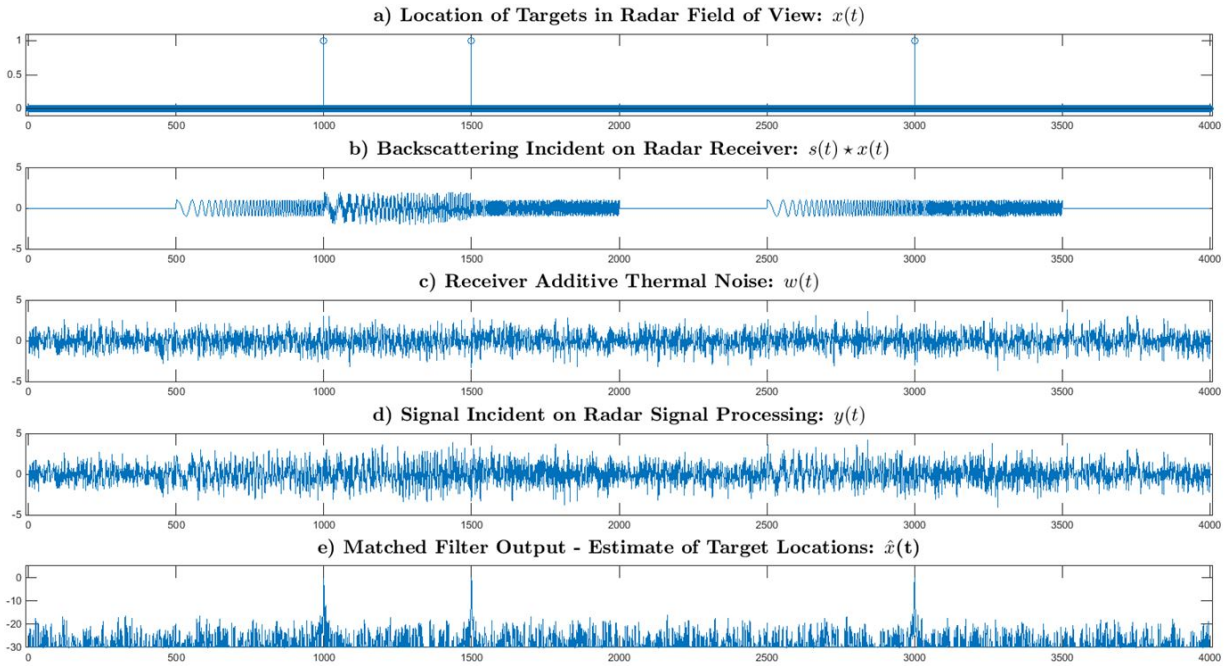

Figure 2.7: Radar signal representation.

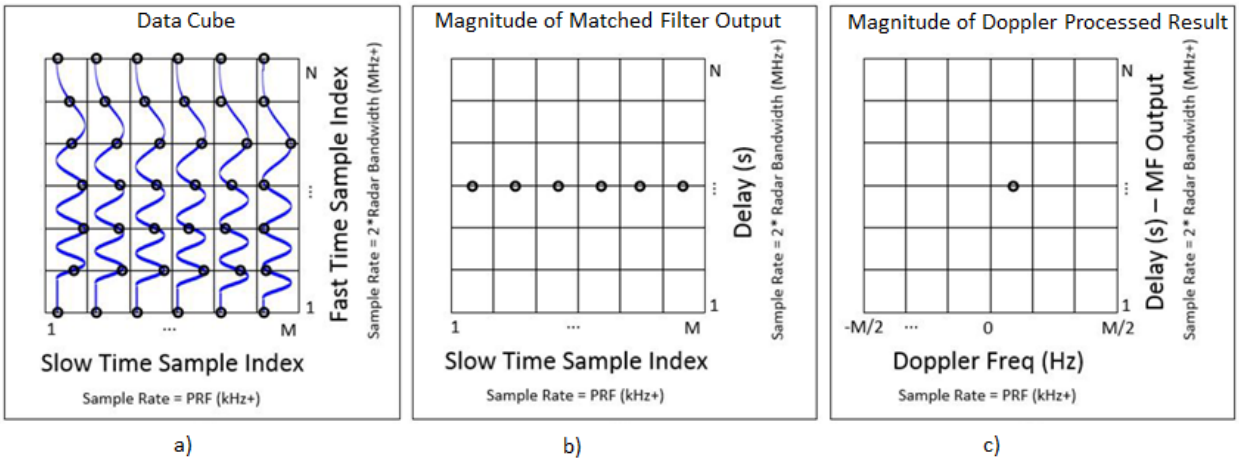

Figure 2.8: a) Formatted stream of raw received data, b) Match filtered output, c) Result of Matched filtering and Doppler Processing

which one impulse response exists at the delay and Doppler shift associated with the target. The result is a plot in terms of time delay and Doppler frequency which can be easily converted to range and velocity using Equations 2.4 and 2.7.

A higher fidelity version of Figure 2.8.c is shown in Figure 2.9.c. The red dashed lines intersect at the peak of the pulse-Doppler map and indicate the planes through which a "range cut" and a

"Doppler cut" might be taken. The result in Figure 2.9 will form a basis of comparison to the results in Chapter 6.

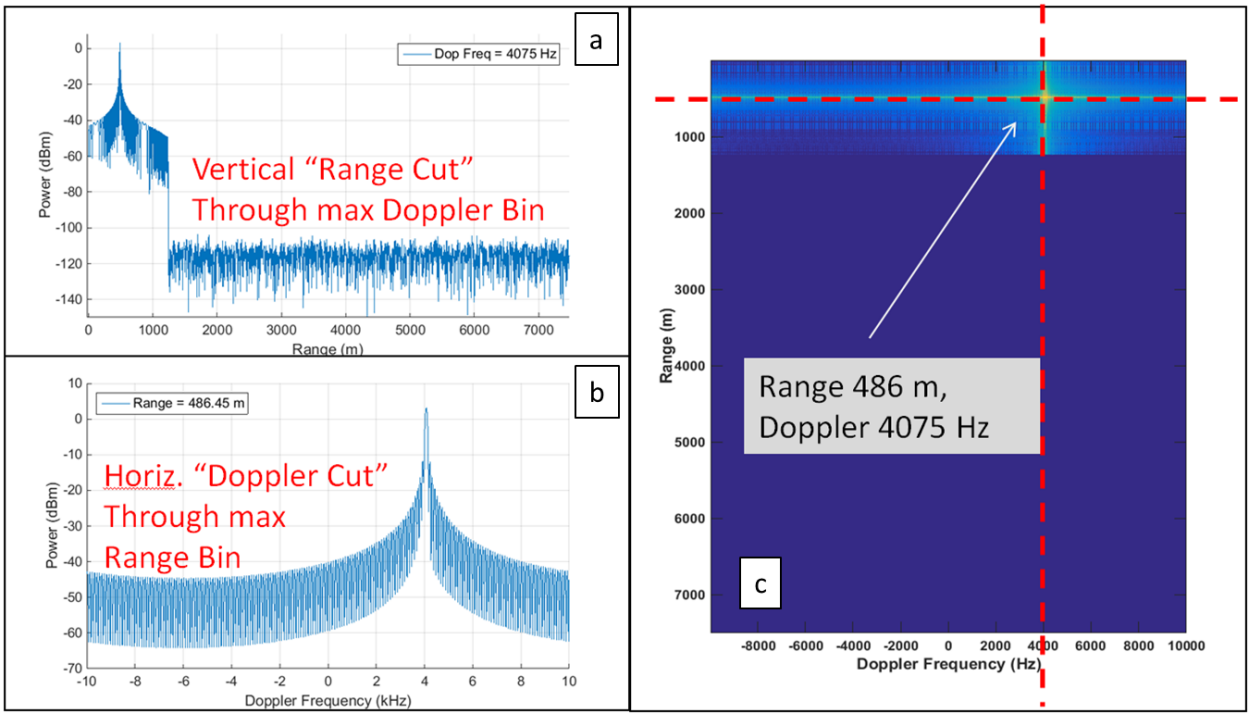

Figure 2.9: Example result from a Pulse Doppler radar.

The result in Figure 2.9.c was formed by applying a normalized matched filter in the fast-time dimension and a 800-point FFT across the slow-time axis. Figures 2.9.a and 2.9.b demonstrate the range and Doppler cuts associated with the peak range bin (indicated by the dashed lines). Without knowing the specifics about the radar or the target, these results could be used to form hypotheses about the transmitted waveform.

In conclusion, several factors go into the development of the radar model from the characteristics of the target of interest, to the transmission scheme, to the receive processing. In order to produce a high-fidelity model of the radar's environment, all of these factors must be understood.

Chapter 3

Test Architecture Models

Without one of the test methods described in the following sections, the most effective way to evaluate the performance of radar hardware is via placement of known calibration targets in a test field and comparison of the radar's measurements with theoretical results. In this method, the test target is a physical entity likely to be a trihedral or Lunenburg lens due to their relatively constant RCS over a broad range of acceptance angles [5] [41]. While the field testing approach will always have a place in a product development life cycle, it must be performed after a certain level of confidence in the radar performance has been reached. The following test methods serve the purpose of providing rigorous and repeatable evidence that a radar would perform as expected in response to idealized, yet representative, test targets before it faces the real world.

The following sections consider architectural details of two major classes of environment simulators. After presenting high level block diagrams, the idealized equations that describe their performance are considered. These equations have been developed in such a way that they are extensions of the natural target model result presented in Equation 2.15.

In contrast with the passive field test method described above, the following systems are all active targets in the sense that they manipulate the radar signal in some way before it is retransmitted. All of them can be configured with antennas to serve as field test targets, a thorough example of which is provided in [5]. For the purposes of this work, however, these test architectures are only

considered in the application where they are connected via cables directly to the radar's transmitter output port and receiver input port for bench-top system testing as was demonstrated by the groups in [17] [22]. The following sections ignore the effects of the antennas and only consider free space propagation in the sense of the attenuation due to the inverse relationship between received power and R^4.

First, two analog methods are discussed where physical delay media is placed between the radar receiver and transmitter. The final section in this chapter covers three variations of a digital architecture. Digital methods of simulating radar environments receive the most attention in this section in preparation for the experimental results provided in the final chapters. All of the following architectures are developed so that they are capable of simulating stationary and moving targets.

3.1 Delay Line Architectures

3.1.1 Coaxial Delay Lines

The analog delay line method of producing synthetic radar targets is the simplest to understand. To simulate the appropriate delay, a transmission line is cut to a length that will delay the radar signal by the desired amount. The delay line is followed by a bank of attenuators that facilitate variation of the power incident on the radar's receiver. This architecture is shown in Figure 3.1 with additional complexity included to address some of the physical limitations described in the following.

The propagation delay, t_p, through the delay line is shown in Equation 3.1 [16] where v_p is the velocity of propagation through the delay line medium, $\sqrt{\varepsilon_r}$ is the refractive index of the delay line medium, and l is the length of the delay line.

$$t_p = \frac{l}{v_p} = \frac{l\sqrt{\varepsilon_r}}{c} \tag{3.1}$$

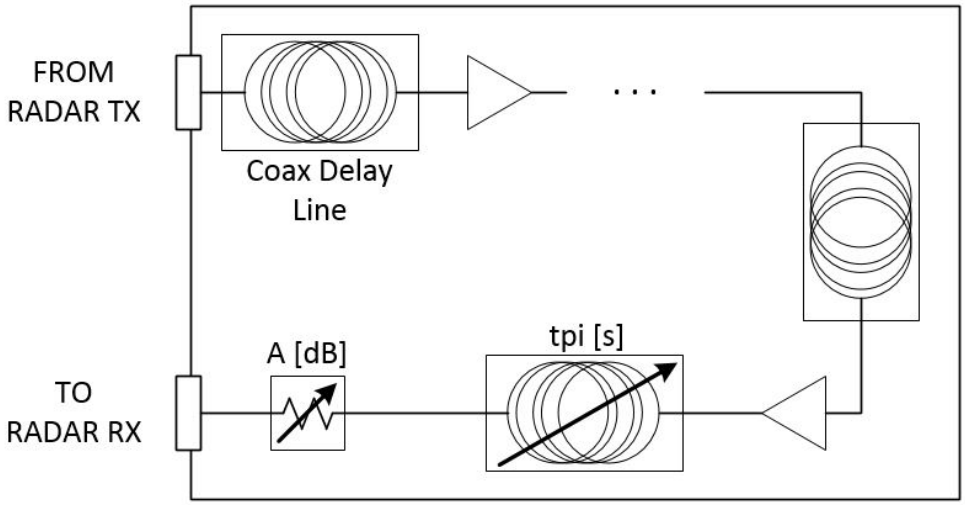

Figure 3.1: Coaxial delay line based target generator architecture. Repeaters are inserted between sections of coaxial line to overcome the significant attenuation characteristic of coaxial cable. Note the final section of delay line is variable in length.

Most transmission line media has a refractive index of approximately 1.5, meaning the velocity of propagation of an electromagnetic wave on this transmission line is scaled by a factor of $\frac{2}{3}$ relative to free space [16]. As an example, to simulate the round trip delay associated with a target at 3 km, the round trip distance is 6 km, and approximately $\frac{2}{3}(6\text{ km}) = 4$ km of coaxial cable would be required.

As previously mentioned, a variable attenuator follows the delay portion to facilitate simulation of R^4 losses. Setting the variable attenuator is complicated by the lossy nature of coaxial cable at RF, which will likely cause significantly more attenuation than desired.

To illustrate this point, a radar interacting with the previous example's ideal reflector at 3 km would expect a loss of $10\log_{10}(R^4)$ = 140 dB just due to the range to the target. If this radar's transmitted power was 10 W or 40 dBm, the nominal received power would therefore be $(40\text{ dBm} - 140\text{ dB})$ = -100 dBm. The attenuation of coaxial cable at S-Band frequencies (2 GHz - 4 GHz) varies based on material, but is at least 20 dB per 100 m [29]. So in the scenario above where 4 km of cable would be required to simulate the delay to the target, the total simulated attenuation would be 800 dB, leaving the power at the receiver to be -760 dBm, or 660 dB lower than expected. To simulate the example scenario with coaxial cable, it is obvious that several re-

peaters would be needed to boost the power to be representative of a real-world reflection as shown in Figure 3.1. Ideally, these amplifiers would be selected so that the total power at the input of the variable attenuator is high enough that the attenuator settings could exercise the entire dynamic range of the radar receiver.

To simulate a variety of ranges or moving targets, the length of the coaxial cable would need to be varied. This flexibility could be achieved by adding a switch matrix and a bank of shorter lengths of coaxial cable that could be added to or removed from the propagation path in various combinations. Depending on whether the switching speed of the coaxial switches is sufficient to simulate the change in range of the target, a single sideband (SSB) modulator may be required to add the representative Doppler shift (not pictured). Multiple targets could be simulated by adding an RF splitter to the diagram in Figure 3.1 before the variable delay and attenuation sections. The paths could be delayed and attenuated independently and then combined before entering the radar receiver.

The discussion so far has left out two harder to characterize but possibly more detrimental effects. The first, dispersion, is a phenomena by which the velocity of propagation on a transmission line varies with frequency, causing linear distortion in the output signal [29]. While dispersion in coaxial cable is often considered negligible for short distances, the 4 km distance in the previous example would likely exhibit significant distortion from dispersion [37] [24]. Second, the noise enhancing characteristic of the chain of lossy transmission line and amplifiers has been omitted. These repeater sections may degrade the SNR past the point of being representative of a real world return.

The mathematical representation of the baseband signal incident on the radar receiver after reflecting off of a static target simulated with a coaxial delay line is shown in Equation 3.2. The addition of w(t) represents AWGN contributed by the amplifiers and attenuator in the transmitter, the weighting of the transfer function of coaxial cable and repeater sections are contained in h(t), A represents the attenuation setting of the variable attenuator in dB and recall t_p is the propagation delay through the coaxial line from Equation 3.1.

$$\mathbf{y}_{bm}(t) = h(t)10^{\frac{-A}{10}}a(t-t_p)e^{-j(2\pi f_{RF}t_p)} + w(t) \tag{3.2}$$

A moving target would be described with Equation 3.3.

$$\mathbf{y}_{bm}(t) = h(t)10^{\frac{-A}{10}}a(t-(t_p+t_{pi}(t)))e^{-j(2\pi f_{RF}(t_p+t_{pi}(t)))} + w(t) \tag{3.3}$$

To simulate this target motion, the variable portion of the propagation delay (indicated as t_{pi} in Equation 3.3) would need to be changed at the range rate. The switching rate required for the variable delay, f_{sw}, can be computed as shown in Equation 3.4 where t_1 is the final delay, t_0 is the start delay and δt_{pi} is the smallest coaxial delay increment.

$$f_{sw} = \frac{|(t_1 - t_0)|}{\delta t_{pi} T_{CPI}} \tag{3.4}$$

Note that as long as f_{sw} is less than the radar PRF, there will be several slow time samples in a row with the same phase shift. The aforementioned optional external Doppler modulator is required if the switching rate in Equation 3.4 can not be achieved to apply the appropriate Doppler shift.

While the analog delay method for simulating a target is clearly a feasible solution, the significant sources of distortion at distances applicable to radar testing makes it an impractical approach [24].

3.1.2 Optical Delay Lines

Optical delay lines are a more attractive option than the previous implementation for several reasons. The first is that the insertion loss of fiber optic cable is on the order of 0.5 dB per km for data rates of up to 20 GHz and beyond [7] [3]. This superior transmission characteristic means the 4 km target delay scenario in the previous section can be easily achieved without needing repeaters. Another reason is that while the propagation velocity of fiber optic line is similar to coax (so the

required length of cable is similar), fiber optic cable is much smaller diameter, lighter, has a smaller bend radius, and has a lower cost, which makes it a feasible medium for simulating long delays in rack mounted test equipment [22] [23].

The optical delay line architecture is illustrated at a high level in Figure 3.2 and features an RF to fiber otpic link [22]. The incoming RF signal modulates a laser in the optical transmitter which generates a fluctuating light pattern. This light pattern propagates through the fiber optic cable and is received by a photodiode in the optical receiver where it is converted back to an RF signal.

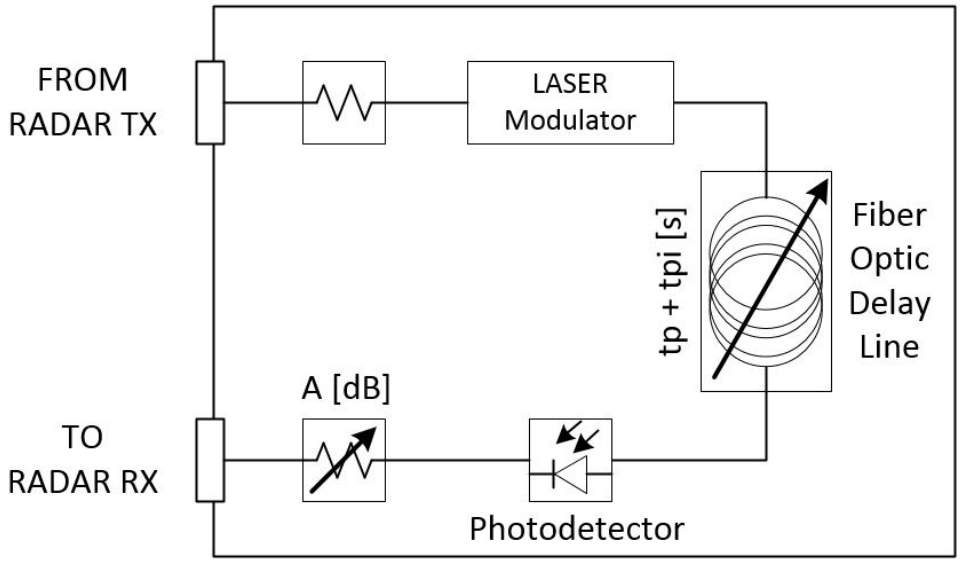

Figure 3.2: Fiber optic delay line based target generator architecture [22]. Note the delay media is variable in length.

Again, in contrast with the coaxial architecture in Figure 3.1, this architecture requires no repeaters. Furthermore Figure 3.2 indicates the use of an attenuator on the front end of the delay generator. This attenuator is used to reduce the radar's transmit power to a level suitable for the optical transmitter modulation process.

It has been established that attenuation by the fiber optic line is not of significant concern, but potential issues such as dispersion and SNR remain. Dispersion in fiber optic lines is related to the the laser's light spectrum line width [3]. The author in [23] documented a case in which a match between the modulating laser and the fiber media's "zero dispersion" point resulted in 1 ps of dispersion over a 31.6 km link. This implies that dispersion effects can be largely avoided for

most radar applications with careful design. The group in [24] confirms that single-mode fiber optic delay lines are appropriate for radar testing.

Regarding the noise performance and dynamic range of RF over fiber links, the aggregation of study results presented in [7] lists dynamic ranges on the order of 115 dB and noise figures of 20 dB or less at 10 GHz. These results offer sufficient performance for most radar applications.

The mathematical representation of a baseband signal incident on a radar ADC after interfacing with a fiber optic target generator match those developed in Equations 3.2 and 3.3 with different values for $h(t)$, $w(t)$, and A as appropriate for this application. The switching rate for the variable delay would also match that expressed in Equation 3.4 with an updated δt_{pi}.

While the performance of optical delay lines are sufficient to impart negligible distortion on an RF signal, they share many of the cumbersome architectural elements of the analog method in the previous section. Both coaxial and fiber optic delay lines require precise cutting of delay line to achieve a radar delay. Several precise cuts need to be made to construct the variable delay portion. Furthermore the performance of the fiber optic cable and modulating laser are sensitive to temperature [23]. The digital architectures discussed in the following section are physically simpler to implement. Their reliance on digital signal processing algorithms facilitates design flexibility while making the target simulation more precise and repeatable.

3.2 Digital Memory Architectures

The first patent for simulation of radar returns using a digital memory architecture was awarded in 1974 [34]. The advent of Field Programmable Gate Arrays (FPGA) has facilitated reconfigurable digital kernels capable of simulating a variety of targets with algorithms that can be upgraded as necessary [42] [47]. There are two architectural elements that limit key performance metrics of these devices. First, maximum data rate through the system dictates the delay resolution. The data rate can be limited by the ADC / DAC sampling rates, FPGA operating limitations, or speed of dual port memory devices [34]. Second, the sampling rate and the number of quantization

bits available in ADC and DAC architectures dictate the instantaneous bandwidth of the target generator and the dynamic range of the output signal respectively [34]. Because target generator architectures typically pull from the same technology set as the radar designs they are built to test, these limitations don't prevent the technology from meeting test requirements in all cases. Instead, they serve as critical design constraints that must be met for realistic environment simulation. A basic digital target simulator architecture is shown in Figure 3.3 [34] [4].

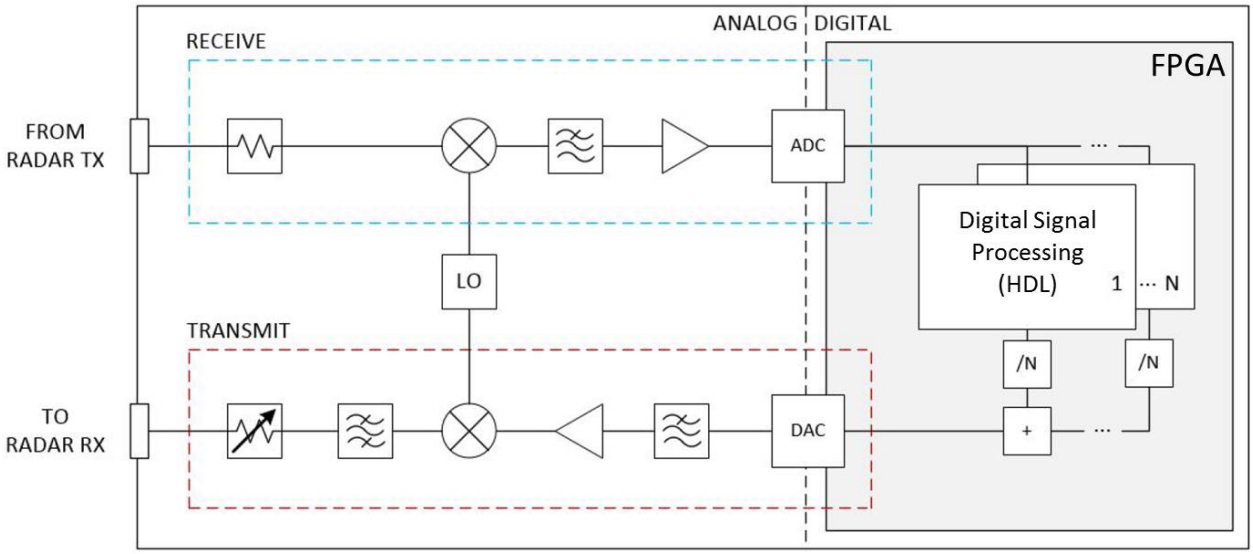

Figure 3.3: General laboratory digital target generator diagram. The figure includes optional multiple digital kernels to facilitate multiple target simulations.

The architecture in Figure 3.3 bears similarities to the radar block diagram architecture in Figure 2.2. The analog portion of the architecture exists for frequency conversion to and from an IF that is acceptable for interface with the ADC and DAC. The receiver of the target generator is directly connected to the transmitter of the radar, which necessitates the front end attenuator to prevent damage or saturation of the mixer and ADC. The manipulation of target delay and Doppler shift is completed in the digital logic implemented in an FPGA, ASIC or a combination of ICs. After reconstruction in the DAC, the IF radar data is upconverted to the radar RF. As in the analog architectures in Figures 3.1 and 3.2, the variable resistor at the output of the transmitter represents an attenuator bank that exists to emulate R^4 effects.

Disregarding the benign inversion of the analog subsection of the design, the unique element of

this architecture is the digital kernel. There are a multitude of digital effects to consider associated with this subsection; ranging from the ADC/DAC-caused quantization noise to digital signal processing (DSP) algorithm and digital logic implementation details. The real flexibility of the design is that the target emulation is totally controlled by and executed in firmware, so reconfiguration or incorporation of changes to the architecture can be done quickly with zero material cost. Furthermore, multiple targets that are independent other than in power level can be simulated by adding independent kernels in parallel in the digital realm as shown in Figure 3.3.

The following sections cover algorithms that can be used to achieve similar types of targets with different levels of fidelity. The signal representations developed in tandem with these architectures are ideal and do not include loss or latency factors. Those issues will be addressed in Chapter 4.

3.2.1 Memory-Only Architecture

The basic requirement for this architecture is a block of dual-port random access memory (DPRAM) capable of simultaneous read and write. The bulk two-way delay to the target is emulated by the amount of time that the sampled radar waveforms are stored in the target generator's memory. Static and moving targets can be simulated with no more than a memory bank and a control algorithm for the memory address pointers as shown in Figure 3.4. Note that this design operates asynchronously from the radar and relies on no knowledge about its operation.

The fundamental parameter of the memory-only architecture is the target generator delay resolution, t_d which is calculated as the reciprocal of the FPGA data rate f_{clk}. In this architecture, it is assumed that the clock rate is equal to the ADC sampling rate $f_{s,ADC}$ and the data rate. [34]. After the digitized samples are stored in memory, the difference between the read and write pointers can be used to calculate the delay introduced by the memory, D_{MEM} as shown in Equation 3.5. In Equation 3.5, $addr_{WR}$ and $addr_{RD}$ are the read and write pointer locations. The pointer spacing, or number of memory locations or clock cycles that the read pointer lags the write pointer by is represented as Δ_{addr}.

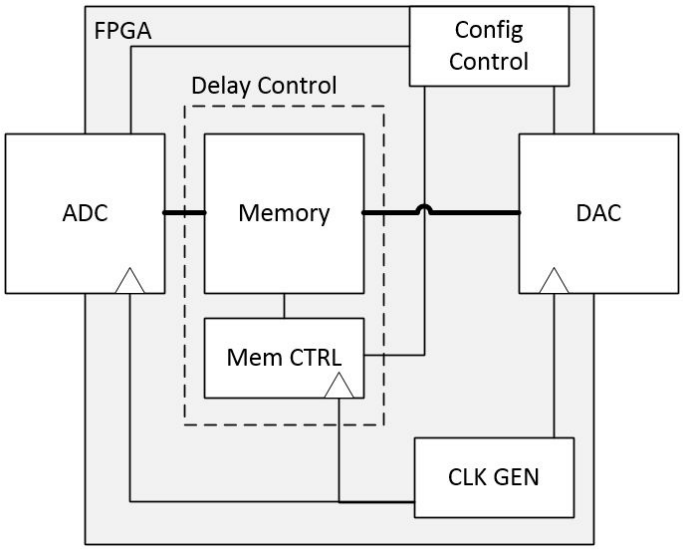

Figure 3.4: Memory Only configuration

$$D_{\text{MEM}} = (\text{addr}_{\text{WR}} - \text{addr}_{\text{RD}})t_d = \Delta_{\text{addr}} t_d \tag{3.5}$$

Note that the delay computed in Equation 3.5 applies to the intentional memory introduced delay only (D_{MEM}) and does not take the latency due to other hardware or algorithm features into account. Unlike the analog architectures, this delay value is not vulnerable to fluctuations with time or temperature other than those that affect the stability of the FPGA clock.

Using the definition in Equation 3.5, the maximum delay the memory can introduce can be calculated by setting Δ_{addr} equal to the total number of addresses in the memory. The simulated range, R is calculated by inserting the result of Equation 3.5 into Equation 2.4, making the simulated range equal to Equation 3.6.

$$R = \frac{\Delta_{\text{addr}} t_d c}{2} = \frac{D_{\text{MEM}} c}{2} \tag{3.6}$$

Likewise, the minimum range to be simulated can be calculated by setting Δ_{addr} to 1; demonstrating the case where the digitized samples are only stored in memory for one clock cycle before being retransmitted and the delay through the kernel is equal to the delay resolution. This mini-

mum range is also equal to the minimum value that the target generator can increment the range by the minimum range step size δR.

During operation, the read and write memory address pointers cycle through the memory contents at the sampling rate. The active memory locations change every clock cycle as a new data sample is available. The spacing of the read and write pointers remains constant when a stationary target is the subject of the simulation.

A visualization of the memory algorithm from the perspective of a memory stack is provided in Figure 3.5. If the sampling rate was 500 MHz for example, each memory cell shown in the figure would represent 2 ns. The configuration in Figure 3.5.a then, depicts a delay of 30 ns, because there are 15 sample intervals separating the read and write pointer. The subsequent clock cycle is shown in Figure 3.5.b. Note the spacing remains the same, but both the read and write pointers have advanced.

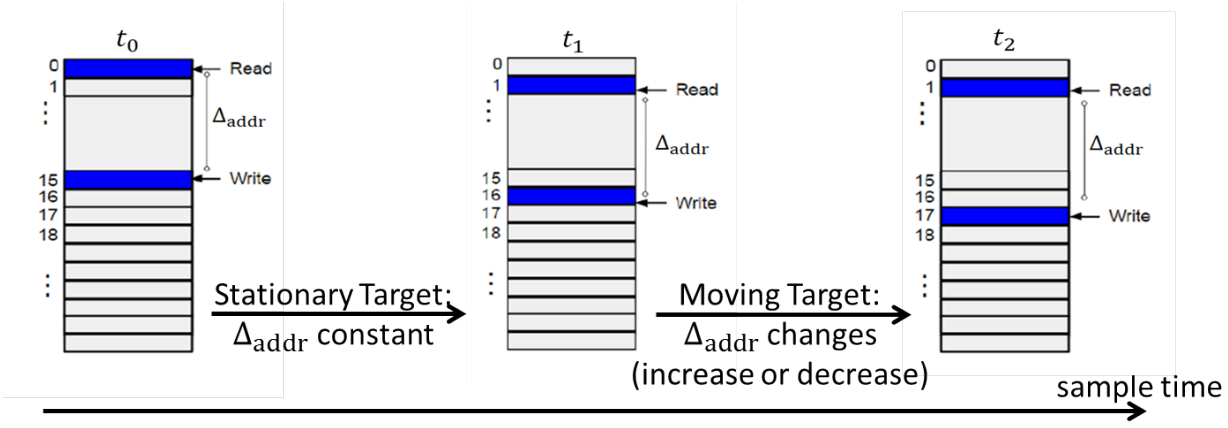

Figure 3.5: Memory Read and Write Process Illustration. The target is stationary between a) and b) and is moving between b) and c).

The mathematical complex representation of the down converted received signal at the input to the radar ADC, $\mathbf{y}_{bm}$ after interfacing with a digital memory simulation of a static target is shown in Equation 3.7. This should be compared to the ideal target return in Equation 2.15. In this equation, A is the setting for the switched attenuator and $w(t)$ represents Additive White Gaussian Noise (AWGN) contributed by the receiver. A more comprehensive representation of $\mathbf{y}_{bm}(t)$ that includes non-ideal effects of the digital architecture will be developed at the end of Chapter 4.

$$\mathbf{y}_{bm}(t) = 10^{(-\frac{A}{10})} a(t - \Delta_{\text{addr}} t_d) e^{-j(2\pi f_{IF} \Delta_{\text{addr}} t_d)} + w(t) \tag{3.7}$$

Equation 3.7 exposes a critical feature of the digital target simulator architecture. Note that the phase shift in the exponential is in terms of f_{IF} rather than f_{RF} as it was for the analog architectures in Section 3.1. This difference is due to the fact that the radar data was down converted to an IF for sampling so the delay operation is being performed on the IF signal. Because of the relationship between phase and wavelength, a different phase offset will be applied to this signal than if the architecture were capable of digitizing and delaying the RF waveform without frequency down conversion. In the case of a stationary target, this phase offset is a constant that will be applied to all pulses and is of no consequence.

The simulation of time varying delay can be accomplished using this architecture by changing the spacing of the memory pointers in real time; increasing or decreasing Δ_{addr} by manipulating the read pointer address. To increase the simulated range, the read pointer must pause for one clock cycle while the write process continues to store new samples as normal. This case is demonstrated in Figure 3.5.c. The previous clock cycle shown in Figure 3.5.b has a spacing of 15 memory cells. In Figure 3.5.c, the write pointer has advanced one cell, but the read pointer is accessing the same data as the previous clock cycle to allow the delay between the pointers to increase. A decrease in the simulated range would correspond with the read pointer skipping ahead one memory cell, again while the write process proceeds as normal. The rate at which Δ_{addr} is changed, referred to as the update rate $f_{\Delta a}$, is governed by Equation 3.8 (which is identical to Equation 3.4 for the delay line architectures with a substitution of t_d for δt_p).

$$f_{\Delta a} = \frac{2|(R_1 - R_o)|}{c t_d T_{CPI}} = \frac{|(t_1 - t_o)|}{t_d T_{CPI}} = \frac{N_{\Delta a}}{T_{CPI}} \tag{3.8}$$

This equation effectively computes the required number of pointer difference changes, $N_{\Delta a}$, by normalizing the scatterer's total change in delay over the CPI ($|t_1 - t_0|$) by the target simulator's delay resolution. This result is divided by the CPI to yield the rate at which the range must be

updated, $f_{\Delta a}$. Furthermore, to simulate a non-constant velocity over the interval, the total number of memory pointer spacing changes during the CPI would remain the same, but $f_{\Delta a}$ would need to vary with time.

The lower limit on the range rate that can be simulated with this method is set by the time duration of the simulated scenario relative to the delay generator resolution. The simulation is designed to last for a certain number of clock cycles; a time duration that is necessarily greater than the radar's CPI. For obvious reasons, if the target is moving so slowly that the total motion over the CPI is less than the target generator resolution, the pointer spacing will never change and no motion will be logged. Given a radar CPI, this target generator architecture is only capable of simulating stationary or moving targets that will see at least one range update during the CPI.

While there is no hardware-imposed upper limit on the range rate, it is constrained by the distortion caused by changing the pointer spacing in real time. Each time the pointer spacing is changed, a discontinuity is introduced in the output data because one of the stored samples is either skipped or repeated for the change to occur. For a low range rate, the likelihood of one of these discontinuities occurring during a pulse is slim. High range rates increase this likelihood, and at some point the missing or repeated samples would cause the quality of the output waveform to degrade too significantly to be representative of a real world target. As will become obvious in the examples in Chapter 6, this upper limit is not of concern with modern data rates and realistic velocities.

The discontinuity associated with the memory pointer change is characterized by a phase shift to the sampled data as shown in Equation 3.9.

$$\Delta\phi = t_d * f_{if} * 360 \tag{3.9}$$

Note that the phase shift is associated with the IF frequency. As the delay step size approaches an appreciable part of the IF period, the resulting discontinuity will be more extreme. Therefore it is likely that lower IF frequencies will be less affected by this result.

The coarse nature of the memory stepping process also introduces the non-ideal condition

where the simulated target will appear to remain perfectly stationary for several slow-time samples in a row due to the limited delay resolution of the target generator. This quantization in range makes the target appear to be experiencing jerk-like motion rather than continuous constant velocity motion. The effects of these discontinuities on the radar's Doppler spectrum and quality of the simulated target are the subject of Chapter 6.

The mathematical representation of a moving target simulated with a dynamically configured memory block is provided in Equation 3.10. This equation resembles Equation 2.15. Note that the memory pointer spacing is now written as a function of time, $\Delta_{addr}(t)$.

$$\mathbf{y}_{bm}(t) = 10^{(-\frac{A}{10})} a(t - \Delta_{\text{addr}}(t)t_d) e^{-j(2\pi f_{IF} \Delta_{\text{addr}}(t) t_d)} + w(t) \tag{3.10}$$

AGain, the exponential in Equation 3.10 reveals a serious non-ideal effect of simulation of a moving target solely by varying pointer spacing. The time-varying delay due to $\Delta_{addr}(t)t_d$ causes a Doppler shift equal to $\frac{2v}{\lambda_{IF}}$. Unlike the delay line cases that operate at the RF (Equation 3.3), in the case of the second exponential, the dependence of the phase shift on the IF will cause the range rate of the simulated scatterer to conflict with the Doppler shift computed by the radar's receive processing. The target generator output spectrum will be shifted by a Doppler frequency associated with the correct velocity motion at the IF; a factor of $\frac{f_{IF}}{f_{RF}}$ lower than it should be if it were illuminated by the RF pulse. Conversely if the memory pointer spacing change occurred frequently enough to create the correct Doppler shift, the total range change of the target would be a factor of $\frac{f_{RF}}{f_{IF}}$ too high.

Whether this architectural flaw is significant is based on the complexity of the radar processing and whether the radar has been designed to compare separate computations of range rate and Doppler shift before identifying a situation of interest [4] [13]. Regardless, it is certainly a non-ideal effect inherent to environment simulation via this algorithm.

3.2.2 Memory and Single Sideband Doppler Architecture

The architecture discussed in this section refines the memory-only architecture described in the previous section by incorporating a SSB modulator to correct for the insufficient Doppler shift. The memory and SSB Doppler architecture is illustrated in Figure 3.6 in which the delay control subsection of the diagram is unchanged from Figure 3.4.

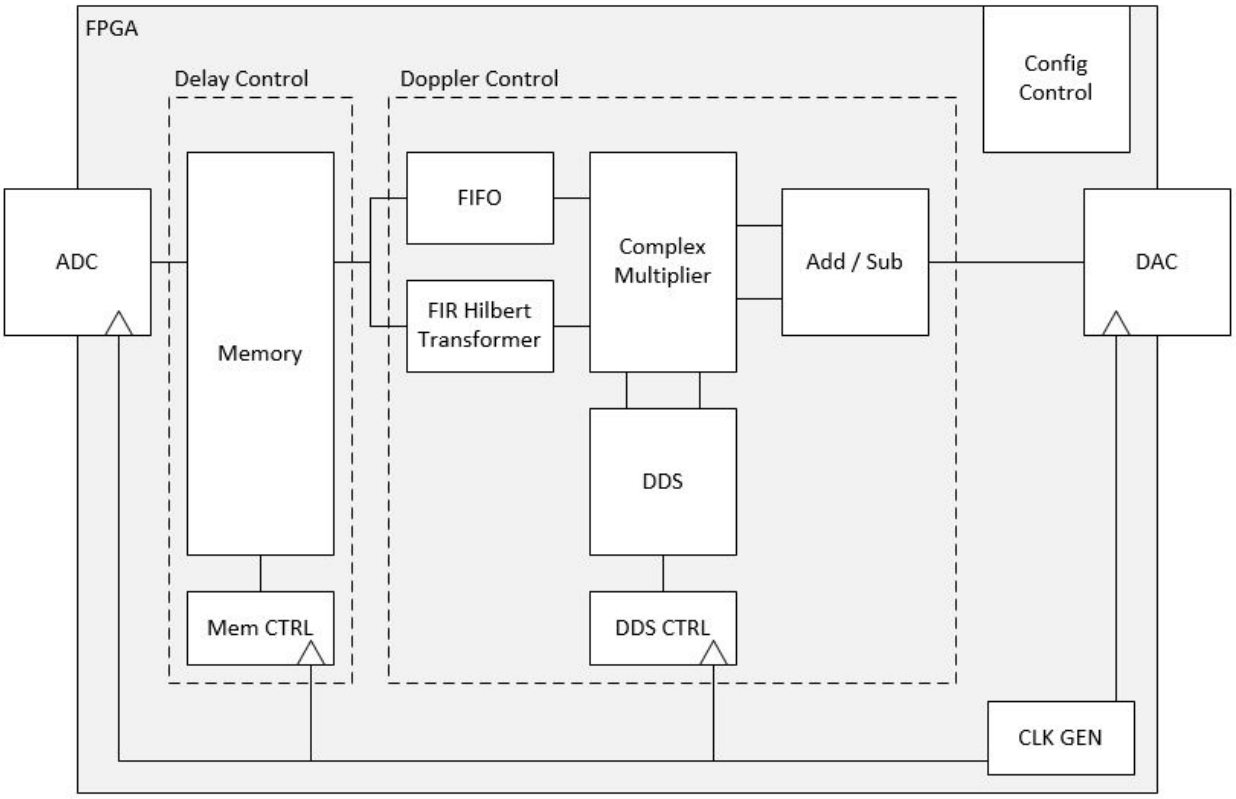

Figure 3.6: Memory and SSB Modulator

A SSB modulator operates by first performing in-phase and quadrature-phase (I and Q) sampling on the waveform. The in-phase data is equal to the original input signal, while a 90^o phase shift of the I channel produces the quadrature-phase channel [20]. In Figure 3.6 the quadrature path is generated by a finite impulse response (FIR) filter implemented as a Hilbert Transformer (an all-pass filter that performs a -90^o phase shift to positive frequencies and a $+90^o$ phase shift to negative frequencies) [10] [20]. The frequency spectrum of the output of the Hilbert Transform, $\hat{S}(f)$, is provided in Equation 3.11 [10] where $S(f)$ is equal to the Fourier Transform of the

sampled signal s(t).

$$\hat{S}(f) = \begin{cases} -jS(f) & \text{for } f \geq 0 \\ +jS(f) & \text{for } f < 0 \end{cases} \tag{3.11}$$

The in-phase path in Figure 3.6 is passed through a FIFO to delay the data by an amount equal to the group delay of the FIR filter; a metric discussed further in Chapter 4 [20] [35].

The I and Q channels are fed in to a complex multiplier where the I channel is multiplied by a cosine oscillating at the Doppler frequency and the Q channel is multiplied by a sine wave oscillating at the Doppler frequency [20]. The resolution of the Doppler shift that can be generated with the DDS is the subject of Chapter 4.

The final addition and subtraction block performs sideband selection [20]. Adding the two channels cancels the lower sideband and yields a positive Doppler shift. Subtracting the Q channel from the I channel yields a negative Doppler shift by suppressing the upper sideband [20]. The sideband rejection capability of the SSB modulator is directly related to how well matched the amplitude and phase of the IQ channels are. Because the I channel is simply delayed, not filtered, any non-ideal effects of the Hilbert Transform FIR filter on the Q channel will result in channel mismatch and imperfect cancellation of the unwanted sideband [20].

Reconsidering the result in Equation 3.10, it is clear that applying a Doppler shift equal to the ideal f_d calculated with Equation 2.7 would yield an incorrect result. The setting of the DDS must take into account the IF frequency-induced shift that will already be present on the signal when it enters the SSB modulator. The DDS setting should be $f_{DDS} = f_d - (\frac{2v}{\lambda_{IF}})$.

The mathematical description of the Doppler corrected output is give in Equation 3.12.

$$\mathbf{y}_{bm}(t) = 10^{(-\frac{A}{10})} a(t - \Delta_{\text{addr}}(t)t_d) e^{-j(2\pi f_{IF}\Delta_{\text{addr}}(t)t_d)} e^{j(2\pi(f_d - (\frac{2v}{\lambda_{IF}}))t)} + w(t) \tag{3.12}$$

This result will be reconsidered in the concluding section of Chapter 4 after the sources of error inherent to the architecture have been discussed in detail.

3.2.3 Fine Delay Control Architecture

The way to reduce the delay quantization effect noted in Equation 3.9 is by decreasing the minimum delay step, t_d. This results an an increase to the rate at which this phase shift can occur and ultimately a decrease in the abrupt phase change in Equation 3.9. Increasing $f_{\Delta a}$ for a given velocity is only possible via changing the sampling rate by some factor U. The complete operation would be to increase the data rate, interpolate, shift the data by the new minimum delay step and then decimate the data to return to the original sample rate.

A block diagram including the fine delay operation is shown in Figure 3.7. The stationary and moving target equations would be equal to Equation 3.12 with t_d replaced with $t_{d,new} = \frac{t_d}{U}$.

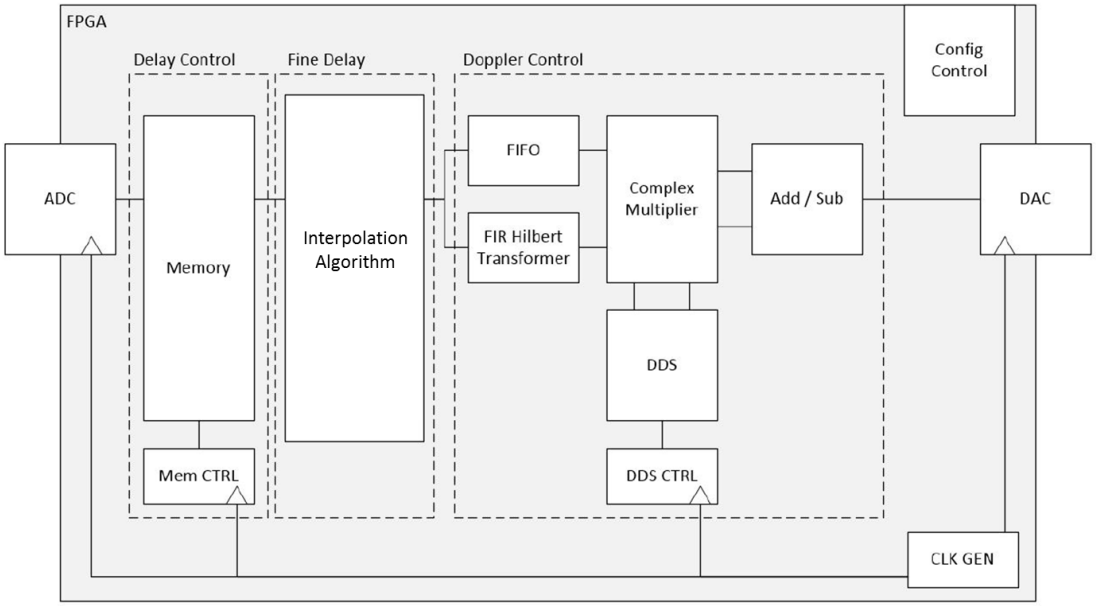

Figure 3.7: Memory and SSB Modulator with Fine Delay

In order to increase the sampling rate so that a phase shift could occur before each pulse, a sample rate increase by a factor greater than 10 would be required. This is highly infeasible with the Nyquist sampling requirement associated with typical radar bandwidths pushing the upper limits of FPGA clock speeds. A high-latency implementation could be to offload the data to an onboard processor. One attractive solution is the architecture shown in Appendix 2. The results of the three architectures discussed in this section are demonstrated in Chapter 6.

Chapter 4

Signal Quality Artifacts

The previous chapter provided general descriptions of three digital radar environment simulator architectures. This chapter goes beyond those idealized descriptions to focus on the sources of error inherent to each implementation. The following first discusses architecture independent sources of error, then delves into the non-ideal characteristics that are specific to the optional elements of the target generator algorithm. The sources of error can be characterized as they impact the radar's major measurement domains; time, frequency, and amplitude. The considerations in the following include not only sources of error, but occasionally design rules to ensure robust performance. Finally, the distortion effects of all the architectural elements will be applied to enhance the device equations in Chapter 3.

4.1 Architecture Independent Error Sources

4.1.1 Analog Receiver

Referring to the general digital target generator architecture in Figure 3.3, the first section to consider is the analog receiver. Careful receiver design is the first step in maintaining signal integrity and is the key to conditioning the data before sampling.

The design of the target generator receiver is simpler and less constrained than the receiver of

a typical radar. First, the target generator will have no unwanted signals at the input because it is directly connected to the radar transmitter. This eliminates the need for a preselector filter before the mixing stage. Second, this direct connection sets the input power and SNR at the input to the receiver equal to the radar's transmit power and output SNR. This input power is likely high enough to necessitate the addition of a large attenuator on the receiver's front end to protect the mixer from saturation.

Even though the input SNR and absence of spectral congestion are superior to that of a typical receiver, the target generator receiver can still be a source of two deleterious effects; spurious signals and noise [29]. Spurious signals will arise from insufficient filtering in combination with poor design of the mixing circuit that handles the RF to IF conversion. Local oscillator (LO) bleed through, LO harmonics, and insufficient rejection of the image frequency and higher order modulation terms could be present in the spectrum after the mixing stage in absence of careful filter selection [29]. Insufficient filtering will allow signals in upper Nyquist zones to alias down into the band of interest and distort the input to the target generator DSP algorithms [20].

The second source of undesired energy in the receiver is the thermal noise generated by every component in the chain that passes through the noise equivalent bandwidth, or IF bandwidth of the receiver [29] [30]. High attenuation resistors and high gain amplifiers tend to be the greatest contributors of thermal noise and therefore degradation of the SNR. The significant front end attenuation included in Figure 3.3 would be considered inadvisable in a radar receiver, because the first element in the receive chain has the greatest effect on the equivalent noise temperature of the receiver, $T_{e,rx}$. Detailed analysis of the system defined in Chapter 5 is provided in Appendix A and shows that in this case, the front end attenuation stage will not compromise performance.

The effect of the target generator receiver on the radar signal is summarized in Table 4.1 in terms of amplitude effects A_{rx}, delay effects D_{rx}, frequency shift f_{rx} and additive noise with a power of $P_{n,rx}$.

The parameters listed in Table 4.1 that are designed to meet a specific numeric requirement are G_{rx} and f_{rx}. The remaining parameters D_{rx}, $H_{rx}(f)$, $P_{n,rx}$are minimized in the design process and

Table 4.1: Analog Receiver Effects

Delay	D_{rx} (measured)
Amplitude	$A_{rx}(f) = G_{rx}H_{rx}(f)$
Frequency Shift	$f_{rx} = f_{RF} - f_{IF}$
Noise	$P_{n,rx} = kB_{IF}G_{rx}(T_{in,rx} + T_{e,rx})$

set to be below some acceptable threshold with a certain level of design margin. While the values of these parameters can be predicted with theory, they are best measured because their values are susceptible to manufacturing variability. The delay through the receiver D_{rx}, for example, includes delay through components and the traces that connect them and ns accuracy in delay is required for target simulation. The function $H_{rx}(f)$ represents the aggregation of the magnitude responses of each RF component in the receiver chain normalized to 1, while the ideal gain or attenuation values are included in G. The ideal value for $H_{rx}(f)$ is unity, which would imply that each component has a perfectly flat band pass response. Finally the noise power added by the target generator receiver is computed with the last equation in Table 4.1 where B_{IF} is the IF bandwidth of the receiver and T_{in} is equal to the output noise power from the radar's transmitter. Detailed noise calculations are located in Appendix A.

4.1.2 Sampling

The ideal input to the ADC has a power level that matches the ADC's full scale range and a spectrum that is band-limited to occupy one Nyquist zone with the ADC analog bandwidth [25]. Meeting these two requirements maximizes the SNR after sampling and guarantees that signal distortion due to aliasing does not occur respectively.

Assuming the incoming signal has been conditioned so that the input spectrum meets the above criteria and has infinite SNR, the ideal SNR after the sampling process is defined in Equation 4.1 where N is the number of sampling bits of the ADC [25]. The noise level indicated in this SNR computation is not the thermal noise associated with the incoming signal (which is zero in the infinite SNR case), but quantization noise generated during the sampling process.

$$SNR_{out,ADC} = 6.02N + 1.77 \quad [\text{dB}] \tag{4.1}$$

This SNR definition assumes that the input to the ADC is at full scale or requires all of the ADC sampling bits for representation. The full scale power level of an ADC is computed with Equation 4.2 under the assumption is that the ADC is matched to a 50-ohm system.

$$P_{FsADC} = 10log_{10}\Big(\frac{(V_{RMS})^2}{50(0.001)}\Big) \quad [\text{dB}] \tag{4.2}$$

If the magnitude of the incoming signal does not meet the FS range, it does not require all N bits for quantization and Equation 4.1 would be computed with N set so the actual number of bits required, which will be lower than the total number of bits available. The quantization noise power will remain constant, and therefore the lower value for N in Equation 4.1 due to a lower signal power results in a lowering of the SNR. Quantization noise error variance is calculated as shown in Equation 4.3 [20] where V_p is the full scale maximum input voltage of the ADC and $q = \frac{2V_p}{2^N}$ is the is the voltage level represented by the least significant bit.

$$\sigma^2_{ADCniose} = \frac{q^2}{12} = \frac{V_p^2}{3 * 2^{2N}} \tag{4.3}$$

It is worth noting that careful design will set the power of the thermal noise at the input to the ADC above the quantization noise level. If that is the case, post processing techniques can be used to improve the SNR. Furthermore, the ADC will not further degrade the SNR of the sampled signal, but Equation 4.1 can only be used for a rough order of magnitude estimate of the SNR [20].

The physical realities inherent to the sampling process yield unwanted spurious signals in the output of the ADC as detailed in [28]. The power level of the strongest of these signals relative to the carrier is captured in a term called spurious free dynamic range (SFDR) [28]. Another metric, the signal to noise and distortion ratio (SINAD), compares the power in the signal to the sum of the noise power and maximum spurious signal level. SINAD can replace SNR_{ADCout} in Equation 4.1 to calculate the effective number of bits (ENOB), N, when all sources of distortion are considered

[25]. The ENOB is a measured device parameter that corresponds to the effective SNR_{ADCout} and is an ADC-specific parameter found in the device data sheet. While the number of quantization bits must be used in Equation 4.3, ENOB should be used in 4.1 [25].

Another significant source of error in ADC operation is the time domain jitter inherent in the sample clock. Jitter, often on the order of ps, is simply described as the variation in when the rising edge of a periodic signal occurs. Total jitter includes contributions from the external clock and the ADC's internal sampling processes. Jitter can have a negative effect on SNR so both clock stability and bit depth must be a design priority in order to achieve a specific level of SNR performance [25].

Finally, the time required to complete the sampling process is referred to as latency [27]. This is a fixed measure that is composed of aperture delay, conversion latency, and clock to data latency. While aperture delay and clock to data latency are hardware defined constants, the conversion latency is computed based on the number of clock cycles to encode the data and therefore varies with sampling frequency [27]. As long as the sampling frequency remains fixed, the total latency will be a constant that can be measured and captured to be used as a calibration factor so the delay through the system matches the user input setting [27].

In summary, the effects of the ADC are presented in Table 4.2.

Table 4.2: ADC Effects

Delay	$D_{ADC} = latency$ (from data sheet)
Amplitude	$A_{ADC} = 1$ (assuming flat response over Analog BW)
Frequency Shift	$f_{ADC} = exp(j0)$
Noise	$P_{Lsb,ADC} = \sigma^2_{ADCniose}$

Similarly to the result for the analog receiver, there are some parameters in Table 4.2 that should be measured and some whose empirical values can be trusted. Unless digital down conversion is implemented, f_{ADC} is zero. Furthermore, if the sampled data resides well within the ADC analog bandwidth, amplitude effects, A_{ADC} should be negligible. The only exception here is if the data at the ADC input exceeds the full scale range and is clipped during sampling [20]. The latency D_{ADC} should be measured as part of the total system delay characterization, but its value is significantly more predictable than that of the receiver due to the fact that its value is highly dependent on the

clock frequency, which will be constrained to tight performance standards by the application [27]. The added noise power $P_{n,ADC}$ will likely be negligible compared to the thermal noise associated with the incoming signal but should be computed regardless.

4.1.3 Reconstruction

After the DSP operations have been performed, the data will be converted to an analog signal by the target generator DAC. Just as with the ADC, the DAC output spectrum is segmented into Nyquist zones in which the signal at the DAC input is folded over and replicated at a spacing of every $\frac{f_s}{2}$ Hz. The zero order hold function of the DAC imposes a sin(x)/x shape on the output spectrum that dictates the attenuation of the higher frequency aliases of the signal of interest.

Quantization effects also define the output SNR of an ideal DAC following the equations described in Section 4.1.2. Recall the quantization effects from the sampling process have propagated through the DSP and possibly have accumulated due to the finite precision operations executed inside the target generator. Regardless of its bit depth, the DAC can only maintain or further degrade the SNR, not improve it. Furthermore, just like the ADC, the output spectrum is potentially characterized by harmonics and inter-modulation products, the power of which are indicated by SFDR. [26].

A summary of the effects of the DAC are shown in Table 4.3. These values are be computed with the same methods as were used for the ADC.

Table 4.3: DAC Effects

Delay	$D_{DAC} = latency$ (from data sheet)
Amplitude	$A_{DAC} = 1$ (assuming flat response over Analog BW)
Frequency Shift	$f_{DAC} = exp(j0)$
Noise	$P_{Lsb,DAC} = \sigma^2_{DACniose}$

4.1.4 Analog Transmitter

After reconstruction, the analog transmitter section completes the process of translating the data to the correct power and frequency for the radar receiver. The major steps include filtering out the aliases from the DAC output spectrum, up converting to the radar's operating frequency, and adding attenuation to simulate the R^4 losses. Assuming those steps have been sufficiently explained in previous sections, the main focus here is how to set the target generator output power level appropriately via the attenuator setting.

The target generator needs to be able to exercise the receiver's entire dynamic range. Therefore, the maximum signal power out of the transmitter has to correspond to a signal that meets the full scale range of the ADC in the radar receiver. The full scale range level is associated with the minimum attenuation setting A_{min}. The maximum attenuation, A_{max} setting must be appropriate to simulate the MDS as defined in Section 2.2.2. The attenuation setting, A, can be computed using the equations in Section 4.1.2, and inserted into the inequality in Equation 4.4. In this equation, G_{rx}, P_{MDS}, and P_{FsDAC} are all associated with the radar's receiver, while P_{inAtt} is the attenuator input power.

$$A_{min} = \frac{P_{FsDAC}}{G_{rx}P_{inAtt}} < A < \frac{P_{MDS}}{G_{rx}P_{inAtt}} = A_{max} \tag{4.4}$$

The distortion contributed by the Analog Transmitter Table 4.4 where G_{tx} includes the attenuator setting.

Table 4.4: Analog Transmitter Effects

Delay	D_{tx} (measured)
Amplitude	$A_{tx} = G_{tx}H_{tx}$
Frequency Shift	$f_{tx} = f_{RF} - f_{IF}$
Noise	$P_{n,tx} = kB_{IF}G_{tx}(T_{in,tx} + T_{e,tx})$

Similarly to the analog receiver, the values for delay through the transmitter D_{rx}, and imperfections in amplitude due to passband limitations $H_{tx}(f)$, are parameters that are best measured after the transmitter has been constructed. In the case of the transmitter, G_{tx} is actually variable due to

the bank of switched attenuators. This will yield a wildly varying value for the total amplitude change A_{tx} over the course of the target emulation and also a varying noise power as well. The noise contribution will also be variable due to the changing equivalent noise temperature $T_{e,tx}$ due to the varying attenuation.

4.2 Digital Kernel Effects

The previous section highlighted architecture-independent design considerations. The following presents the effects of various design elements that play an optional role in the target generator firmware architecture.

4.2.1 Memory Delay Elements

Regardless of the architecture, if the goal is to simulate a programmable delay, incoming data samples must be stored in memory. To enable the architectures discussed in Chapter 3, synchronous and simultaneous read and write operations must be executed on a block of dual port RAM (DPRAM).

The effective delay setting for the memory pointer spacing described in Section 3.2.1 is equal to the user input after the fixed latency of the design has been taken into account. This latency includes a host of factors such as the delay through the analog front end, $D_{rx} + D_{tx}$, the delay through the sampling and reconstruction processes, $D_{ADC} + D_{DAC}$ the delay through any DSP algorithms that may execute as part of the architecture D_{DSP}, and finally, the delay associated with the memory read and write processes, D_{MEM}. These latencies, so long as their sum does not exceed the minimum delay requirement for the application, are inconsequential to the design. They are constants and should be measured and used as factors to adjust the setting for the memory pointer spacing Δ_{ptr} so that the output signal is delayed by the amount desired by the user.

In general, the memory implementations associated with the lowest total latency are those that are available as part of the FPGA fabric like a block RAM (BRAM) because no external routing

is required for data transfer [44]. The FPGA architecture has memory cells distributed across its fabric that can be coordinated to work as a block of RAM. These can be thought of as static memories, and they are clock-synchronous and dual-port capable [44]. The limiting factor of FPGA-based memory is space, because the memory cells are also used as registers for storage of variables during algorithm execution. When the entire HDL design is taken into account, there may not be enough potential memory addresses to simulate the maximum delay of interest though this is unlikely with a high performance FPGA [42]. As higher sampling rates require more memory to represent the same target, the worst case scenario from a memory resources standpoint would be a system designed to interface with a large-bandwidth radar detecting far away targets. These constraints compound in a multi target case that would require multiple memory banks in parallel.

If more memory is required, a wide variety of dedicated off-chip solutions exist. The most appropriate off-chip memory option for this application is Quad Data Rate (QDR) RAM, an implementation that can make memory accesses on the rising and falling edges of two input clocks that are 90^o out of phase (at four times during a sampling interval) [12]. QDR is implemented as a Static RAM (SRAM), meaning the entire memory contents are accessible to the user with a constant access latency. This is in contrast to Dynamic RAM (DRAM) that employs a complex paging structure that yields higher average efficiency for random memory accesses in large memories but does not have a constant latency by design [6]. DRAM would offer no improvement to the deterministic nature of memory accesses in the target simulator application and would likely result in increased latency [6]. Another positive attribute of QDR is that it is implemented with separate input and output (SIO) ports [12]. SIO facilitates truly synchronous read and write operations, while common input output (CIO) implementations share one memory access port between read and write, effectively halving the number of operations that can happen during a clock cycle.

Once the memory has been chosen, the delay through the memory device can be computed as shown in Equation 4.5.

$$D_{MEM} = \Delta_{addr} t_d + t_d(n_{wr}) + t_d(n_{rd}) + v_p(l_{twr}) + v_p(l_{trd}) + ts_{mem} + ts_{FPGA} \tag{4.5}$$

In this equation, n_{wr} and n_{rd} are the number of clock cycles required for read and write operations required respectively, v_p is the velocity of propagation of data on a signal trace, l_{twr} and l_{trd} are the length of the read and write traces, ts_{mem} and ts_{FPGA} are the data set up times for the input pins on the memory chip and FPGA. Note that if the memory is implemented as an FPGA BRAM, the last four terms would equal zero.

Table 4.5 summarizes the effects of the memory subsystem.

Table 4.5: Memory Effects

Delay	D_{MEM}
Amplitude	$A_{MEM} = 1$
Frequency Shift	$f_{MEM} = exp(j0)$
Noise	$n_{MEM} = 0$

The only attribute of the data that is affected by the memory is the delay. This delay setting can be computed with a high level of fidelity in the case of an on-chip memory, but should be measured in the case of off-chip memory. No attenuation, additive noise, or frequency shift is contributed by the memory operation.

4.2.2 Digital Filters

The magnitude and phase response of a filter can be used to completely analyze the way a filter will impart amplitude and phase distortion onto an input signal. A plot of the forward transmission coefficient (S21) illustrates how much attenuation will be applied across the spectrum [29]. The pass band is easily identified as the region of spectrum for which the attenuation is typically less than 3dB (ignoring ripple), while the transition region is the spectrum over which the attenuation increases dramatically until it reaches its stopband level. Ideally, filters are designed so that the pass band is wide enough that the signal of interest fits well within the 3 dB bandwidth. Therefore, the only source of amplitude distortion should be the pass band ripple [35] [20].

Conversely, sufficient attenuation of unwanted signals is only guaranteed if the signals lie within the stopband, as opposed to in the transition region. Signal bandwidths that border on

the Nyquist zone boundaries set by the sample rates can make sufficient rejection hard to achieve in the case of alias rejection filters for example [20].

Next, the delay through the filter, or group delay $D_{G,FIR}$, is a crucial design parameter in this application and is calculated as shown in Equation 4.6 [20].

$$D_{G,FIR} = \frac{-\Delta\phi}{\Delta f} \tag{4.6}$$

Equation 4.6 shows that the group delay is equal to the derivative of the phase with respect to frequency. For all frequencies to pass through the filter with the same delay, the filter's phase response must be linear [20] [29].

While amplitude distortion, if severe enough, could be corrected, phase distortion is a much more complicated phenomena to unravel. Because relative phase has such a key implication to radar measurement performance, only Finite Impulse Response (FIR) filters are applied in the digital kernel. Unlike Infinite Impulse Response (IIR) filters, FIR filters are guaranteed to have a linear phase response when designed with symmetric coefficients [21].

Assuming the filter phase response is linear, the group delay can also be quickly calculated with Equation 4.7, in which S is the number of coefficients.

$$D_{G,FIR} = \frac{(S-1)}{2f_{clk}} \tag{4.7}$$

The coefficients of digital filters must be truncated relative to their ideal values to feasibly be implemented in an FPGA. FIR filters are typically more robust than IIR to truncation effects [35]. Applying the techniques thoroughly documented in [35], truncation of coefficients can yield negligible effects in FIR filters. A summary of the filter effects is provided in Table 4.6.

Table 4.6: FIR Effects

Delay	$D_{G,FIR}$
Amplitude	$A_{FIR}(f) = H_{FIR}(f)$
Frequency Shift	$f_{FIR} = exp(j0)$
Noise	negligible

The delay through a digital filter $D_{G,FIR}$ will be accurately predicted by 4.7. The amplitude effect is frequency dependent and defined by the filter transfer function $H_{FIR}(f)$. The noise added by digital filters is an effect of quantization and truncation of filter coefficients and output data. As the available precision of these operations meets or exceeds the precision in the ADC and DAC, these effects are negligible.

4.2.3 Direct Digital Synthesis

The Direct Digital Synthesizer (DDS) serves as a LO source for the SSB modulator in this application. Its specific contribution to system performance is related to frequency stability and clarity. A DDS is specifically appropriate for this application due to the perfect amplitude and phase match between quadrature channels [2].

A DDS is composed of a phase accumulator and a sine wave amplitude stored in a look up table (LUT). The basic DDS architecture is shown in Figure 4.1 [9].

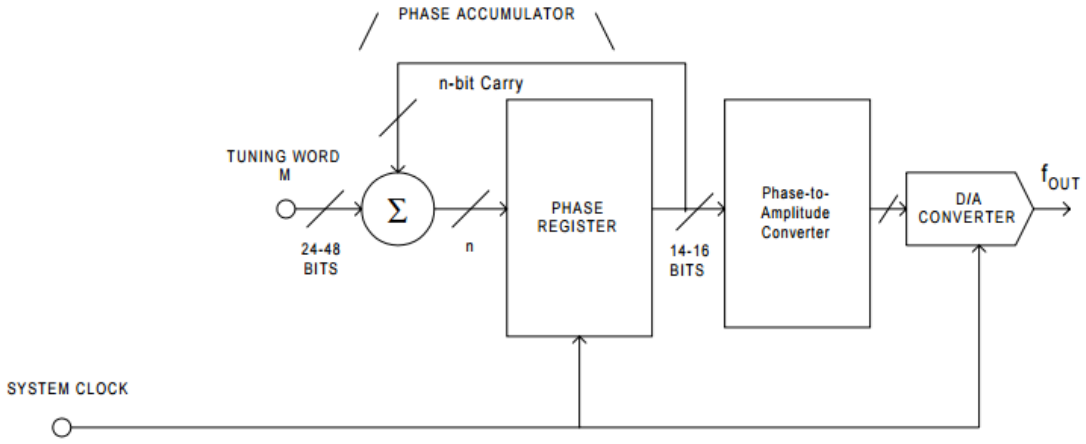

Figure 4.1: Frequency-tunable DDS System, reproduced from [9].

The output frequency of the DDS is changed by selecting a different tuning word W_{FC}, or increment step size input to the phase accumulator. The value of W_{FC} determines the rate at which the system steps through the LUT addresses. The output frequency, f_{DDS} is related to the clock rate for the accumulation process f_{clk}, the tuning word W_{FC}, and the number of bits in the phase

accumulator N as is shown in Equation 4.8.

$$f_{DDS} = \frac{W_{FC} f_{clk}}{2^N} \tag{4.8}$$

As is depicted after the Phase Register block in Figure 4.1, it is common practice to truncate the phase accumulator output to limit the memory length. This truncation causes spurs in the output spectrum as thoroughly described in [33]. A thoughtful DDS design will implement one of a variety of techniques such as dithering the output to reduce the amplitude of these output spurs and improve the SFDR of the DDS [33].

The SNR of the DDS output spectrum due to quantization of the sine wave amplitude values stored in memory [33] follows Equation 4.1. Quantization effects are the dominant source of noise in the DDS output spectrum. Often noise shaping techniques, oversampling, and $\Sigma\Delta$ Modulators are implemented to shift the noise power out to higher frequencies [33].

The significant impact of the DDS output, however, has to do with the achievable frequency resolution. The finer the resolution, the more likely the correct frequency can be generated without introducing rounding errors. The worst case offset of the DDS output frequency is $\frac{f_{res}}{2}$, or half of the resolution away from the desired frequency. Equation 4.8 can be used to compute the frequency resolution f_{res} of the DDS if W_{FC} is set equal to 1. Based on the user's setting, f_{set}, the true DDS output can be computed in Equation 4.9.

$$f_{DDS} = \left\lceil \frac{f_{set}}{f_{res}} \right\rceil f_{res} \tag{4.9}$$

DDS can also be used to produce outputs that are perfectly phase offset. This is of particular use IQ sampling [20], or SSB modulation [10] [2] applications in which two LO signals with a relative phase shift of 90^o between them are required. While analog IQ generation is highly susceptible to channel imbalance [20], DDS implementations can generate perfectly phase synchronized and amplitude matched quadrature channels.

The DDS effects can only be considered in this application as part of the SSB modulator. In

this case the DDS effects are shown in Table 4.7 along with those of the Hilbert Transformer, multiplier and adder from the Doppler control subsection of Figure 3.6.

Table 4.7: SSB Modulator Effects

Delay	$D_{DSP} = D_{G,FIR} + D_{MULT} + D_{ADD}$
Amplitude	$A_{DSP} = 1$
Frequency Shift	$f_{DSP} = f_{DDS}$
Noise	negligible

Note that no attenuation is expected with this implementation of a DDS. Assuming the amplitude and phase are perfectly matched between the I and Q channels, the undesired sideband will be perfectly canceled. No delay is specifically due to the DDS itself, but the multiplication, addition, and filtering operations in the the SSB modulator will cause latency that can be summed to yield the total delay due to the SSB modulator, D_{DSP}.

4.3 Device Equations with Non-ideal Effects Included

Finally, the device equations in Chapter 3 will be updated with the information described in the previous sections. These equations are summarized in Table 4.8.

The total delay, D_T is computed as shown in Equation 4.10.

$$D_T(t) = D_{rx} + D_{ADC} + D_{MEM}(t) + D_{DSP} + D_{DAC} + D_{tx} \tag{4.10}$$

Table 4.8: Target Generator Device Equations with Non-Ideal Effects

Architecture	**Target Type**	**Chapter 3 Reference**
Mem Only	Static	Eq. 3.7
$\mathbf{y}_{bm}(t) = h_{rx}(t)G_{rx}h_{tx}(t)G_{tx}a(t-D_T)e^{-j(2\pi f_{IF}D_T)} + w(t)$		
Mem Only	Moving	Eq. 3.10
$\mathbf{y}_{bm}(t) = h_{rx}(t)G_{rx}h_{tx}(t)G_{tx}a(t-D_T(t))e^{-j(2\pi f_{IF}D_T(t))} + w(t)$		
Mem and SSB	Moving	Eq. 3.12
$\mathbf{y}_{bm}(t) = h_{rx}(t)G_{rx}h_{tx}(t)G_{tx}a(t-D_T(t))e^{-j(2\pi f_{IF}D_T(t))}e^{j(2\pi(f_{DDS}))t)} + w(t)$		

In summary, the most significant inevitable non-ideal effect is the total delay due to propagation

delay through the hardware and firmware latencies. The remaining features of amplitude distortion, additive noise, and frequency shift should be made manageable with careful design and must be verified before the target generator is used for testing.

The results in Table 4.8 can be used to account for all of the non-ideal effects inherent to the implementation of the target generator. The features of the design that have been noted throughout this chapter are potential sources of error if they are not applied as a correction factor to the device settings before running a test. Thorough assessment of the design is paramount to accuracy of the simulated target qualities and the capability of the target generator to serve as an part of an effective testbed for a particular radar design.

Chapter 5

Detailed Design and Analysis

While the previous sections developed the theoretical framework within which the designs in Section 3.2 and their outputs will be characterized, this chapter's focus is to explicitly define the hardware and firmware algorithm. As a result, this chapter builds upon the constraints discussed in Chapter 3 and the architecture specific equations of Chapter 4 to yield a complete description of the final design that will be simulated and analyzed in Chapter 6. This chapter covers the sampling and signal processing circuitry, the RF conversion circuitry in both the target generator and the radar, and the specifics of the firmware algorithms implemented in the FPGA.

The digital kernel was designed with the following assumptions. First, the kernel is to serve as the core of a test system designed for interface with a complete radar system. As such, the target generator is only connected to the radar via the transmitter and receiver ports. The algorithm therefore has no explicit knowledge of the radar's operating parameters; only the nominal operating conditions as provided by the user. While circuits could be implemented to attempt real-time measurements of the radar's operating parameters, none are included in this design. The algorithm operates asynchronously of the radar. No attempt is made in this target simulator implementation to measure or synchronize with any aspect of the radar design.

5.1 Hardware Platform

This design was targeted for use with the Xilinx KC705 development board and a 4DSP FMC150 sampling card. The 4DSP card has two ADC channels and two DAC channels that are synchronized with an on-board clock source. The ADC, DAC, and clock data are routed to and from the Kintex-7 FPGA through a high density FMC connector installed on the KC705 board. The development board also supports peripheral connections that could be used to transfer data to and from a host PC.

A list of the significant components of the sampling subsystem is shown in Table 5.1 followed by a high level block diagram of the connections between these components in Figure 5.1.

Table 5.1: KC705 and FMC150 Bill of Significant Materials

Ref. Des.	Description	Part Number	Host Board
U1	Clock Distributor and Synchronizer	CDCE72010	FMC150
U2	Analog to Digital Converter, 12-bit	ADS62P29	FMC150
U3	Digital to Analog Converter, 16-bit	DAC3283	FMC150
U10	Kintex-7 FPGA	XC7K325T-1FFG900C	KC705

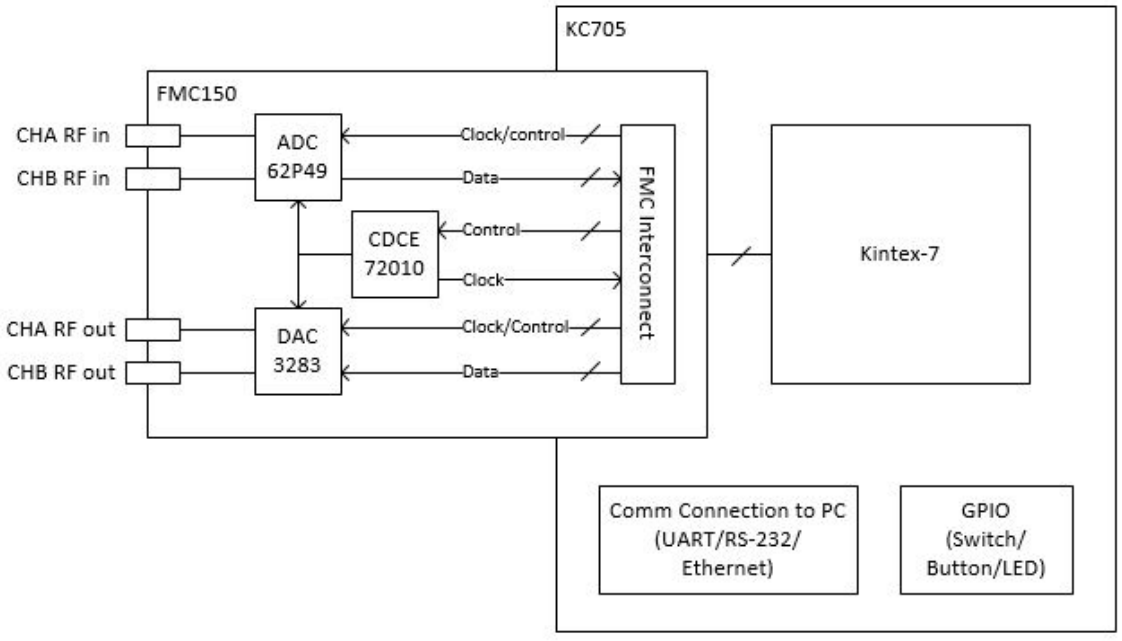

Figure 5.1: KC705 and FMC150 High Level Block Diagram

For this work, only one channel of the FMC150 card is used in an IF sampling configuration.

The sampling rate of the ADC and DAC are programmable via the clock chip. Xilinx provides a VHDL reference firmware design for this hardware set that handles the configuration of the ADC, DAC, and clock chip in addition to managing the data handshake process for transfer to and from the user-defined algorithm. This design streamlines the use of the hardware components, making their configuration transparent to the user and will not be discussed further.

The Kintex-7 FPGA specifications are listed in Table 5.2. These values represent theoretical maximums and will likely be reduced by constraints imposed by the firmware implementation.

Table 5.2: Relevant Kintex-7 Specifications [48] [42]

Parameter	**Value**	**Units**
Speed Grade	1	
Max Clock Speed	800	MHz
DSP Slices	840	
Logic Cells	325,000	
BRAM	28	Mb

The selection of hardware defines the system data rate and signal levels at the input and output of the FMC150 card. Key performance metrics of the hardware are listed in Table 5.3 along with a reference to which aspect of the rest of the design is constrained by each parameter [47] [1].

Table 5.3: KC705 and FMC150 Operating Limits

Variable	**Parameter**	**Limit**	**Units**	**Constraint**
f_s	ADC Max Sampling Frequency	245.75	MHz	Algorithm Delay Resolution
f_{aADC}	ADC Analog Bandwidth	700	MHz	Analog Circuit IF
V_{ppin}	ADC Max Input Voltage	2	Vpp	Analog Circuit Gain
P_{inADC}	ADC Max Input Power	10	dBm	Analog Circuit Gain
q_{ADC}	ADC LSB Voltage	141	μVrms	Analog Circuit Noise Temp
N_{ADC}	ADC Quant. Noise Spec. Density	-144	dBm/Hz	Analog Circuit Noise Temp
D_{ADC}	ADC Latency	22	clocks	Total System Latency
f_{aDAC}	DAC Analog Bandwidth	800	MHz	Analog Circuit IF
V_{ppout}	DAC Max Output Voltage	1	Vpp	Analog Circuit Gain
P_{outDAC}	DAC Max Output Power	4	dBm	Analog Circuit Gain
q_{DAC}	DAC LSB Voltage	4	μVrms	Analog Circuit Noise Temp
N_{DAC}	DAC Quant. Noise Spec. Density	-174	dBm/Hz	Analog Circuit Noise Temp
D_{DAC}	DAC Latency	59	clocks	Total System Latency
f_{IF}	IF Sampling Frequency	60	MHZ	ADC Sampling Freq

Next, the power levels at the input and output of the radar will be specified to complete the definition of the system constraints in Section 5.2. Section 5.3 then proceeds with the specification and analysis of a representative RF front end that is suitable for interface between the radar and sampling circuitry above.

5.2 Radar Signal Level Definition

There are six signal level constraint points to be considered in the high level transmit and receive chains shown in Figure 5.2. In the transmit chain (Points 1 - 3), the interfaces are at the radar DAC output, the radar transmitter to target generator receiver interface, and the target generator ADC. In the receiver chain (Points 4 - 6), the constraint points consist of the target generator DAC output, the target generator transmitter to radar receiver interface, and the radar ADC input. Section 5.1 established the boundary conditions associated with the ADC and DAC within the target generator (points 3 and 4 in Figure 5.2). The following will define constraints on the remaining four boundaries; a summary of which are presented in Table 5.4.

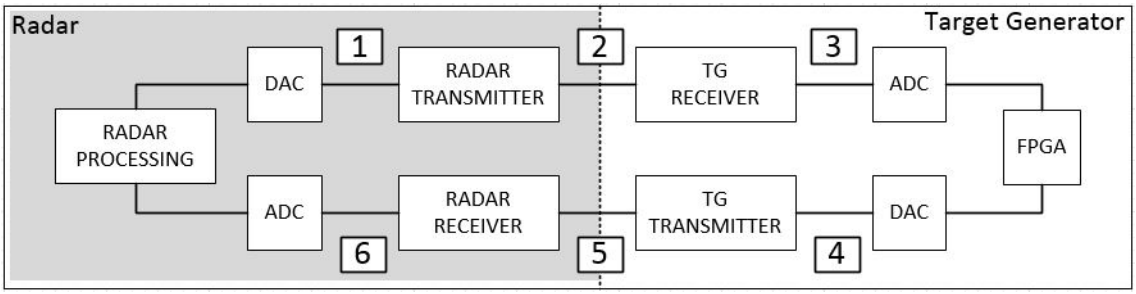

Figure 5.2: Complete System High Level Block Diagram

The hypothetical radar design is specified with a 12-bit DAC and ADC each with a full scale range of 1 Vpp and IF bandwidth of 245.76 MHz. This selection defines the values for the minimum and maximum total received power at the radar ADC as was discussed in Chapter 4 in addition to the input noise temperature for the system. The values in Table 5.4 are explicitly computed in Appendix A.

The signal levels at the interface between the radar and the target generator are set by the radar's

Table 5.4: Radar Signal Conditioning Parameters

Variable	Parameter	Limit	Units
P_{outTx}	Radar Transmit Power	40 10	dBm W
$P_{outRDAC} = P_{inRADC}$	Radar DAC and ADC Power In/Out	4 1	dBm Vpp
$FS_{RDAC} = FS_{RADC}$	Radar DAC and ADC full scale range	0.354	Vrms
$N_{RADC} = N_{RDAC}$	Radar DAC and ADC number of bits	12	
B_{IF}	Radar IF Bandwidth	100	MHz
$q_{DAC} = q_{ADC}$	Radar DAC and ADC Quantization Noise Voltage	70	μVrms
$P_{n,DAC} = P_{n,ADC}$	Radar DAC and ADC Quantization Noise Power	-70	dBm

operating mission. In this case, the radar's transmit power is arbitrarily chosen to be 10 W. The signal levels at the input to the receiver can then be computed using the radar range equation in Equation 2.1 after the target ranges of interest are selected in Chapter 5.

5.3 Hypothetical RF Front End

Now that the signal level and bandwidth constraints on the system have been established, the analog portion of the radar design and the target generator's down and up conversion circuits can be developed.

The analog conversion circuits that would be needed to translate the RF radar data to the IF for sampling are not physically implemented as part of this research, yet the effects of a representative design will be included in the simulation. This model of the RF front end circuitry facilitates a simulation of the system performance in a representative testing environment. The complete analog system is depicted in Figure 5.3 and is effectively a combination of the diagrams in Figures 2.2 and 3.3.

A simple single-stage conversion circuit is assumed to be sufficient in both the radar and target generator. As was mentioned in Chapter 4, the system is assumed to have been designed so that perfect rejection of spurious mixing products has been achieved.

The key operating parameters of the analog components — noise figure, bandwidth, and gain

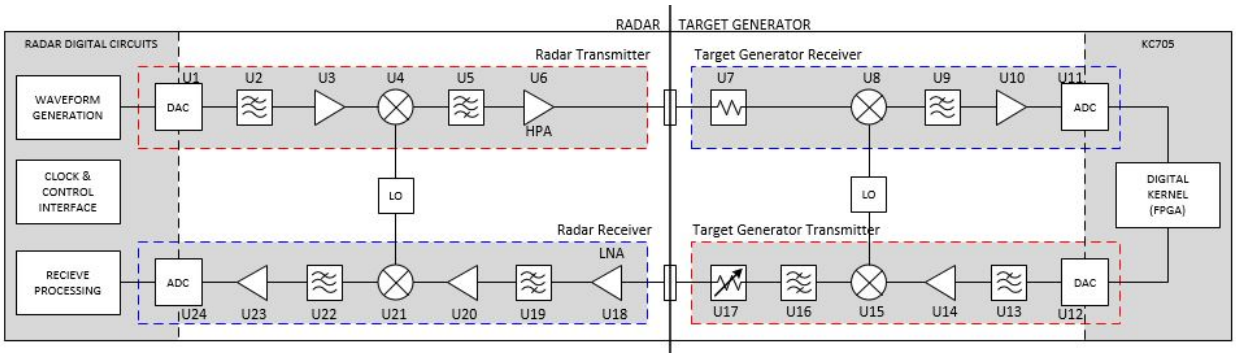

Figure 5.3: Complete Diagram

— were selected to be representative of an ideal design made with realistic components. For example, an amplifier like U14 with 21 dB of gain and a noise figure of 5 dB may not exist to be purchased at present, but its features suit this application and are realizable with current technology. A summary of the significant attributes of the analog components in the radar and target generator is provided in Table A.2 along with a detailed block diagram of the components and their corresponding signal levels in Figure A.2. These are both located in Appendix A.

An aspect of the architecture that is not ignored in this research is the effect of the additive noise associated with the target generator. The thermal noise level associated with the signal at the radar ADC must match the level that would be expected if the radar were making free space measurements to avoid presenting an unrealistic environment during the test. This difference in noise level is important because as was discussed in Chapter 4, the radar processing is designed to overcome a specific minimum SNR at the receiver input.

Because the radar is directly connected to the target generator, the typical computation of the noise incident on the radar processing using $P_n = kTBF$ is not sufficient. Detailed noise figure and noise power calculations are presented in Appendix A and a summary of these results is shown below in Table 5.5. These noise-related parameters will be used in the system simulation discussed in Chapter 6. For purposes of this table, the theoretical minimum and maximum attenuations are set at 20 dB and 200 dB.

Next, section 5.4 describes the firmware implementation in the FPGA.

Table 5.5: RF System Characteristics

Parameter	Value	Ref. Point in Fig. 5.3
TG Attenuation Values	$20 < A < 200$ dB	5
Radar Rx NF	2.69	6
Radar Tx Output Noise Temp.	$307x10^6$ K	2
Target Gen. Rx Output Noise Temp.	$307x10^3$ K	3
Target Gen. Tx Output Noise Temp.	$1244 > T_{e,tgtx} > 290$ K	5
Radar Rx Output Noise Temp.	$346x10^3 > T_{e,rx} > 156x10^3$ K	6
SNR out of Radar Tx	73.7 dB	2
SNR out of Target Gen. Tx	$69.6 > SNR_{in,rx} > -104.4$ dB	5
SNR into Radar ADC, Free Space	$72.0 > SNR_{in,ADC} > -108.3$ dB	6
SNR into Radar ADC	$68.2 > SNR_{in,ADC} > -108.3$ dB	6

5.4 Target Generator Algorithm Description

The target generator firmware algorithm was developed and tested in the design environments provided by Xilinx' Vivado and Matlab's Simulink. While the Xilinx platform provides detailed analysis of the synthesized design including timing analysis and FPGA resource utilization, Simulink's design environment is more suited for DSP development and has access to the superior analytical capabilities of Matlab. Simulink's compatibility with Xilinx-defined blocks facilitated the import and export of user algorithms between the two environments so that the design features could be vetted with the tools provided by each design suite.

5.4.1 Top Level

A high level block diagram of the architecture considered in the following was presented in Figure 3.6. The top level hardware description language (HDL) implementation of that diagram is shown in Figure 5.4 and is capable of vetting each type of target simulator style described in Section 3.2. Note the dashed lines which indicate the major subsystems as they were marked in Figure 3.6. The pin description for the top level design is shown in Table 5.6.

The algorithm has three operating modes that are selectable via the multiplexer control signals, **bypass** and **ssb_ena**. The first mode is a path that bypasses the algorithms and sets the output data equal to the input data with no added delay. This feature is particularly useful for characterizing

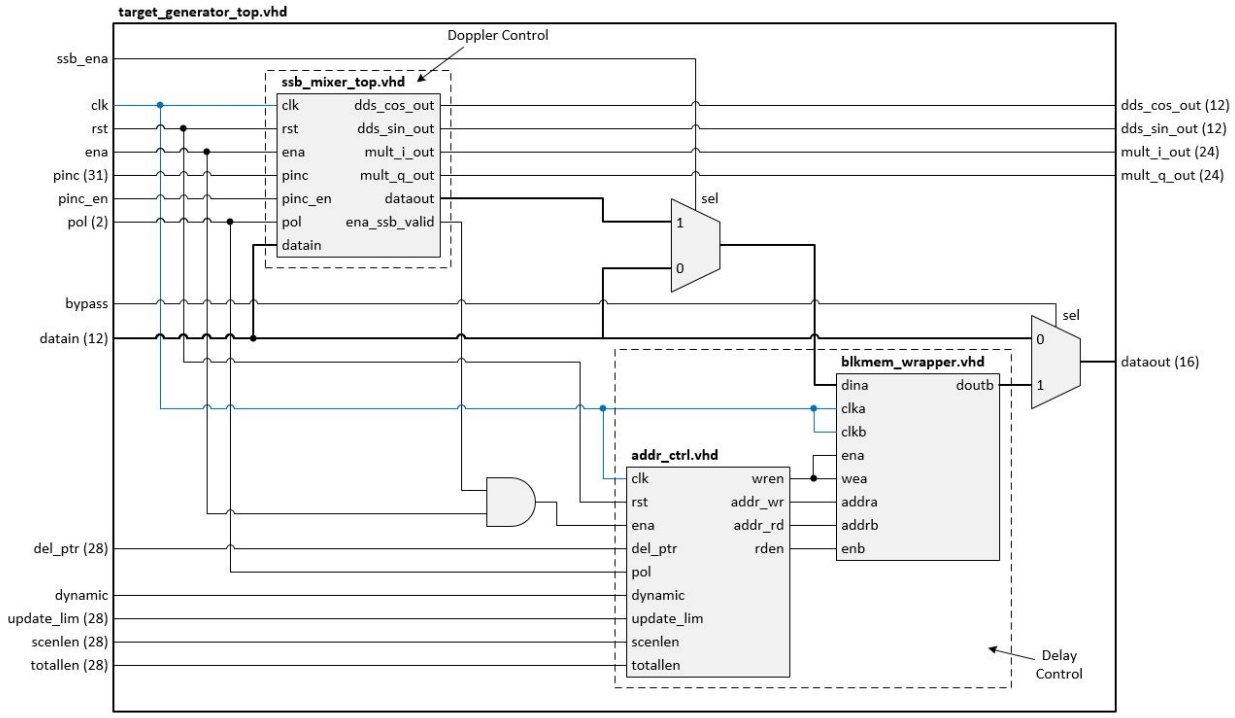

Figure 5.4: Top Level Target Generator Algorithm

Table 5.6: Top Level Pin Descriptions

Pin Name	Type / Length / Port	Description
clk	std_logic / 1 / in	245.76 MHz Clock
rst	std_logic / 1 / in	User-asserted reset pin, active high
ena	std_logic / 1 / in	User-asserted enable pin, active high
bypass	std_logic / 1 / in	0 = bypass all algorithms, 1 = use memory out
ssb_ena	std_logic / 1 / in	1 = SSB Doppler shift, 0 = bypass SSB
dynamic	std_logic / 1 / in	1 = enable moving targets 0 = disable moving targets
pol	std_logic / 2 / in	00 = inbound target, 11 = outbound, 01 / 10 = stationary
pinc_en	std_logic / 2 / in	enable phase increment in DDS
pinc	std_logic / 32 / in	phase increment value for DDS
del_ptr	std_logic / 28 / in	starting pointer difference for address controller
update_lim	std_logic / 28 / in	count for memory pointer spacing update interval
scenlen	std_logic / 28 / in	duration of the simulated scenario
totallen	std_logic / 28 / in	total time duration for algorithm in clock cycles
datain	std_logic / 12 / in	input data from 12 - bit ADC
dataout	std_logic / 16 / out	output data to 16 - bit DAC

the hardware latency without the effects of the DSP. The two remaining options are to either feed the data through the Delay Control block only, or to select a path where the output goes through

both the Doppler Control and Delay Control blocks.

In either the memory only case or the memory and Doppler case, the memory address control algorithm is enabled after the user enable has been asserted and the single sideband mixer output has stabilized. This is realized by performing an "AND" operation between the external **ena** signal and the internally generated **ena_ssb_valid** signal as shown in Figure 5.4.

5.4.2 Delay Control

The three VHDL blocks in Figure 5.4 are composed of additional logic. First, the blkmem_wrapper.vhd file is a wrapper around a Xilinx IP core for BRAM implementation. This memory is configured as a Simple DPRAM. For the purpose of this simulation, the memory depth is set to be 16384. Because the sampling rate rate has been set per Table 5.3, the longest delay that can be simulated with this design is 66.5 μs according to Equation 3.5. This delay is associated with a target at a range of 10 km per Equation 3.6. The remaining settings for the BRAM were left as the Xilinx defaults [44]. A summary of the significant features of the memory block appears in Table 5.7.

Table 5.7: Block Memory Configuration [44]

Attribute	**Value**
Depth	16384
Read Port Latency	2 clock cycles
Resource Usage	**Value**
DSP48 Slices	0
LUT Count	173
Max f_{clk} on Kintex-7	400 MHz

The detail included in the address controller is shown in Figure 5.5. The algorithm is primarily composed of four counters that indicate that the count limit has been reached by driving their **wrap** output high. The **update_count**, **write_addr_count**, and **read_addr_count** modules are designed to assert their **wrap** outputs for one clock cycle and then reset the count and start over, while the **process_count** module latches its **wrap** outputs high until receiving a reset command from the top level module.

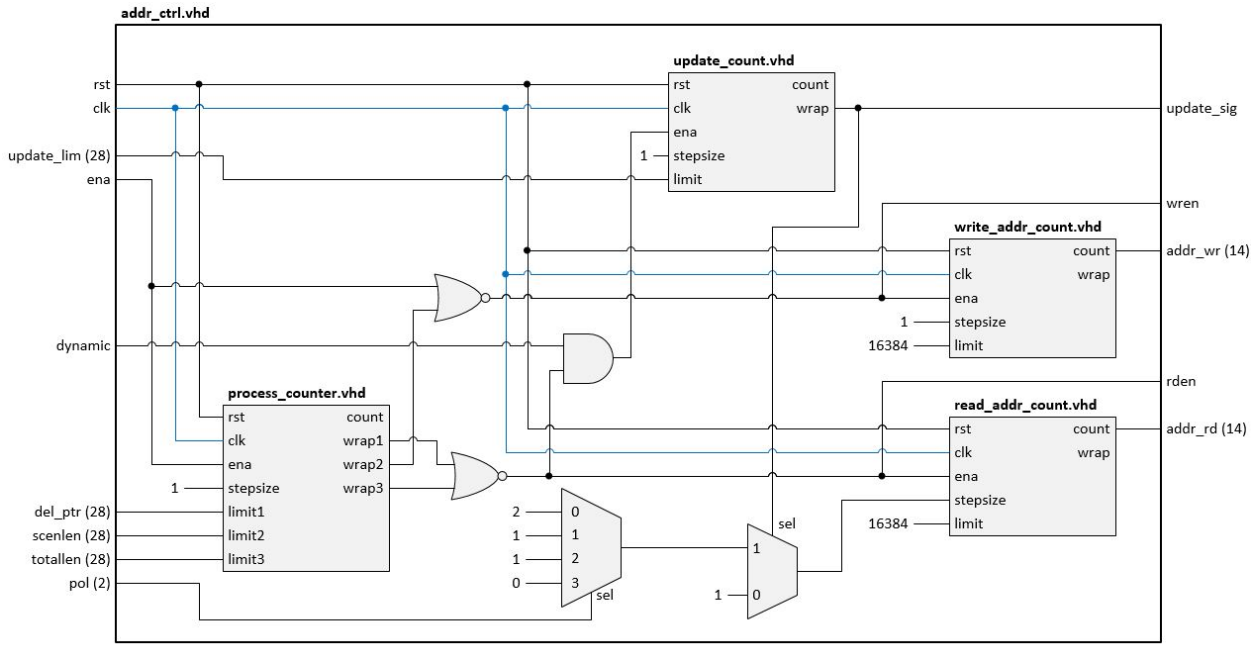

Figure 5.5: Detail of Address Control Block

Note from Figure 5.5 that the **wrap** outputs of the **process_counter** pass through an "XOR" gate to yield the **wren** and **rden** signals that are used to start the address count processes and to enable read and write operations in the block memory. The write process stores incoming data samples starting from when the user enables the algorithm and stops when the scenario length has been reached. The read process is enabled when the desired pointer spacing has been reached and is disabled when the total algorithm length (**del_ptr** + **scenlen** in this case) has been reached. A user-asserted reset is required to restart the algorithm.

In the case of a moving target, the "AND" of the **rden** line with the **dynamic** input equals b'1', thereby enabling the **update_count** module. This module drives its **wrap** output high at the update rate frequency defined in Equation 3.8. When this wrap signal is driven high, the **stepsize** input to the read process changes from its default value of b'1' to the value selected by the **pol** signal as shown in Figure 5.5.

A summary of the input and output ports of the address controller is provided in Table 5.8.

Table 5.8: Address Controller Pin Descriptions

Pin Name	Type / Length / Port	Description
clk	std_logic / 1 / in	245.76 MHz Clock
rst	std_logic / 1 / in	User-asserted reset pin, active high
ena	std_logic / 1 / in	User-asserted enable pin, active high
dynamic	std_logic / 1 / in	1 = enable moving targets 0 = disable moving targets
pol	std_logic / 2 / in	00 = inbound; 11 = outbound; 01 / 10 = stationary
del_ptr	std_logic / 28 / in	starting pointer difference for address controller
update_lim	std_logic / 28 / in	count for memory pointer spacing update interval
scenlen	std_logic / 28 / in	duration of the simulated scenario
totallen	std_logic / 28 / in	total time duration for algorithm in clock cycles
update_sig	std_logic / 1 / out	high if memory pointer spacing change occurred
wren	std_logic / 1 / out	write enable to block memory and write addr counter
rden	std_logic / 1 / out	read enable to block memory and read addr counter
addr_wr	std_logic / 14 / out	write address
addr_rd	std_logic / 14 / out	read address

5.4.3 Doppler Control

Next, the details of the SSB mixer HDL implementation are provided in the diagram in Figure 5.6 and a description of the input and output pins appears in Table 5.9.

Table 5.9: SSB Modulator Pin Descriptions

Pin Name	Type / Length / Port	Description
clk	std_logic / 1 / in	245.76 MHz Clock
rst	std_logic / 1 / in	User-asserted reset pin, active high
ena	std_logic / 1 / in	User-asserted enable pin, active high
pol	std_logic / 2 / in	00 = inbound; 11 = outbound; 01 / 10 = stationary
pinc_en	std_logic / 2 / in	enable phase increment in DDS
pinc	std_logic / 32 / in	phase increment value for DDS
datain	std_logic / 12 / in	input data from 12 - bit ADC
dataout	std_logic / 16 / out	output data to 16 - bit DAC

As is shown in Figure 5.6, the input data to the SSB modulator is first passed through an FIR filter implemented as a Hilbert Transformer that was described in Section 3.2.2. The Xilinx implementation of the filter has two output data streams, one that is in-phase with the input data and one that lags the phase of the input data by 90°. The true filtered output is the quadrature output, while the in-phase output is simply a copy of the input data that has been delayed by a

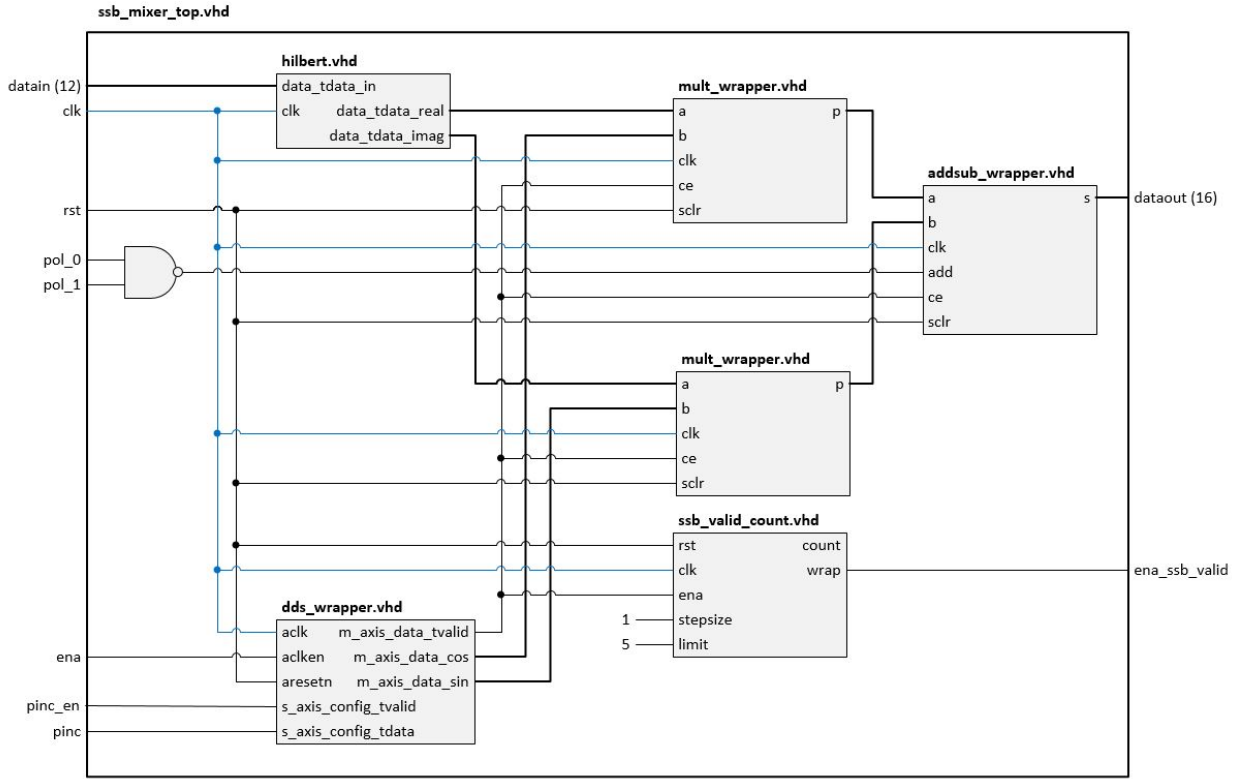

Figure 5.6: Detail of SSB Mixer

number of clock cycles equal to the group delay through the filter.

The in-phase filter output is multiplied by a cosine signal generated by the DDS while the quadrature output is multiplied by a sine wave oscillating at the same frequency. The DDS output frequency is selected by the phase increment value stored in the **pinc** input. This phase increment is equal to the tuning word, W_{FC} in Equation 4.8. The DDS output takes time to stabilize after receiving the **ena** signal. The **ssb_valid_count** module is used to output a latched high signal, **ena_ssb_valid**, after the output has stabilized to initiate the algorithm.

The **pol** input is used to select whether the output of the multipliers will be added or subtracted. In the case of an inbound target, the multiplier outputs are summed to produce a positive Doppler shift via rejecting the lower sideband. The outputs are subtracted to suppress the upper sideband and yield a negative Doppler shift. The output of the addition/subtraction block is the delayed and Doppler shifted data for transmit back to the radar.

All of the remaining blocks in this section are user-configured Xilinx IP. Their configuration

and associated latency are as follows.

First, the Hilbert Transformer implemented here is a FIR filter of order 50 as was required to achieve approximately 20 dB of rejection of the unwanted sideband as shown in Figure 5.8. The magnitude and phase response of this filter are plotted in Figure 5.7 and its configuration parameters are listed in Table 5.10.

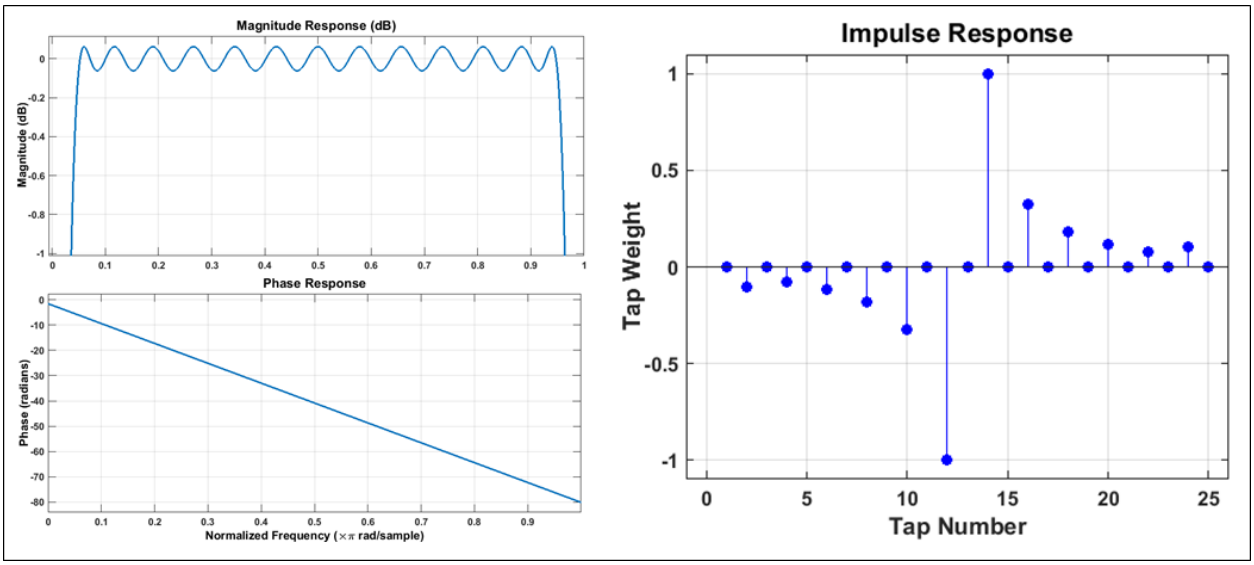

Figure 5.7: Hilbert FIR Magnitude, Phase, and Impulse Responses

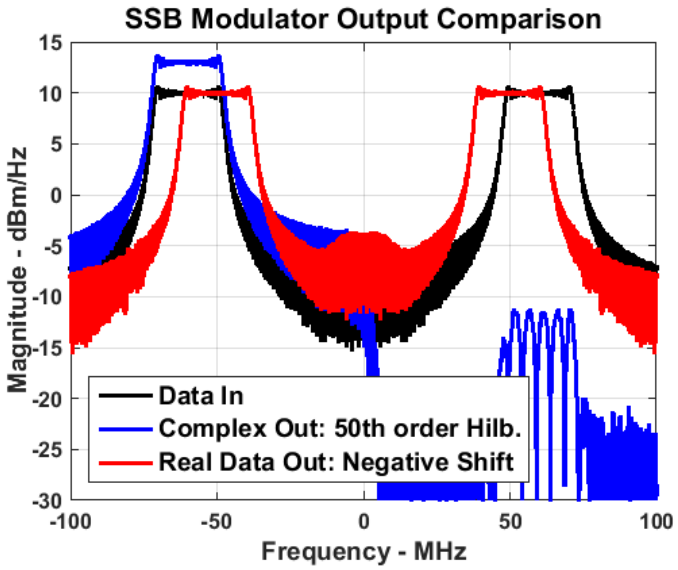

Figure 5.8: SSB Modulator Output Sideband Rejection Performance Comparison

Table 5.10: Hilbert FIR Configuration [46]

Attribute	**Value**
Output Width	16 bits
Rejection	48 dB
Flatness	+/- 1 dB
Order	50
Latency	25 clock cycles
Quantization	Quantize Only
Resource Usage	**Value**
DSP48 Slices	3
BRAM Count	1
Max Clock Kintex-7	420 MHz

As was stated in Chapter 3, the amplitude and phase match between the I and Q channels is paramount to good rejection performance of the SSB modulator. The output of the SSB modulator using a 50th order filter is shown in Figure 5.8 featuring a LFM signal that will be defined in Chapter 6. In that plot, the complex trace demonstrates the suppression of the upper via summation of the I and Q outputs of the Hilbert transform (no frequency shift was applied in that case). The suppression of the upper sideband is 25 dB. The total output of the SSB modulator with a frequency shift of -10 MHz is shown in the red trace. The 50th order Hilbert transform required to achieve sufficient sideband rejection would theoretically result in a group delay of 25 clock cycles per Equation 4.7; a result that was confirmed by the Xilinx analysis tools.

Table 5.11: DDS Configuration [45]

Attribute	**Value**
Output Width	13 bits
Noise Shaping	Taylor Series Corrected
Phase Width	32 bits
Frequency Resolution	0.1 Hz
Phase Angle Width	11 Bits
SFDR	72 bits
Latency	8 clock cycles
Resource Usage	**Value**
DSP48 Slices	3
BRAM Count	1
Max Clock Speed Kintex-7	450 MHz

Next, the DDS configuration settings are shown in Table 5.11. The 0.1 Hz resolution can be verified computationally by setting the frequency control word equal to 1 in Equation 4.8 and the number of bits equal to 32. A 32-bit phase accumulator is required to achieve 0.1 Hz resolution after which the output width is truncated to 13 bits. This truncation yields output spurs, and results in a SFDR of 72 dB according to the Xilinx analysis tools which was found to be sufficient for this application. The noise shaping algorithm is not discussed here as it is simply an option in the Xilinx implementation.

Finally, the significant parameters of the multiplication and addition/subtraction modules are described in Tables 5.12 and 5.13.

Table 5.12: Adder Config. [43]

Attribute	Value
Output Width	25 bits
Programmable	Yes
Latency	1 clock cycle
Resource Usage	**Value**
LUT Count	25
FF Count	25
Max Clock Speed Kintex-7	540 MHz

Table 5.13: Multiplier Config. [49]

Attribute	Value
Output Width	25 bits
Pipeline Stages	4
Latency	4 clock cycles
Resource Usage	**Value**
DSP48 Slices	0
LUT Count	173
Max Clock Speed Kintex-7	540 MHz

To avoid accumulation of errors due to truncation, the output of the multiplier and adder are allowed to grow to the necessary output width. The output data is reformatted to the appropriate bit width at the end of the algorithm before the DAC.

5.4.4 HDL Design Summary

In summary, the resource utilization, bandwidth constraints clock limitations, and total algorithm latency are summarized in Table 5.14. These results are the analysis of the total top level design in Section 5.4.

Table 5.14: HDL Design Summary

Attribute	Value	Units
Input Width	12	bits
Output Width	16	bits
Latency	52	clock cycles
Resource Usage	**Value**	**Percent Utilization**
LUT	190	0.09%
Flip Flop	91	0.02%
DSP48 Slices	4	0.4%
Maximum Clock Speed	400 MHz (BRAM)	80 %

Table 5.14 clearly demonstrates that this design does not approach full utilization of the FPGA's capabilities. This suggests that putting multiple copies of this architecture in parallel to facilitate multiple target simulations would be possible, and also that a more complex algorithm could be implemented. Also, because maximum clock speed for the design is almost twice the actual sam-

pling and data rate of 245.76 MHz, there is a strong likelihood that this design will function as simulated when implemented in the FPGA. Investigations into these areas are left for future work.

5.5 Target Generator Design Summary

In summary, the major target generator design parameters are presented in Table 5.15.

Table 5.15: HDL Design Summary

Variable	Units	Value	Description
$f_{s,ADC}$	MHz	245.76	ADC Sampling Rate
f_{IF}	MHz	60	IF Center Frequency
t_d	ns	4.069	Minimum Delay Step
δR	m	0.61	Minimum Range Step
R_{max}	km	10	Maximum Range
R_{min}	m	100	Minimum Range
δf_d	Hz	0.1	Doppler Shift Resolution
A_{min}	dB	20	Minimum Attenuator Setting
A_{max}	dB	200	Maximum Attenuator Setting

These parameters are superficial in the sense that they are based on hypothetical hardware. They are representative, however, of the key pieces of information that are required to determine whether the target generator design is suitable for interface with a candidate radar system for testing.

Chapter 6

Simulation Development and Results

While the target generator algorithm described in Chapter 5 can be scaled to perform simple tests on any radar system, the simulation results in this chapter are collected using a representative radar design. The numbers specified in the following are of no consequence to the effectiveness of the target generator research results. If different radar parameters were used, the equations in Chapters 3, 4, and 5 could be used to update the system performance expectations.

6.1 Simulated Radar Parameters

The radar parameters used for the base case simulation are summarized in Table 6.1. The results of the simulations using these results are presented in Section 6.3 and represent the control case for the subsequent simulations in which the radar and target parameters will be varied.

First, the minimum delay step size of the target generator is set at 4.069 ns by the target generator ADC sampling rate of 245.76 MHz. Therefore, the minimum range step size of the target generator is 0.61 m. The range resolution of the radar was selected to be ten times the minimum range step size of the target generator or 6.1 m. This choice forced the bandwidth of the radar to be equal to one tenth of the target generator sampling rate, 24.576 MHz.

Next, the CPI 0.01 s was chosen to facilitate the time-intensive simulation of the target generator firmware via Simulink. The simulation scenarios were designed such that multiple target

Table 6.1: Simulated Radar Parameters - Base Case

Variable	Units	Value	Description
B	MHz	24.576	LFM Bandwidth
ΔR	m	6.1035	LFM Range Resolution
f_{RF}	GHz	2	RF Center Frequency
τ	us	5	Pulse Duration
PRI	us	50	Pulse Repetition Interval
PRF	kHz	20	Pulse Repetition Frequency
CPI	s	0.01	Coherent Processing Interval
Δf_d	Hz	100	Doppler Resolution
M		200	Number of Pulses during CPI
Mod		LFM	Modulation Scheme
$B\tau$		122.9	LFM Time Bandwidth Product
B	MHz	21	BPSK Bandwidth
ΔR	m	7.14	BPSK Range Resolution
$B\tau$		105	BPSK Time Bandwidth Product

range updates would occur during the CPI but the target would stay in one radar range bin. The duration of the CPI and the maximum total change in position (equal to the radar range resolution) set the maximum expected velocity. The radar's PRF was then set based on the Doppler bandwidth associated with the velocities of targets to be simulated.

The frequency domain representation of the transmitted waveforms are plotted in Figure 6.1. Note the transmitted power is 40 dBm (10 W) per the hardware specifications in Chapter 5.

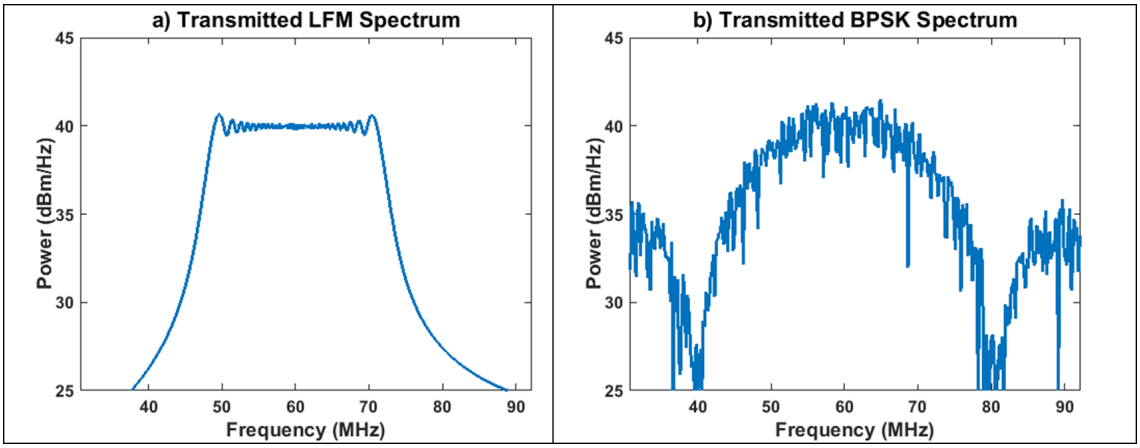

Figure 6.1: Frequency Domain Representation of the Transmitted Waveforms

The majority of the following simulations use the LFM waveform while the BPSK results are

included to support the claim of generality of this target generator algorithm.

All of the following results are formed using identical radar signal processing. First, the received data is oversampled by a factor of 10 and matched filtered in the fast-time dimension. Next, the slow-time data is oversampled by a factor of 4 before its FFT is computed. The processing gain associated with the base case radar parameters are $10log_{10}(\tau B) = 10log_{10}(122.9) = 20.9$ dB for the matched filtering process and $10log_{10}(M) = 10log_{10}(200) = 23$ dB for the coherent integration process for a total of 45 dB of processing gain. The result of the following simulations are the Doppler bin and range bin cuts of the final Range Doppler map that are associated with the highest power response as discussed in Section 2.2.5 Figure 2.9. The BPSK waveform has a slightly lower time-bandwidth product than the LFM and therefore its matched filtering gain is only $10log_{10}(105) = 20.3$ dB. All of the following results have been normalized (the matched filter has been divided by the signal length and the Doppler processed output is divided by the number of pulses). Therefore, the processed signal maintains the pre-processed absolute power level and the noise power is reduced relative to the level of the noise incident on the ADC by the sum of the matched filter and coherent integration gain, 44 dB.

The baseline range for these simulations was chosen such that the input SNR could be overcome by the the radar's processing gain. As computed in Appendix A, the SNR incident on the ADC is -29 dB. The 44 dB of radar processing gain will result in a post processed SNR of 15 dB at the range used in the following simulations. Next, the baseline parameters for the simulated target will be discussed.

6.2 Simulated Target Description

The results discussed in Section 6.3 are generated by comparing the radar's response to two environment models. The first model is referred to as the natural model (NM) and is used to represent the expected response of a radar after interfacing with a real free space target like the example in Figure 2.9. The second model is used to explore the expected response of the radar to a quantized

interpretation of the world as would be produced by the target generator. Both models use the representative noise and SNR values that are derived in Appendix A. New additive white Gaussian noise (AWGN) samples are generated each time the simulation is run.

The natural model operates at the RF and models motion by imparting a continuous phase shift on the backscattered signal following the ideal mathematical formulation and example in Chapter 2. The targets generated by the quantized model (QM), however, are limited by the delay and Doppler resolution of the target generator. Therefore the phase shift applied to the backscattered signal is discontinuous as discussed in Section 3.2. The quantized model does not include other negative effects associated with the target generator from Chapters 4 and 5 such as limited precision numerical representation, algorithm latency, or distortion due to the HDL algorithm. The quantized model operates at the IF like the target generator design.

The baseline parameters for the target that will be simulated in the following sections are shown in Table 6.2.

Table 6.2: Baseline Target Generator Settings

Variable	Units	Value	Description	Case
R0	m	487	Starting Distance to Target	Both
R1	m	490.05	Ending distance to target	Moving
ΔR	m	3.05	Change in Range over CPI	Moving
$f_{\Delta a}$	Hz	500	Range Update Rate	Moving
v	m/s	305.2	Velocity (Doppler Frequency = 4.069 kHz)	Moving
f_D	Hz	4069.0	Doppler Frequency (Velocity = 305 m/s)	Moving
P_{FS}	dBm	4	Radar received Power for ADC full scale range	Both
P_{R0}	dBm	-98.5	Radar received Power associated with target at R0	Both
A_{FS}	dB	21	Attenuation associated with P_{FS}	Both
A_{R0}	dB	119	Attenuation associated with P_{R0}	Both
σ	dBsm	1	Target Radar Cross Section	Both

Section 6.3.1 demonstrates a static target and Section 6.3.2 demonstrates a moving target. In the case of the moving target, the target moves through half of a radar range bin or 3.05 m. Because the range resolution of the radar is ten times the minimum range step size of the target generator, the simulated velocity requires five range updates to be made over the CPI of 0.01 s. The resulting velocity is associated with a Doppler frequency of 4069 Hz, or approximately two-fifths of the

radar's Doppler bandwidth.

The following simulations are executed with one of two settings for the variable attenuator in the target generator receiver. If the attenuation is set to A_{FS} in Table 6.2, the total received power at the radar ADC will be equal to its full-scale range. An attenuation setting of A_{R0}, however, will yield the expected received power associated with the target distance R_0 per Equation 2.1 and Appendix A. This realistic attenuation level masks the details of the simulation result, however, so the minimum attenuation associated with the full-scale range is used in a majority of the simulations presented in the next section.

6.3 Baseline Case

6.3.1 Static Target

The range and Doppler spectrum for the static case with baseline radar and target parameters are documented in Figure 6.2. The figure includes the radar output in response to the targets generated by the NM and QM. Per the calculations in Appendix A, when the attenuation applied by the target generator results in signal at the output of the radar ADC is equal to the full scale range of 4 dBm, the noise level is expected to be -64 dBm. These values yield a pre-processed SNR of 68 dB. After applying the 44 dB of processing gain provided by the radar signal processing operations, the resulting SNR should be 112 dB. Note the normalization associated with the processing steps result in the peak power maintaining a level of 4 dBm (ADC full-scale range) and a decrease in the noise power to -108 dBm.

In the case of the LFM waveform shown in Figure 6.1.a with no windowing, the result of the correlation operation performed by the matched filter has a first range sidelobe expected at a level of 13.2 dBc (point 3,4 in Figure 6.2) [30]. Similarly, the first sidelobe in the non-windowed Doppler spectrum result is expected at 13.2 dBc (point 7,8). The key points of Figure 6.2 are defined in Table 6.3. Note the perfect agreement between the NM and QM results.

Figure 6.2 is the result of the radar processing when the variable attenuator in the target gen-

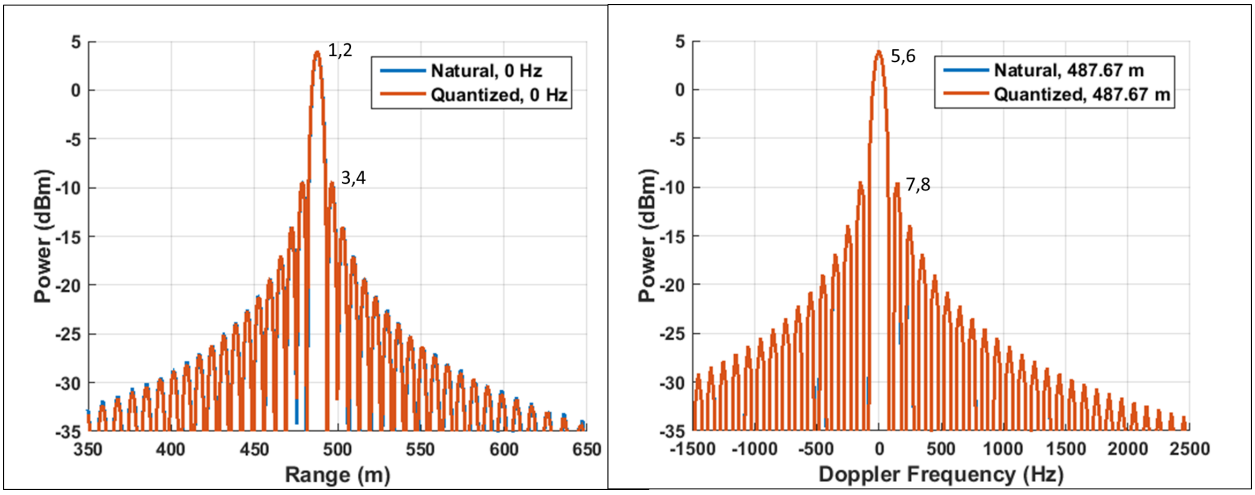

Figure 6.2: Static Target, Attenuation = 21 dB: (Left) - Range Cut, (Right) - Doppler Cut

Table 6.3: Key Points Summary of Figures 6.2 and 6.3

Point	Parameter	Value	dBc
1,5	Peak Power, NM	(487.7 m, 4.0 dBm, 0 Hz)	-
2,6	Peak Power, QM	(487.7 m, 4.0 dBm, 0 Hz)	-
3	Peak Range Sidelobe, NM	(496.8 m, -9.47 dBm)	13.47
4	Peak Range Sidelobe, QM	(496.8 m, -9.47 dBm)	13.47
7	Peak Doppler Sidelobe, NM	(150 Hz, -9.46 dBm)	13.46
8	Peak Doppler Sidelobe, QM	(150 Hz, -9.46 dBm)	13.46
Fig 6.3, 2	Noise Level	(1774 m, -107 dBm)	111 (SNR)

erator transmitter is set to apply the minimum amount of attenuation ($A = 21$ dB) that is required to make the data fit the full-scale range of the radar ADC. The relative signal and noise levels are more clearly illustrated on the left side of Figure 6.3. Note that the SNR for the minimum attenuation case (reported as dBc for the noise level in the last line of Table 6.3) is 111 dB.

The results in Figure 6.4 and the right side of Figure 6.3, on the other hand, demonstrate the result when the variable attenuator setting is $A_{r1} = 119$ dB from Table 6.2. This attenuation yields the expected received power level at the ADC input (-94 dBm) for the return from a target at a range of 487.67 m per the radar range equation while the pre-processed noise level is -66 dBm. The points of interest marked in Figure 6.4 are labeled in Table 6.4.

Like Figure 6.2, the results in Figure 6.4 show almost perfect agreement in the mainlobe response of the radar processing of the natural target model and the quantized target model. This is

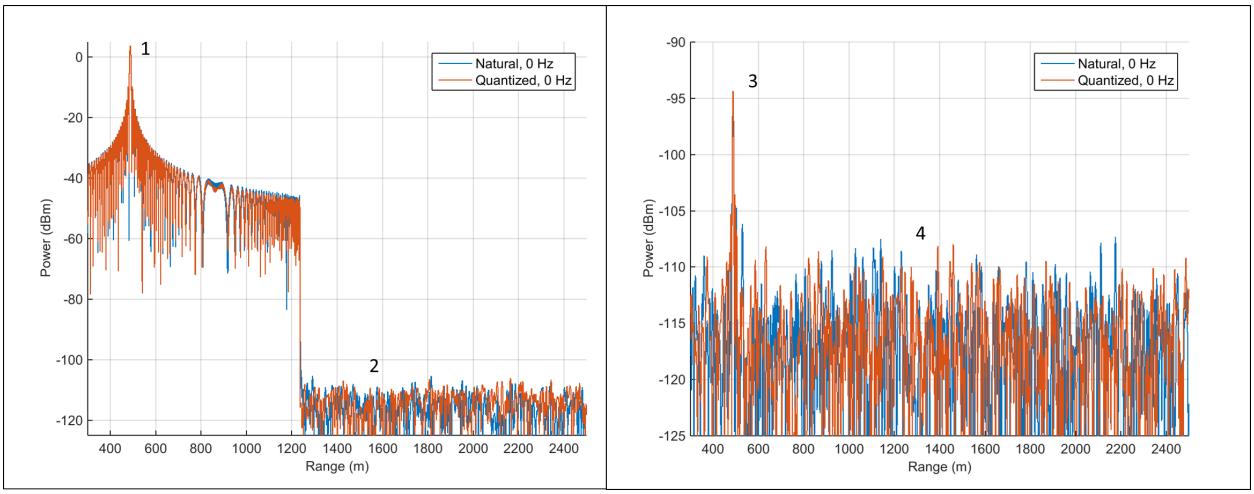

Figure 6.3: Static Target - Range Cuts; (Left) Atten. = 21 dB, (Right) Atten. = 119 dB

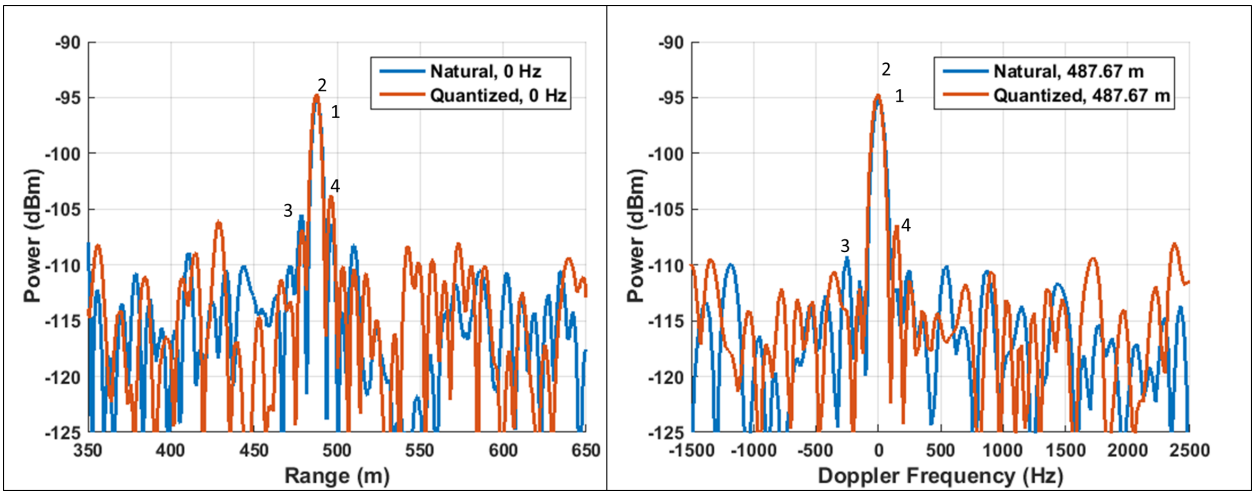

Figure 6.4: Static Target, Atten. = 119 dB: (Left) - Range Cut, (Right) - Doppler Cut

Table 6.4: Key Points Summary of Figures 6.3 and 6.4

Point	Parameter	Value	dBc
1,5	Peak Power, NM	(487.7 m, -95.14 dBm, 0 Hz)	-
2,6	Peak Power, QM	(487.7 m, -94.67 dBm, 0 Hz)	-
3	Peak Range Sidelobe, NM	(478.5 m, -105.5 dBm)	10.36
4	Peak Range Sidelobe, QM	(496.2 m, -103.8 dBm)	9.13
7	Peak Doppler Sidelobe, NM	(-250 Hz, -109.3 dBm)	14.16
8	Peak Doppler Sidelobe, QM	(150 Hz, -106.4 dBm)	11.73
Fig. 6.3, 4	Noise Level	(1368 m, -108.5 dBm)	14.36 (SNR)

an indication that the synthetic target would create an accurate model of the target that could be used for testing.

The first range and Doppler sidelobes are still expected to be at 13.2 dBc. Notice, however, that the processed noise level is of the same order as the expected side lobe level and is responsible for producing results that vary from expectations in Table 6.4. The 14.36 dB of SNR associated with these results is within 1 dB of what was expected in the calculations in Appendix A.

It is clear that an emulated target at this range could be detected by the radar system if the radar were to apply a threshold to the output of the radar processing of approximately 10 dBc. This is a valid appraoch as long as sufficient confidence exists that noise spikes will not cause false detections.

6.3.2 Moving Target

Next, Figure 6.5 demonstrates the NM and QM representations of a moving target with the minimum attenuation setting; $A = 21$ dB. Recall the baseline target parameters for the moving case are in Table 6.2. The target starts at 487.76 m and moves 3 m toward the radar over the CPI resulting in a positive Doppler shift of 4.069 kHz. It is evident from the Doppler cut that there are significant differences between how the NM and QM targets are interpreted by the radar. The points of interest marked in Figure 6.5 are labeled in Table 6.5. The radar parameters are unchanged relative to the results in Section 6.3.1.

Note that peak power measured in these results is approximately 1 dB lower than the static case discussed in Section 6.3.1. Furthermore, rather than sidelobes in range and Doppler that are approximately 13.2 dBc, in this case the sidelobes are in the range of 14 to 15 dBc. The difference in peak magnitude is due to the fact that its motion is associated with a widening of the main lobe even though the target is staying within one radar range bin.

Before discussing the differences between the radar response to the NM and QM targets, it is worth noting that again there is almost perfect agreement between the models in the fast time dimension. The peak power in the mainlobe only differs by approximately 0.5 dB and in both

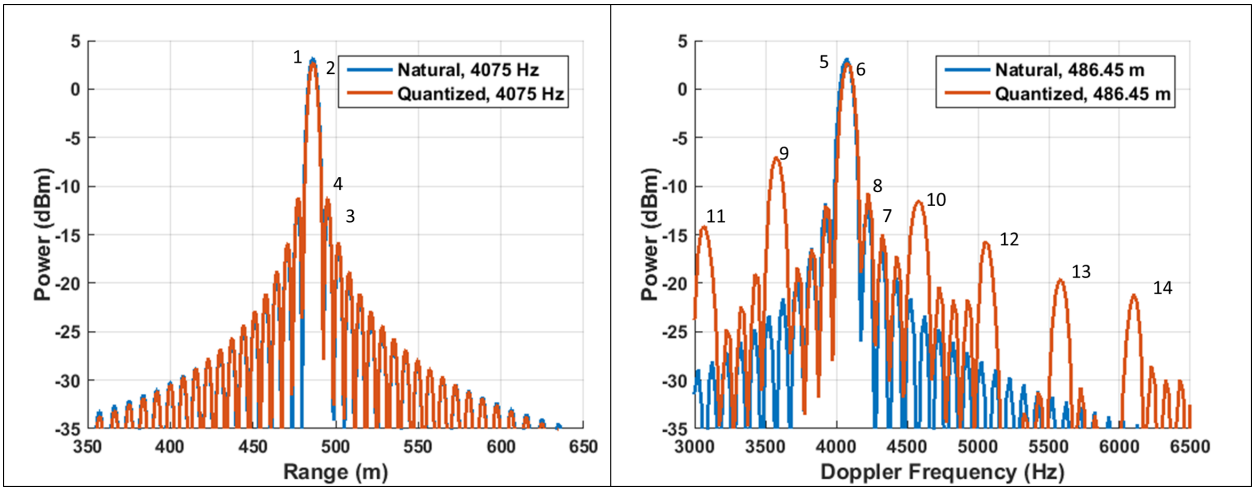

Figure 6.5: Moving Target, Basic Case, Atten. = 21 dB: (Left) - Range Cut, (Right) - Doppler Cut

Table 6.5: Key Points Summary of Figure 6.5

Point	Parameter	Value	dBc
1,5	Peak Power, NM	(486.5 m, 3.16 dBm, 4075 Hz)	-
2,6	Peak Power, QM	(486.5 m, 2.74 dBm, 4075 Hz)	-
3	Peak Range Sidelobe, NM	(495.6 m, -11.89 dBm)	15.05
4	Peak Range Sidelobe, QM	(495.0 m, -11.25 dBm)	13.99
7	Peak Doppler Sidelobe, NM	(4225 Hz, -11.99 dBm)	15.15
8	Peak Doppler Sidelobe, QM	(4225 Hz, -10.69 dBm)	13.43
9	First Model Doppler Spur, QM	(3575 Hz, -6.96 dBm)	9.70
10	Second Model Doppler Spur, QM	(4575 Hz, -11.52 dBm)	14.26
11	Third Model Doppler Spur, QM	(3075 Hz, -14.18 dBm)	16.92
12	Fourth Model Doppler Spur, QM	(5050 Hz, -15.64 dBm)	18.38
13	Fifth Model Doppler Spur, QM	(5575 Hz, -19.60 dBm)	22.34
14	Sixth Model Doppler Spur, QM	(6100 Hz, -21.13 dBm)	23.87

cases, the target is detected at a range of 485.6 m and a Doppler frequency of 4075 Hz as expected. Furthermore, the sidelobe structure in both the range and Doppler plots are almost identical for the first 3 sidelobes.

The primary difference between the two models is present in the Doppler spectrum shown in the right side of Figure 6.5. The spurious nature of the Doppler spectrum of the QM is due to the phase discontinuities associated with the moving target when the target generator memory pointer spacing changes. In this example, because the target generator IF is 60 MHz, each range step is associated with a phase change of $\approx 87.9^{\circ}$ per Equation 3.9. The location of the spurious signals

are predicted by Equation 3.8. Their spacing is equal to the update rate $f_{\Delta a}$ and referenced to the Doppler frequency. In this case, the Doppler frequency is 4.069 kHz and $f_{\Delta a}$ is 500 Hz, so the nearest spurs are expected at 4.569 kHz and 3.569 kHz. Due to the granularity of the Doppler spectrum, these spurs appear at 4.575 kHz and 3.575 kHz (indicated by points 9 and 10 in Figure 6.5).

The presence of these spurs limits the effectiveness of the target generator model. The spur at point 9 is only 9.7 dBc. If the detection algorithm in the radar under test applies the same threshold that was sufficient in Section 6.3.1, the output spectrum in Figure 6.5 may result in more than one target being perceived by the radar.

Figure 6.6 demonstrates the moving target result when the range-appropriate attenuation of $A = 119$ dB has been applied by the target generator. In this case, the discrepancy between the two models is not as easy to identify because the noise is masking the spurious effects of the model. The Doppler spectrum spur at point 9, however, is still visible with the help of Equation 3.8 knowledge of the update rate and referencing the results in Figure 6.5. The key points of Figure 6.6 are labeled in Table 6.6.

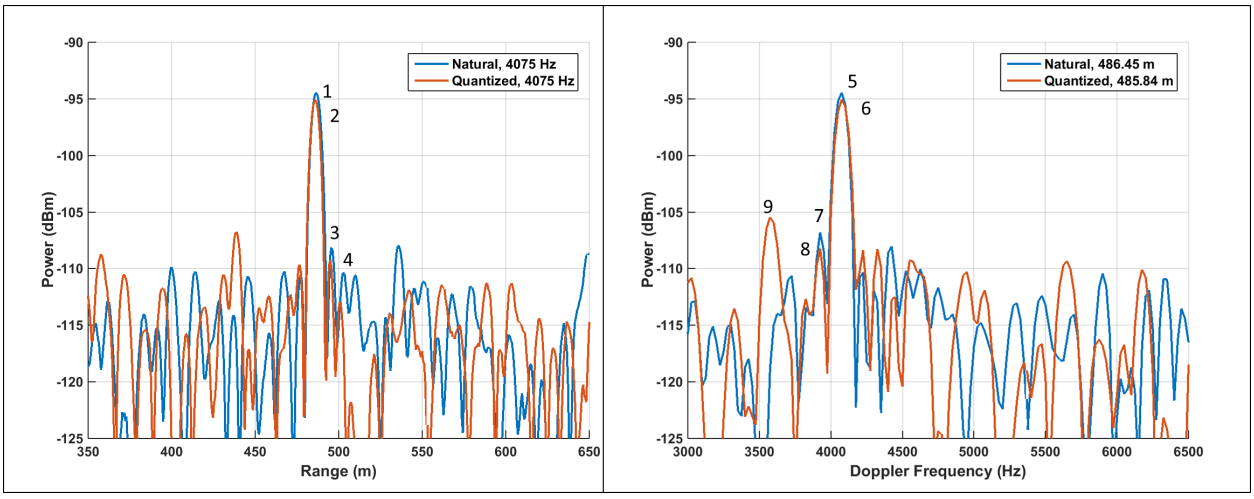

Figure 6.6: Moving Target, Base Case, Atten. = 119 dB: (Left) - Range Cut, (Right) - Doppler Cut

This result is the first case in which the range values reported for the NM and QM targets differ. Referencing the expression for range measurement accuracy in Equation 2.6, and using $\Delta R = 6.01$ and $SNR = 10^{(15/10)}$, $\sigma_R = \frac{6.01}{\sqrt{10^{1.5}}} = 2.78$ m. While this accuracy statement has not been rigorously

Table 6.6: Key Points Summary of Figure 6.6

Point	Parameter	Value	dBc
1,5	Peak Power, NM	(486.5 m, -94.45 dBm, 4075 Hz)	-
2,6	Peak Power, QM	(485.8 m, -95.07 dBm, 4075 Hz)	-
3	Peak Range Sidelobe, NM	(495.6 m, -108.2 dBm)	13.75
4	Peak Range Sidelobe, QM	(495 m, -109.2 dBm)	14.13
7	Peak Doppler Sidelobe, NM	(3925 Hz, -106.8 dBm)	12.35
8	Peak Doppler Sidelobe, QM	(3925 Hz, -108.2 dBm)	13.13
9	Peak Model Doppler Spur, QM	(3925 Hz, -105.4 dBm)	10.30

proven in terms of these models, it offers a possible reason for the discrepancy in Figure 6.6 that can be explored in future work.

The results in Sections 6.3.1 and 6.3.2 represent the baseline to which the following simulations are compared. Special care should be taken to compare the absolute and relative power levels of the spurs as indicated in Tables 6.3 and 6.5 to the results presented in Sections 6.4 through 6.7.

Next, the parameters from Tables 6.1 and 6.2 will be modified to demonstrate how the radar's response changes as the simulated target changes attributes of the radar, the target, or the target generator are modified. The goal of the following discussion is to develop intuition about the relationship between the radar and target generator. All of the following simulations are performed with an LFM waveform and use the minimum target generator attenuation setting so changes to the artifacts of the QM can be easily identified.

6.4 Variations on the Target Baseline

This section focuses on how the radar's response changes with respect to target-specific changes. These results demonstrate the differences present in the interpretation of various targets that a radar may be designed to detect. The results in this section are of critical importance to a testing application where targets with a range of attributes may be simulated.

6.4.1 Velocity

As it has been established that the update rate and phase discontinuities due to target generator step changes are directly responsible for the spurious output Doppler spectrum, the cases considered in this section were designed such that the velocities require a specific number of target generator steps to complete the scenario simulation. The three cases considered here are described in Table 6.7 and should be compared to the Section 6.3.2 results in Table 6.5 and Figure 6.5.

Table 6.7: Values for v

Model	v (m/s)	f_D (Hz)	$f_{\Delta a}$ (Hz)	TG Steps	Expectation
QM, $v = v_{base}$ (Fig 6.5)	**-305.2**	**4069**	**500**	**5**	**Spacing at 500 Hz**
QM, $v = 0.1v_{base}$	-30.52	406.9	0.05	0	Smooth Response
QM, $v = 0.3v_{base}$	-91.55	1220.7	0.15	200	Spacing at 200 Hz
QM, $v = 0.5v_{base}$	-152.58	2034.5	0.25	300	Spacing at 300 Hz
Natural Model	all cases above			-	Smooth Response

The first result in Figure 6.7 represents a case where the target generator is emulating a target that requires no delay updates over the CPI. During the CPI, the target moves 0.05 radar range bins or 0.31 m which is half of the distance associated with the minimum target generator delay step. In this case, the target generator's memory update algorithm will be of no use for the range simulation. Due to its quantization in range, the target generator is effectively emulating a stationary target with a fixed Doppler shift. The Doppler shift evident below is entirely caused by the Doppler correction portion of the target generator architecture. The NM, on the other hand, includes motion that causes range walk and is responsible for its slight peak degradation relative to the QM and the discrepancy in range reported in the legend of Figure 6.7. The Doppler spectrum in Figure 6.7 shows almost perfect agreement between the two models and the result in Figure 6.7 strongly resembles the stationary case in Figure 6.2.

The next case, shown in Figure 6.8, represents the situation where the emulated target velocity requires one target generator delay update. In this case, the update occurs halfway through the simulation so the target spends approximately equal time at two discrete locations emulated by the target generator. In this case, the expected spur spacing is 200 Hz; something that can be easily

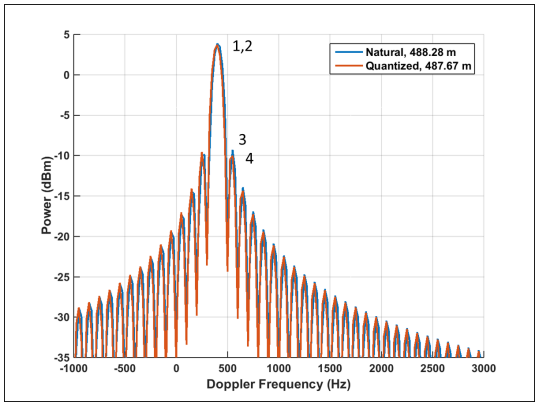

Figure 6.7: Doppler Spectrum, $v = 0.1v_{base}$

Table 6.8: Summary of Figure 6.7

Point	Parameter	Value	dBc
1	Pk Pwr, NM	400 Hz, 3.90 dBm	-
2	Pk Pwr, QM	400 Hz, 3.98 dBm	-
3	Pk DSL, NM	550 Hz, -9.30 dBm	13.20
4	Pk DSL, QM	550 Hz, -9.77 dBm	13.75

observed in the figure summary provided in Table 6.9. The Doppler spurs result in an elevation of the QM spectrum by approximately 3 dB relative to the NM spectrum across the band. The significant exception to this rule is at point 4 in Figure 6.8 where a Doppler sidelobe corresponds with a spur and the result is elevated by approximately 6 dB relative to the NM.

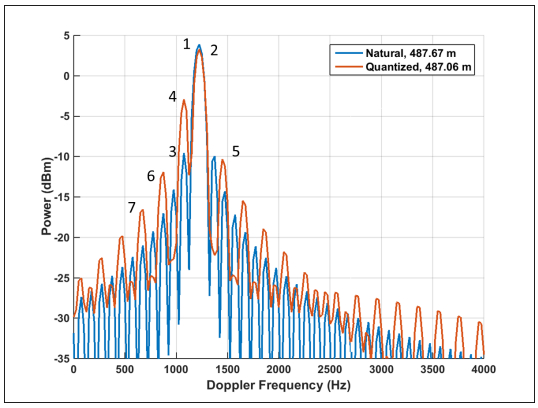

Figure 6.8: Doppler Spectrum, $v = 0.3v_{base}$

Table 6.9: Summary of Figure 6.8

Point	Parameter	Value	dBc
1	Pk Pwr, NM	1225 Hz, 3.88 dBm	-
2	Pk Pwr, QM	1225 Hz, 3.28 dBm	-
3	Pk DSL, NM	1075 Hz, -9.856 dBm	13.44
4	Pk DSL, QM	1075 Hz, -2.93 dBm	6.21
5	Spur, QM	1450 Hz, -10.30 dBm	13.58
6	Spur, QM	875 Hz, -11.94 dBm	15.22
7	Spur, QM	675 Hz, -16.52 dBm	19.80

Finally, Figure 6.9 demonstrates a case where two target generator updates and therefore three quantized ranges are required to represent the target motion. The target is moving at 50% of the base case velocity and therefore moves 1.5 m over the CPI. The spurs in the Doppler spectrum for this case appear to be interfering with each other in this example because their spacing is not as consistently equal to $f_{\Delta a}$. Specifically, points 4-6 and 8-10 are spaced as predicted, but not with respect to each other, and point 7 is an outlier. The general effect of the spurious spectrum, however, is the same as the other results. This case also reveals a discrepancy in the measured Doppler

frequency of the target. While the NM measures the Doppler at 2025 Hz, the QM measures it at 2050 Hz. It is worth noting that the nominal value for the simulated Doppler frequency is 2034.5 Hz and the boundary between the two Doppler bins in question is at 2037.5 Hz.

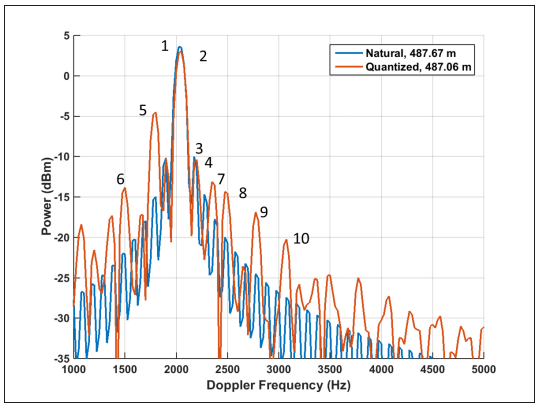

Figure 6.9: Doppler Spectrum, $v = 0.5v_{base}$

Table 6.10: Summary of Figure 6.9

Point	Parameter	Value	dBc
1	Pk Pwr, NM	2025 Hz, 3.60 dBm	-
2	Pk Pwr, QM	2050 Hz, 3.05 dBm	-
3	Pk DSL, NM	2175 Hz, -10.02 dBm	13.6
4	Pk DSL, QM	2200 Hz, -10.37 dBm	13.4
5	Spur, QM	1800 Hz, -4.47 dBm	7.5
6	Spur, QM	1500 Hz, -13.81 dBm	16.9
7	Spur, QM	2350 Hz, -13.09 dBm	16.1
8	Spur, QM	2475 Hz, -14.35 dBm	17.4
9	Spur, QM	2775 Hz, -16.88 dBm	19.9
10	Spur, QM	3075 Hz, -20.24 dBm	23.2

It is very important to note that as it is likely that a radar is designed to detect targets with Doppler shifts across its Doppler bandwidth, a radar under test will see all of these spectral responses as function is being tested and characterized. Therefore, the repeatable way in which the velocity changes the output response should be taken into consideration of the results or used as a calibration factor to correct the radar measurement. Table 6.11 provides a comparison between the previous results.

Table 6.11: Results of Varying Target Velocity, v

	v_{base} - (4 steps)	$0.1v_{base}$ - (0 step)	$0.3v_{base}$ - (1 step)	$0.5v_{base}$ - (2 steps)
Peak	2.74 dBm	3.98 dBm	3.28 dBm	3.05 dBm
PSL	+150 Hz, 15.15 dBc	+150 Hz, 13.75 dBc	+150 Hz, 6.20 dBc	+150 Hz, 13.42 dBc
Peak Spur	-500 Hz, 9.70 dBc	-	+225 Hz, 13.58 dBc	+250 Hz, 7.52 dBc

The conclusion associated with these results is that the relative height of the peak spur due to the quantized model changes as velocity is varied in addition to the expected change in spur spacing. Two cases in this section resulted in spurs greater than 8 dBc. This spur level may be unacceptable for some radar processing schemes.

6.4.2 Multiple Targets

This section exhibits a case where two targets are modeled with the QM as represented by the parallelization of the digital kernel in Figure 3.3. To avoid over-complicating the plot in Figure 6.10, the NM results are not included here. As was discussed in Chapter 2 it is known that superposition will apply to targets in the natural model. Therefore the expected NM Doppler spectrum result for multiple targets would be equal to that in the base case moving target scenario in Figure 6.5.

The result in Figure 6.10 suggests that superposition also applies to the QM. In this case, two targets at different ranges and velocities are simulated. The Single Target (blue) trace indicates the familiar base case target with Doppler frequency of 4.069 kHz (measured at 4075 Hz). The spectrum in the Two Target (red) case includes all of the Doppler spurs from both targets. The second target's Doppler shift is expected to be 5.280 kHz (measured at 5275 Hz).

Points 7 and 10 in Figure 6.10 for example, are spurs only associated with Target 2, while points 4, 6, and 8 represent frequencies where the Target 1 spurs are present in both models. It is the difference between the latter set of points that demonstrate the coherent summation of the two targets via superposition in the Two Target case.

One thing that is obvious from the summary of these results in Table 6.12 is that further from the Doppler frequency of interest, the power level of the spurs in the two target model begin to match those of the single target model, as is evidenced by point 4, and visual consideration of the spectrum at 7000 Hz and above. Furthermore, the spurs are elevated especially in the region between the two targets as is evidenced by the differences in height of point 3, 6, and 8. This type of behavior is to be expected in the case of superposition.

In conclusion, the results in Figure 6.10 and Table 6.12 suggest that it is possible to simulate multiple targets with the quantized model without experiencing a significant increase in the elevation of the Doppler spectrum associated with multiple targets. There are likely to be worse cases that the targets considered here, namely the $0.2v_{base}$ or $0.3v_{base}$ cases discussed previously in section 6.4.1.

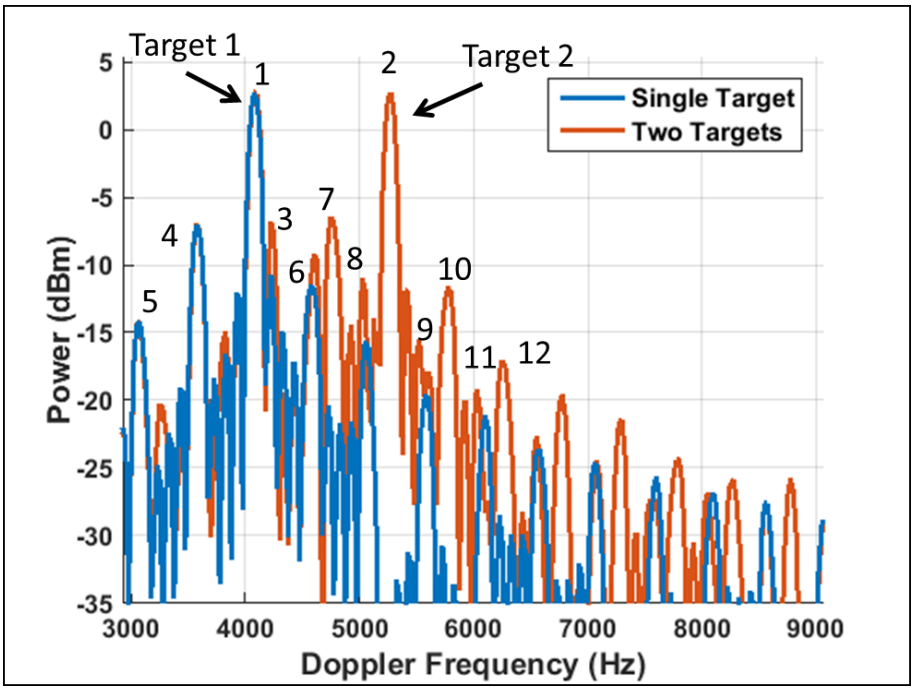

Figure 6.10: Comparison of Doppler Spectrum with of a Single and Multiple Target Simulation

Table 6.12: Key Points Summary of Figure 6.10

Point	Parameter	1 Target Value	dBc	2 Target Value	dBc
1	Pk Pwr, TGT1	(4075 Hz, 2.74 dBm)	-	(4075 Hz, 2.82 dBm)	-
2	Pk Pwr, TGT2	-	-	(5275 Hz, 2.76 dBm)	-
3	Pk DSL, TGT1	(4225 Hz, -10.69 dBm)	13.43	(4225 Hz, -6.82 dBm)	9.64
4	Spur, TGT1	(3575 Hz, -6.96 dBm)	9.70	(3575 Hz, -6.96 dBm)	9.78
6	Spur, TGT1	(4600 Hz, -11.73 dBm)	14.47	(4600 Hz, -9.18 dBm)	12.0
7	Spur, TGT2	-	-	(4750 Hz, -6.42 dBm)	9.18
8	Spur, TGT1	(5050 Hz, -15.64 dBm)	18.38	(5025 Hz, -10.99 dBm)	13.81
10	Spur, TGT2	-	-	(5775 Hz, -11.61 dBm)	14.37

6.5 Variations on the Radar Baseline

Now that intuition has been developed regarding how the radar's response to varying target parameters can change, the following section will hold the target constant and vary the radar parameters.

6.5.1 PRF and Number of Pulses and CPI

Changing the values for the PRF, M, and CPI resulted in negligible changes to the simulation results as was expected. If the CPI remains constant, an increase in the PRF will result in an increased Doppler bandwidth. No change is expected due to the velocity's percent of the Doppler bandwidth, just in how the range crossings relate to the target generator delay spacing as was illustrated in Section 6.4.1. Furthermore, increasing the PRF while the CPI is held constant will yield an increase in the number of pulses that are transmitted and therefore a 3 dB increase to the coherent integration gain will be realized during processing.

Increasing the CPI yields a refinement in the Doppler resolution. While this refinement may be used as a tool to better distinguish differences between the NM and QM Doppler spectrum, the finer resolution will not change the nature of the results. If the radar processing features a shorter CPI, the Doppler resolution will be degraded and the output spectrum will tend to appear elevated due to the presence of spurs while losing the lobe-and-null structure that has been present in all the results shown here.

6.5.2 Bandwidth

This section explores the effects of changing the radar bandwidth and thereby the radar range resolution. It is expected that changing the range resolution will yield a predictable change to the range dimension response but it will not appreciably affect the Doppler spectrum. In the cases presented in Figure 6.11, the target velocity is held constant, but in each unique bandwidth condition, the target moves through a different percentage of the radar's range resolution cell. The specific cases considered here are summarized in Table 6.13.

Table 6.13: Values for Bandwidth and Range Resolution

Model	BW (MHz)	ΔR (m)	Radar Bin
QM, $\Delta R = \Delta R_{base}$ (Fig 6.5)	**24.58**	**6.10**	**0.5**
QM, $\Delta R = 2\Delta R_{base}$	12.28	12.2	0.25
QM, $\Delta R = 0.5\Delta R_{base}$	49.21	3.05	1
Natural Model	all cases above		

Figure 6.11 facilitates comparison between the various range resolution settings and the response for the NM and QM.

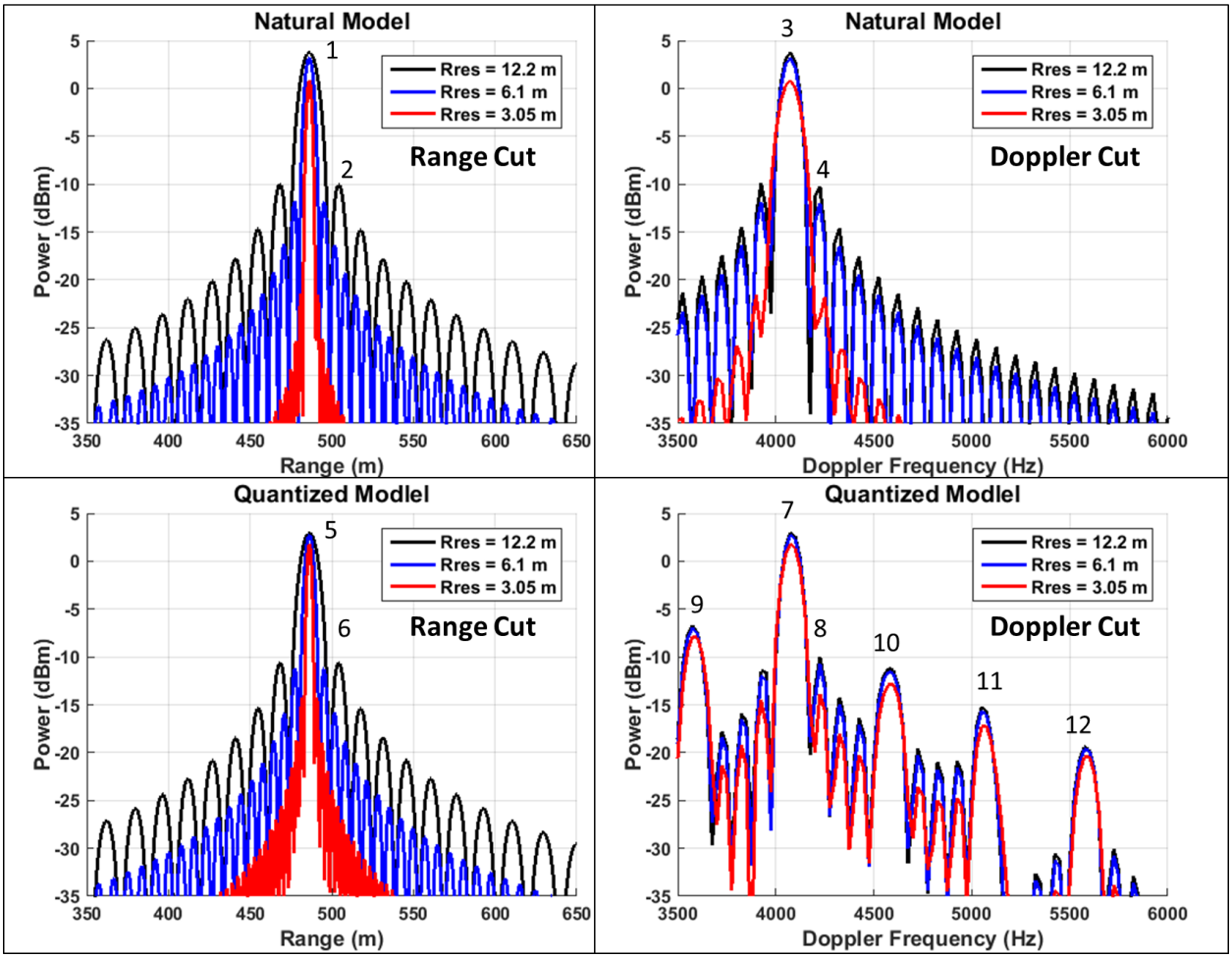

Figure 6.11: Results of Variation of Range Resolution

The QM shows less variation in peak power as the range resolution changes than the NM, due to the fact that it is not covering as much distance as the NM. The QM target will always move a shorter distance than the NM unless the total change in range for the simulation is an integer

multiple of the range associated with the target generator delay step size. The shorter distance covered by the QM target yields slightly less broadening of the mainlobe and therefore higher main lobe energy and less sidelobe suppression. Extending this conclusion to the variation in range resolution, as the total target motion occupies a larger percent of the radar range bin, the mainlobe power is decreased, the mainlobe width is increased and the sidelobes are suppressed. This phenomena is referred to as range walk [30]. The suppression of the main lobe is the most significant at the finest range resolution ($\Delta R = 3.05$ m) when the target motion is moving through an entire range bin. The fact that the Doppler spectrum is also impacted by this phenomena is due to the Range-Doppler coupling nature of the LFM as discussed in [18].

The results of this section reaffirm expected results regarding range walk and resolution as the radar's bandwidth is modified. Furthermore, they continue the demonstration of strong agreement between the NM and QM in range and consistency in the non-ideal aspects of Doppler spectrum response.

6.5.3 Windowed Results

In this section, the radar signal processing will be modified to to include a 55 dB Taylor window in both the range and Doppler processing. The performance of the Taylor window relative to the rectangularly windowed result is demonstrated in Figure 6.12 and Table 6.14 where the widening of the mainlobe and -55 dBc sidelobe suppression is the expected result. Note that the sidelobes in the windowed NM result have been pushed down to approximately -50 dBm by the window.

Table 6.14: Key Points Summary of Figure 6.12

Point	Parameter	Value	dBc
1	Pk Pwr, NM	(486.5 m, 3.59 dBm)	-
1	Pk Pwr, Win	(486.5 m, 2.91 dBm)	-
2	Pk RSL, NM	(495.6 m, -12.15 dBm)	15.74
3	Pk RSL, Win	(504.8 m, -45.76 dBm)	48.67
4	Pk DSL, NM	(4225 Hz, -12.25 dBm)	15.84
5	Pk DSL, Win	(4375 Hz, -53.0 dBm)	55.91

The goal of using the window is to fully expose the characteristics of the model which are at

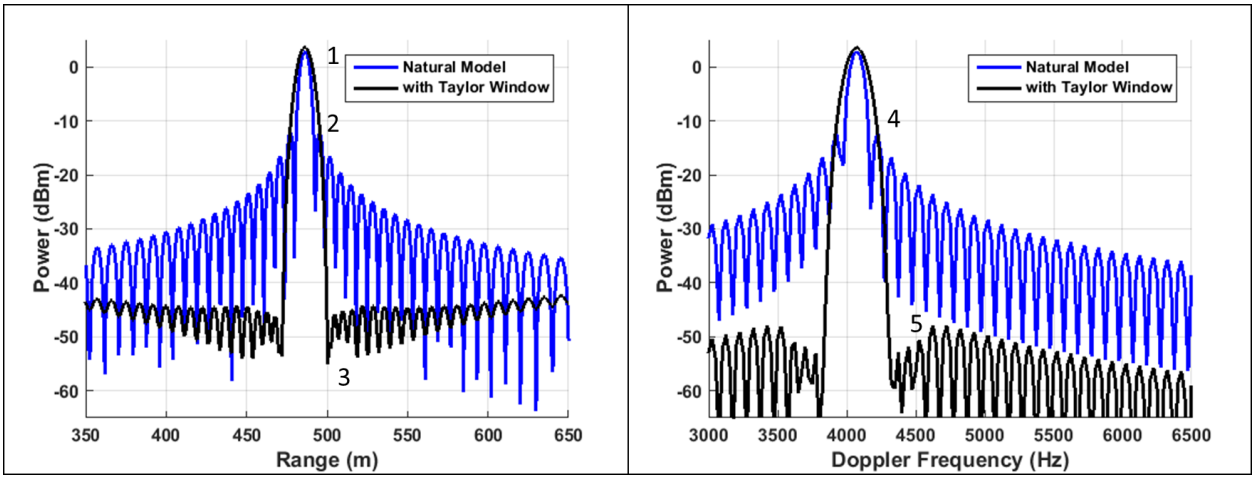

Figure 6.12: Natural Model With and Without Windowing

known positions far from the main lobe. Figure 6.13 demonstrates the effect of the window on the QM. While the sidelobes are suppressed in similar fashion to the NM, the spurious effects of the target generator algorithm are not suppressed by windowing.

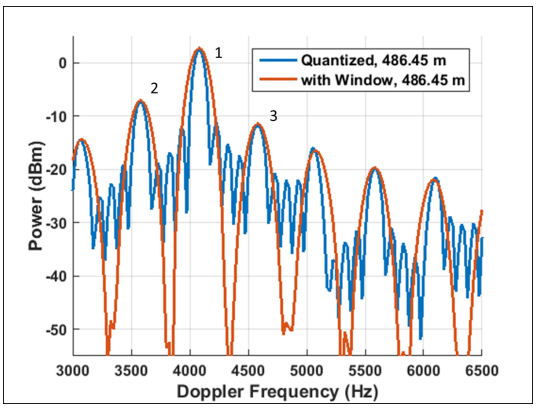

Figure 6.13: Doppler spectrum of Quantized Model with Windowing

Table 6.15: Key Points Summary of Figure 6.13

Point	Parameter	Value	dBc
1	Pk Pwr, QM	4075 Hz, 2.5 dBm	-
1	Pk Pwr, Win	4075 Hz, 2.8 dBm	-
2	Spur, QM	3575 Hz, -7.2 dBm	9.7
2	Spur, Win	3575 Hz, -7.0 dBm	9.8
3	Spur, QM	4575 Hz, -11.8 dBm	14.3
3	Spur, Win	4575 Hz, -11.4 dBm	14.2

6.5.4 BPSK

This section presents an analysis of the moving target in Section 6.3.2 with a BPSK waveform, the spectrum of which is shown in Figure 6.1.b. The modulation is a length 105 minimum peak sidelobe code from [32] with an expected peak to range sidelobe ratio of -26.4 dB in the matched filter output. This code was selected so that the time-bandwidth product and range resolution would be comparable with the LFM waveform used in the other simulations.

The results are presented in Figure 6.14 and Table 6.16. The range result looks different as expected, due to the different waveform but there is strong agreement between the Doppler spectrum in Figure 6.6 and Figure 6.14 below.

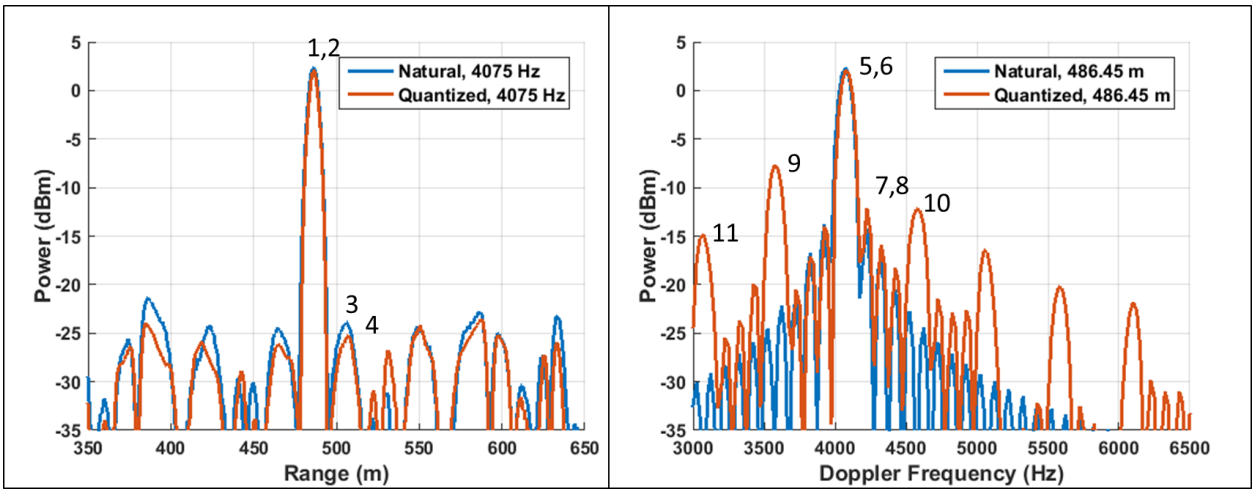

Figure 6.14: Baseline Case with BPSK

Table 6.16: Key Points Summary of Figure 6.14

Point	Parameter	Value	dBc
1,5	Peak Power, NM	(486.5 m, 2.36 dBm, 4075 Hz)	-
2,6	Peak Power, QM	(486.5 m, 2.13 dBm, 4075 Hz)	-
3	Peak Range Sidelobe, NM	(506.6 m, -23.91 dBm)	26.27
4	Peak Range Sidelobe, QM	(506.6 m, -25.25 dBm)	27.38
7	Peak Doppler Sidelobe, NM	(4225 Hz, -14.24 dBm)	16.60
8	Peak Doppler Sidelobe, QM	(4225 Hz, -12.25 dBm)	14.28
9	First Model Doppler Spur, QM	(3575 Hz, -7.61 dBm)	9.74
10	Second Model Doppler Spur, QM	(4575 Hz, -12.18 dBm)	14.31
11	Third Model Doppler Spur, QM	(3075 Hz, -14.18 dBm)	16.99

Note that points 9, 10, and 11 are at the same Doppler frequency and have almost an identical absolute and relative power levels to the results in Table 6.16. This result is significant because it supports the expectation that this target generator architecture is waveform independent. The following simulations return to using the LFM waveform under the assumption that a different waveform would yield the same spurious Doppler spectrum and that techniques that improve the result would also be effective in the case of a different waveform.

6.6 Variations on the Target Generator Baseline

Next, the target generator design parameters will be varied relative to the values defined in Table 5.15. These results will develop how the target generator design impacts the quality of the target as perceived by the radar's processing.

6.6.1 Sampling Rate

First, the target generator sampling rate will be varied as shown in Table 6.17 while the remaining parameters are held constant. An increase in the sampling rate results in a decrease in the minimum range step size of the target generator but does not impact the range dimension of the radar processing.

Table 6.17: Values for f_s

Title	Value	Units	Expectation	t_d	$f_{\Delta a}$
QM, Base Case (Fig.6.5)	**245.76**	**MHz**	**500 Hz spur spacing**	**4.069 ns**	**500 Hz**
QM, $f_s = 2f_{sbase}$	491.52	MHz	1 kHz spur spacing	2.038 ns	1 kHz
QM, $f_s = 4f_{sbase}$	983.04	MHz	2 kHz spur spacing	1.019	2 kHz
Natural Model	all cases above		Smooth Response	all cases above	

The ability to move a target by a smaller step size suggests that the target would be moved more often to maintain the same velocity (or vice versa). In these simulations, if the sampling frequency is doubled, the number of times the target is moved doubles. This also results in a doubling of the update rate, $f_{\Delta a}$. Therefore, the spacing of the spurs in the Doppler spectrum is

also expected to increase by a factor of two; a highly desirable result. The sampling rate has an inverse relationship with the size of the phase shift imparted with every target generator step. A doubling in the sampling rate would reduce the phase discontinuity by half. The measurement of the range to the target and the Doppler frequency associated with the target, should not change.

The cases summarized in Table 6.17 are depicted in Figures 6.5 (Section 6.3), 6.15, and 6.16. The points of interest in these figures are shown in Tables 6.5 (Section 6.3), 6.18, and 6.19 respectively. No range cuts are shown in these figures because the variation in sampling rate had a negligible effect in range as expected.

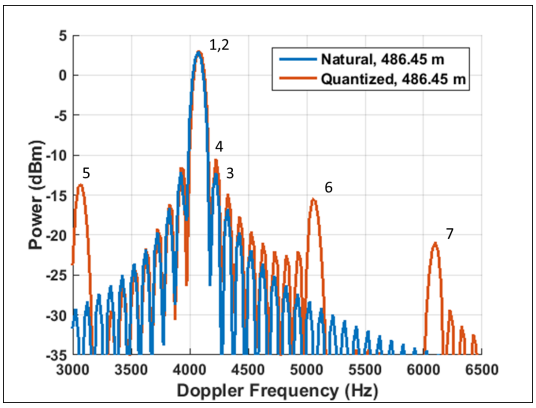

Figure 6.15: Doppler Spectrum, $2f_s$

Table 6.18: Summary of Figure 6.15

Point	Parameter	Value	dBc
1	Pk Pwr, NM	(4075 Hz, 3.16 dBm)	-
2	Pk Pwr, QM	(4075 Hz, 3.39 dBm)	-
3	Pk Dop SL, NM	(4225 Hz, -11.99 dBm)	15.15
4	Pk Dop SL, QM	(4225 Hz, -10.20 dBm)	13.83
5	Model Spur, QM	(3075 Hz, -13.40 dBm)	16.79
6	Model Spur, QM	(5050 Hz, -15.25 dBm)	18.64
7	Model Spur, QM	(6100 Hz, -20.67 dBm)	24.06

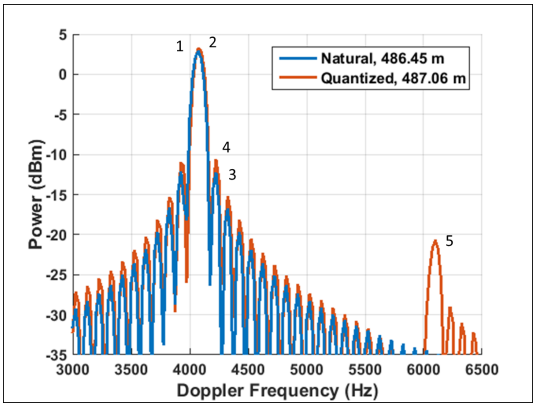

Figure 6.16: Doppler Spectrum, $4f_s$

Table 6.19: Summary of Figure 6.16

Point	Parameter	Value	dBc
1	Pk Pwr, NM	(4075 Hz, 3.16 dBm)	-
2	Pk Pwr, QM	(4075 Hz, 3.59 dBm)	-
3	Pk Dop SL, NM	(4225 Hz, -11.99 dBm)	15.15
4	Pk Dop SL, QM	(4225 Hz, -10.31 dBm)	13.90
5	Model Spur, QM	(6100 Hz, -20.45 dBm)	24.04

A point of interest is that while the progression from f_s to $4f_s$ results in the reduction in the number of Doppler spurs due to the model, the main lobe response and sidelobe structure of the Doppler spectrum remain relatively unchanged and show good agreement with the natural model.

In both cases, the QM main lobe power level is slightly higher than the NM main lobe. As was covered in Section 6.5.2, this is likely because the QM target covers slightly less distance than the NM due to its inherent quantization in range.

Another result of interest is that point 7 in Figure 6.15 and point 5 in Figure 6.16 are at an identical level. The equal location of the two spurs is to be expected because the update rate for the results in Figure 6.16 is a multiple of that in Figure 6.15.

Table 6.20: Results of Varying Target Generator Sampling Rate, f_s

Param	Natural	Base Case	$2f_s$	$4f_s$
Peak	4075 Hz, 3.2 dBm	4075 Hz, 2.7 dBm	4075 Hz, 3.4 dBm	4075 Hz, 3.6 dBm
PSL	4225 Hz, -12 dBm	4225 Hz, -12 dBm	4225 Hz, -10.20 dBm	4225 Hz, -10 dBm
Pk Spur	-	3575 Hz, -7.6 dBm	3075 Hz, -13 dBm	6100 Hz, -20 dBm

Table 6.20 provides a summary of the key points of comparison between the four cases compared in this section. The conclusion associated with these results is that oversampling of the data at the input to the target generator yields a clearer Doppler spectrum. As seen in Table 6.20, all four cases yield comparable peak responses The $4f_s$ result in Figure 6.16 has the best result as the first spur is located at 150% of the Doppler frequency away with a power level of 20 dBc.

6.6.2 Intermediate Frequency

This section is focused on varying the target generator's IF. Considering the relationship in Equation 3.9, the magnitude of the phase change was directly related to the radar's transmit frequency while the discrete delay steps occur. Therefore as the IF increases, a more significant discontinuity in the data will manifest.

Figure 6.17 and Table 6.21 demonstrate the effect of varying the IF frequency. These cases are associated with $\Delta\phi$ equal to 44° when the IF is 30 MHz, 88° when the IF is 60 MHz, and 131° when the IF is 90 MHz. The NM is not included in these results because it operates at the RF.

It is clear from these results that a decreased IF results in less pronounced spurs in the Doppler spectrum. The reason for this trend is clearly depicted in Figure 6.18.

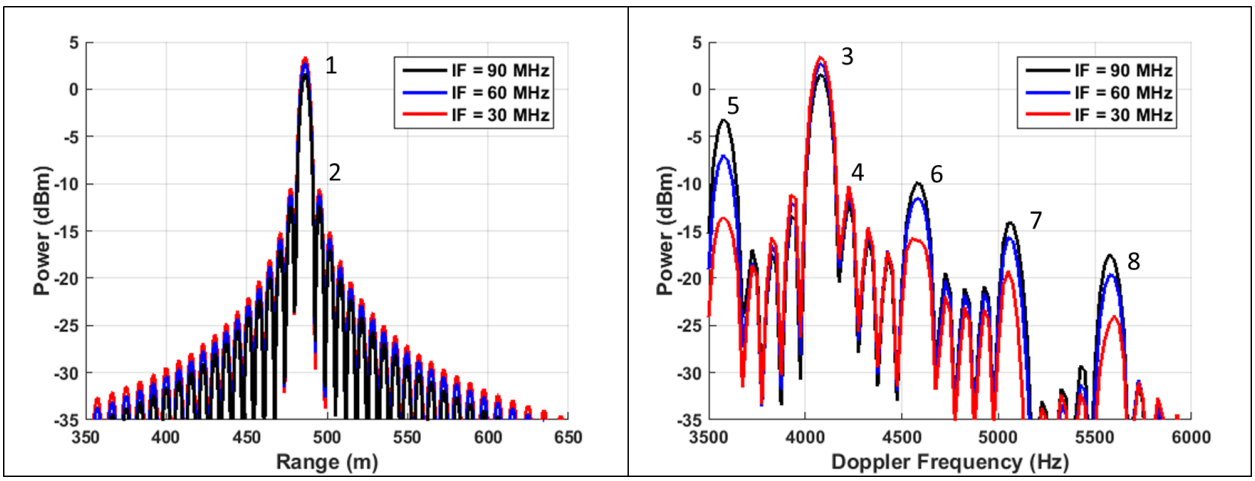

Figure 6.17: Comparison of three different values for f_{IF}

Table 6.21: Key Points Summary of Figure 6.17

Point	Param	IF = 30 MHz	dBc
1,3	Pk Pwr	486.5 m, 3.40 dBm	-
2	Pk RSL	495m, -10.59 dBm	14.0
4	Pk DSL	4225 Hz, -10.23 dBm	13.6
5	Spur 1	3575 Hz, -13.49 dBm	16.9
6	Spur 2	4500 Hz, -15.85 dBm	19.3
Point	Param	IF = 60 MHz	dBc
1,3	Pk Pwr	486.5 m, 2.74 dBm	-
2	Pk RSL	495m, -11.25 dBm	14.0
4	Pk DSL	4225 Hz, -10.69 dBm	14.1
5	Spur 1	3575 Hz, -6.96 dBm	10.4
6	Spur 2	4575 Hz, -11.52 dBm	14.9
Point	Param	IF = 90 MHz	dBc
1,3	Pk Pwr	486.5 m, 1.61 dBm	-
2	Pk RSL	495m, -12.42 dBm	14.0
4	Pk DSL	4225 Hz, -11.8 dBm	13.4
5	Spur 1	3575 Hz, -3.09 dBm	4.7
6	Spur 2	4575 Hz, -9.95 dBm	11.6

Figure 6.18 is a plot of results in Figure 6.17 without the Doppler correction. After superimposing a sinc function with nulls at the update rate $f_{\Delta a}$, it is clear to see that the changes in spur amplitude are due to how close these spurs are to the nulls. This figure clearly demonstrates that the lower the f_{IF} chosen, the lower the amplitude of the Doppler spectrum spurs. These results support the results in [4].

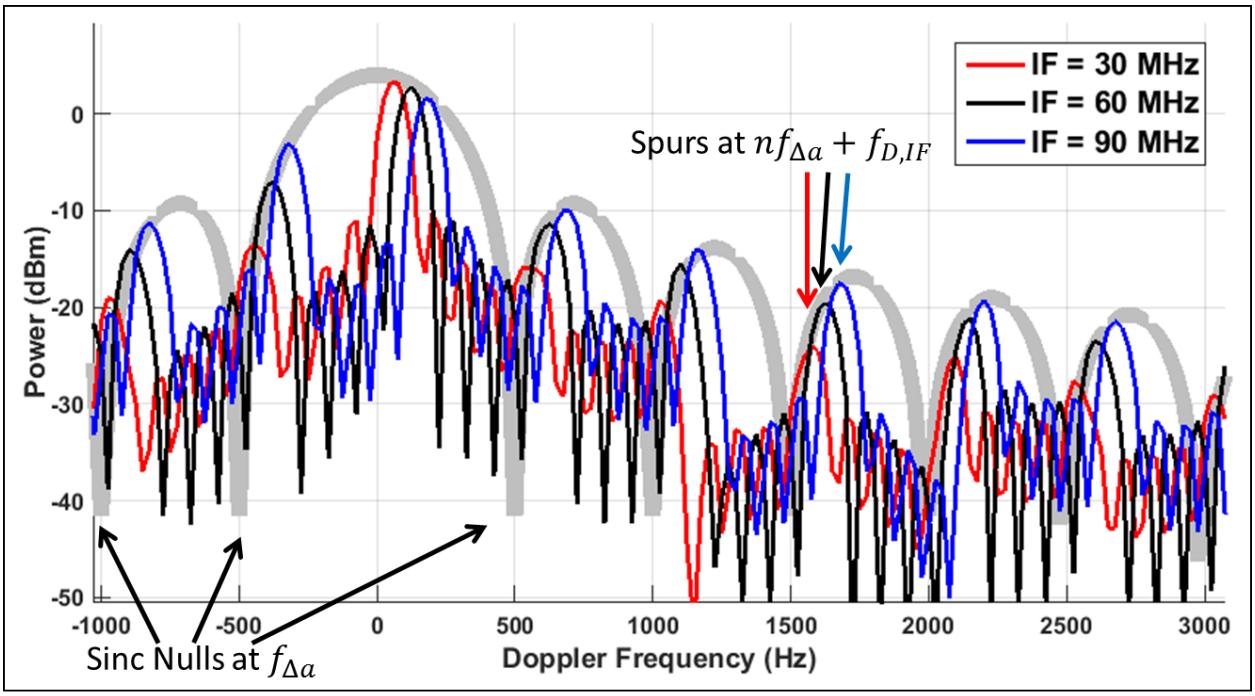

Figure 6.18: Variation of f_{IF} with no Doppler correction superimposed with a sinc funcion with nulls at $f_{\Delta a}$

Notice a worst case exists (not shown) when the IF is equal to $\frac{f_s}{2}$. At that point, the mainlobe of the sinc weighting would contain two equal amplitude peaks, one a the expected Doppler shift $f_{D,IF}$ and one at $-f_{D,IF}$. The remaining Doppler spurs would be at maximum amplitude and corresponding with the peaks of the sinc weighting sidelobes. This worst case scenario corresponds to a memory step change phase shift of 180°

This sinc weighting should be applied to the variation of the velocity results in Section 6.4.1 to better predict the spur amplitudes at any simulated velocity. The work in [4] provides a rigorous mathematical treatment of this result and demonstrates that the sinc weighting is directly related to the limitations on the update rate imposed by the minimum delay step size of the target generator. Recall that in the sampling rate variation in Section 6.6.1, an increase in the sampling rate caused the update rate to increase and the Doppler spur spacing to increase. This would correspond to a broadening of the sinc lobes depicted in Figure 6.18. Further development of these results is left to future work.

6.6.3 Architectural Improvement

This section demonstrates how the QM can be improved by changing the architecture of Chapter 3 as discussed in Appendix **??**. The results in this section all use the base case radar and target parameters of Tables 6.1 and 6.2. The new model is referred to as the Interpolated Model (IM).

First the unwindowed results are plotted in Figure 6.19 and summarized in Table 6.22. The IM results demonstrate significant improvement over the QM in the suppression of the model spurs and closely match those of the NM. The only anomalous frequency is indicated by point 3 in the left subfigure.

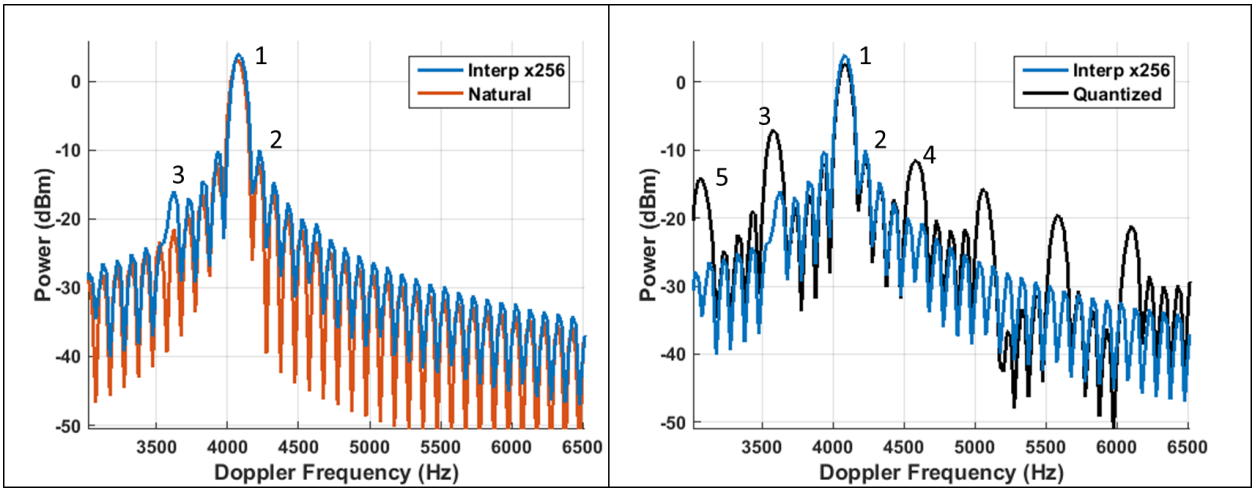

Figure 6.19: Comparison of the Doppler spectrum of the Natural, Quantized, and Interpolated Models

Next, the windowed results are shown in Figure 6.20 and the key points are identified in Table 6.23. The model spurs inherent to the IM are visible as a result of applying a -55 dB Taylor window. While the model spurs are still present, the IM offers 13.67 dB of suppression in the peak model spur relative to the QM (point 2 in Figure 6.20) and a total of 24.7 dBc. The IM spurs also decrease more rapidly than those caused by the QM and are on the level of the NM by the time they are 2000 Hz away from the Doppler frequency. While the windowed IM result does not totally remove the spurious effects near the Doppler frequency, it demonstrates clear superiority to the QM in all cases.

Finally, the interpolation factor was varied. As can be seen in Figure 6.21 and Table 6.24,

Table 6.22: Key Points Summary of Figure 6.19

Point	Param	Interp. x256	dBc
1	Pk Pwr	4075 Hz, 3.93 dBm	-
2	Pk DSL	4225 Hz, -9.98 dBm	13.9
3	Spur 1	3625 Hz, -15.95 dBm	19.9
4	Spur 2	-23 dBm	-
5	Spur 3	-27 dBm	-
Point	Param	Natural	dBc
1	Pk Pwr	4075 Hz, 3.16 dBm	-
2	Pk DSL	4225 Hz, -11.99 dBm	15.2
3	Spur 1	3575 Hz, -21.56 dBm	24.7
4	Spur 2	-23 dBm	-
5	Spur 3	-27 dBm	-
Point	Param	Quantized	dBc
1	Pk Pwr	4075 Hz, 2.74 dBm	-
2	Pk DSL	4225 Hz, -10.69 dBm	13.4
3	Spur 1	3575 Hz, -6.96 dBm	9.7
4	Spur 2	4575 Hz, -11.52 dBm	14.3
5	Spur 3	3075 Hz, -14.18 dBm	16.9

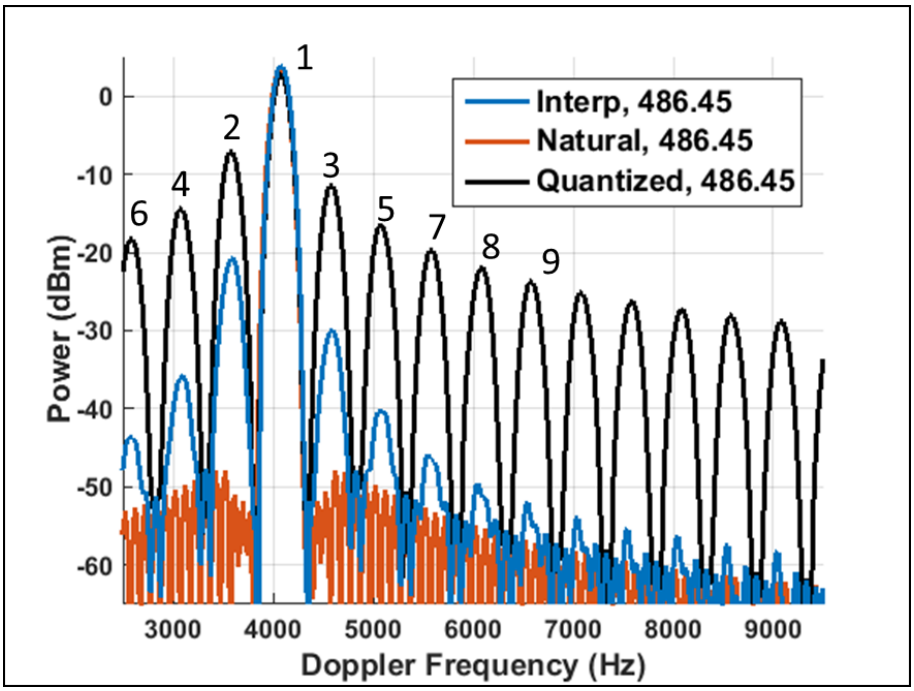

Figure 6.20: Windowed Comparison of Natural, Quantized, and Interpolated Models

Table 6.23: Key Points Summary of Figure 6.20

Point	Parameter	Interp. x256	dBc
1	Peak Power	4075 Hz, 4.22 dBm	-
2	Spur 1	3600 Hz, -20.44 dBm	24.7
3	Spur 2	4600 Hz, -29.66 dBm	33.9
4	Spur 3	3100 Hz, -35.53 dBm	39.8
5	Spur 4	5075 Hz, -39.99 dBm	44.2
Point	Parameter	Natural	dBc
1	Peak Power	4075 Hz, 3.84 dBm	-
2	Spur 1	-50.78 dBm	54.6
3	Spur 2	-50.1 dBm	53.9
4	Spur 3 -51.84 dBm	55.7	
5	Spur 4	-52 dBm	55.8
Point	Parameter	Quantized	dBc
1	Peak Power	4075 Hz, 3.04 dBm	-
2	Spur 1	3575 Hz, -6.77 dBm	9.8
3	Spur 2	4575 Hz, -11.12 dBm	14.2
4	Spur 3	3075 Hz, -14.06 dBm	17.1
5	Spur 4	5075 Hz, -16.17 dBm	19.2

increasing the interpolation factor has zero impact on the 500 Hz spacing spurs near the Doppler frequency. Furthermore, this plot exposes a secondary set of spurs caused by the IM. These spurs are spaced between 4000 Hz and 4025 Hz, which is approximately equal to the simulated Doppler frequency. The spacing is a factor of eight greater than that of the Quantized model spurs. These secondary effect spurs are further suppressed as the interpolation factor increases.

The inability of the interpolation model to suppress the sidelobes closest to the mainlobe is an effect of the implementation discussed in Appendix **??**. If the bandwidth existed to execute a classic interpolation method, these spurs would have been completely reduced.

In summary, the IM offers great improvement over the QM with the minimal penalties discussed in Appendix **??**. In the case of the non-windowed results in Figure 6.19, it is clear that the IM and NM have almost equal performance.

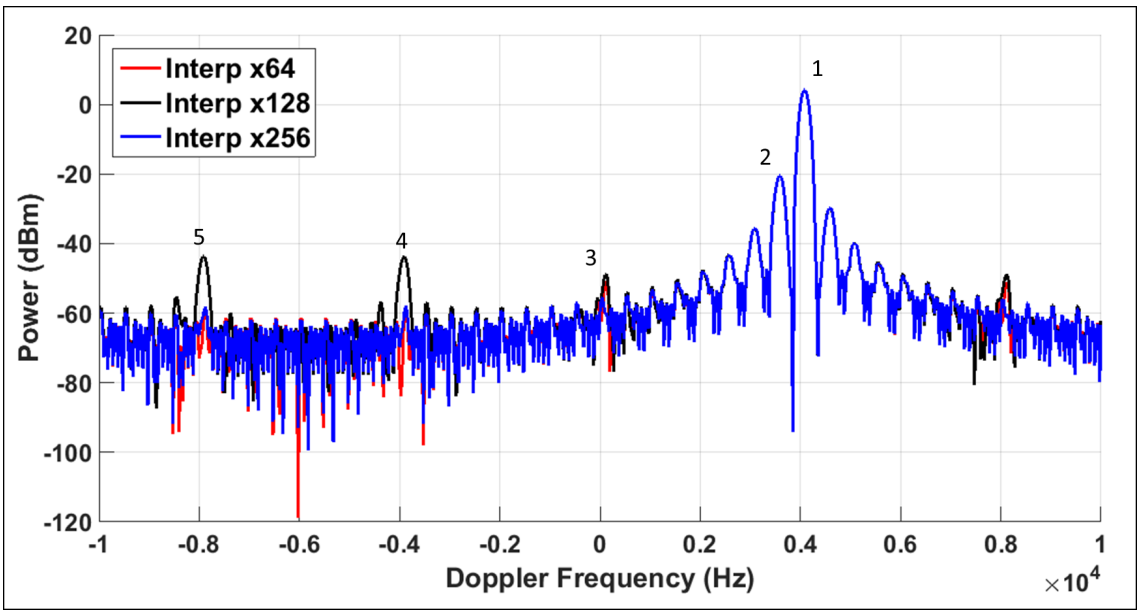

Figure 6.21: Windowed Comparison of Interpolation Factor

Table 6.24: Key Points Summary of Figure 6.21

Point	Parameter	Interp. x64	dBc
1	Pk Pwr	4075 Hz, 4.22 dBm	-
2	QM Spur 1	3600 Hz, -20.44 dBm	24.7
3	IM Spur 1	125 Hz, -48.61 dBm	52.8
4	IM Spur 2	-3900 Hz, -43.74 dBm	48.0
5	IM Spur 3	-7925 Hz, -43.63 dBm	47.8
Point	Parameter	Interp. x128	dBc
1	Pk Pwr	4075 Hz, 4.22 dBm	-
2	QM Spur 1	3600 Hz, -20.44 dBm	24.7
3	IM Spur 1	125 Hz, -50.81 dBm	55.0
4	IM Spur 2	-3875 Hz, -58.77 dBm	63.0
5	IM Spur 3	-7875 Hz, -58.98 dBm	63.2
Point	Parameter	Interp. x256	dBc
1	Pk Pwr	4075 Hz, 4.22 dBm	-
2	QM Spur 1	3600 Hz, -20.44 dBm	24.7
3	IM Spur 1	50 Hz, -55.52 dBm	59.7
4	IM Spur 2	-3875 Hz, -58.02 dBm	62.2
5	IM Spur 3	-7875 Hz, -58.98 dBm	63.2

6.7 HDL Comparison

While all of the previous results were executed using purely Simulink and Matlab based models, the following results are gathered by comparing the Simulink QM with the HDL implementation

of the QM, referred to as the HDL Model (HDLM). The HDLM was designed in Xilinx's Vivado tool set and imported into Simulink for direct comparison with identical input data. Simulink facilitates a bit-true simulation using Xilinx logic blocks with easy access to the superior spectral analysis tools provided by Matlab. The simulation time for this bit-true simulation is excessive, an unfortunate result that prompted the creation of the QM for easy comparison of results with the NM. The HDLM brings the previous results closer to physical reality by including all of the negative effects of the algorithm including latency, numerical precision effects, the Hilbert Transform filter, and the DDS.

The results in Figure 6.22 and Table 6.25 generally show great agreement between the QM and HDLM. The significant difference is elevation of the Doppler sidelobes to the left of the main lobe, but this sidelobe elevation does not persist across the band.

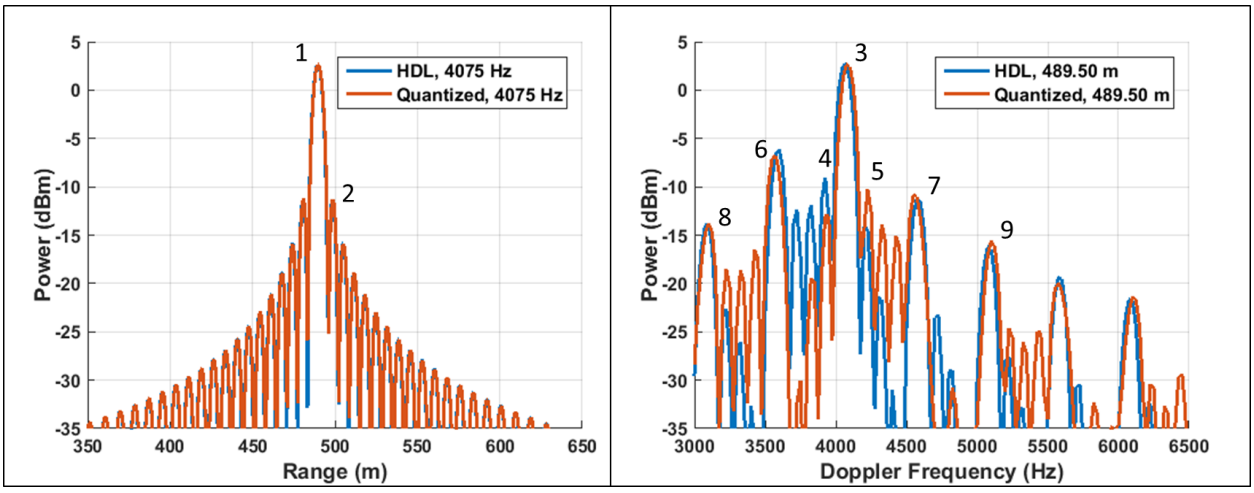

Figure 6.22: Comparison of Quantized and HDL Models

Table 6.25: Key Points Summary of Figure 6.22

Point	Parameter	QM	dBc	HDLM	dBc
1	Peak Power	4075 Hz, 2.67 dBm	-	4075 Hz, 2.67 dBm	-
2	Pk RSL	498.7, -11.27 dBm	13.94	498.7, -11.27 dBm	13.94
3	Pk DSL	4225 Hz, -10.26 dBm	13.02	3975 Hz, -9.018 dBm	11.78
4	Spur 1	3575 Hz, -6.78 dBm	9.54	3600 Hz, -6.14 dBm	8.9
5	Spur 2	4550 Hz, -10.80 dBm	13.56	4575 Hz, -11.13 dBm	13.89

This model does not include limitations due to clock speed, routing, jitter and sampling effects.

The large design margin documented in the summary in Section 5.4.4 however, suggests that the physical realities of the hardware implementation should not be a limiting factor. Furthermore, the simulation was completed with the minimum additive noise associated with the attenuator setting $A = 21$ dB, but more significant noise is expected to have a negligible effect as was exhibited in previous Matlab models. These preliminary results suggest that the Matlab QM is an accurate representation of the HDL that can be used to verify future changes to the algorithm.

6.8 Hardware Test Results

Finally, the FPGA on the KC705 development board was programmed with the firmware design described in Section 5.1 and a test was executed with the hardware configuration shown in Figure 6.23.

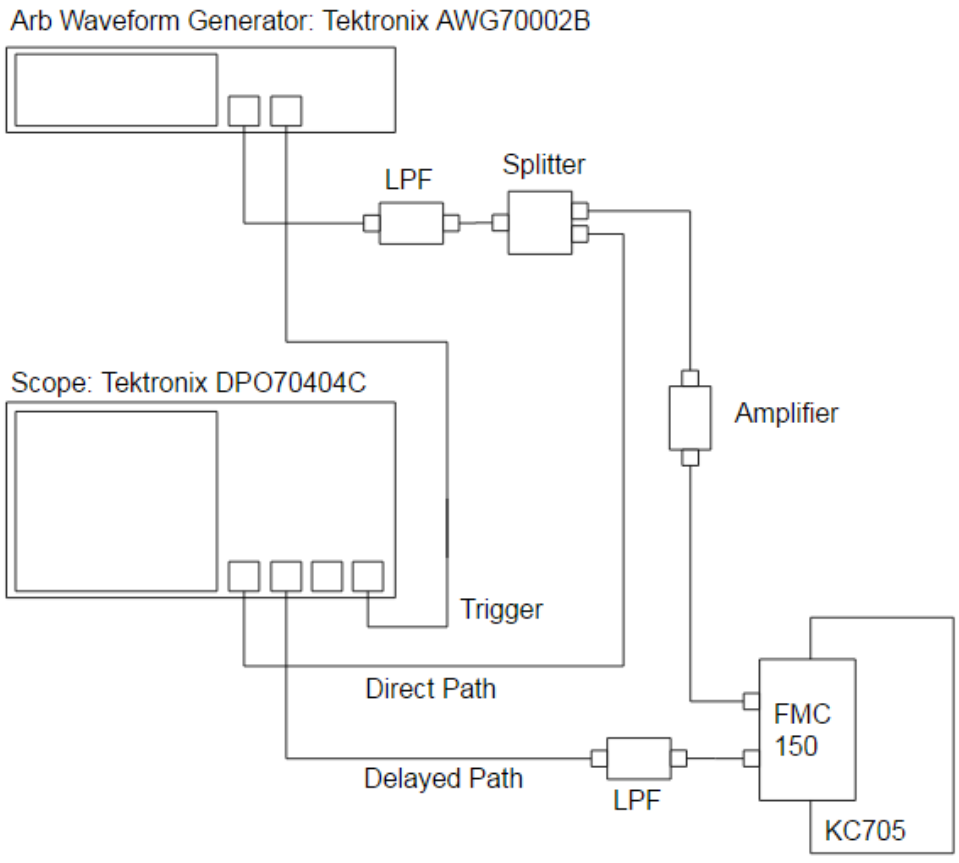

Figure 6.23: Hardware Test Configuration

A Tektronix arbitrary waveform generator (AWG70002A) was used to generate the representative radar waveform. The AWG output was low pass filtered then passed through a splitter. One channel of the splitter was fed into Channel 1 of a Tektronix oscilloscope (DPO70404C) to serve as a reference waveform. The other path was amplified and fed to the FMC150 card ADC and the KC705 for manipulation. After reconstruction by the FMC150 DAC and low pass filtering, this delayed path was fed into Channel 2 of the oscilloscope.

The oscilloscope's data buffer capacity is insufficient to store all of the data samples associated with the total simulation duration. Therefore, the significant subset of the data was collected using the oscilloscope's fast frame mode. A trigger signal produced by the AWG was used to initiate the capture of a fixed number of samples after the trigger event that would include the delay applied to the radar waveform.

Figure 6.24 demonstrates the result of hardware emulation of a synthetic target with an inbound velocity of 305 m/s, or the baseline target from Section 6.3.2. This figure compares the Doppler spectrum of the hardware data with that of the quantized model.

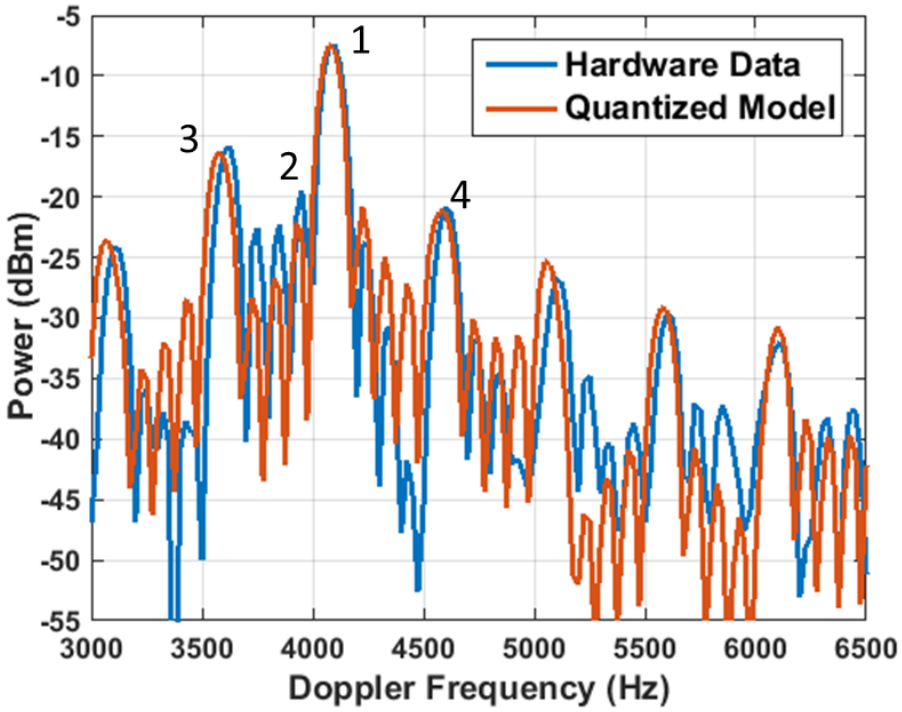

Figure 6.24: Comparison of Hardware results with Quantized Model

The high level of agreement between the two traces in Figure 6.24 provide further evidence that the hardware simulations presented above are representative of the result of the hardware implementations. Furthermore, this result yields the encouraging conclusion that the HDL design provides effective simulation of a radar target.

6.9 Results Summary

The previous simulations were divided into three sections. The first considered variations of the target in Section 6.4, next, variations of the radar in Section 6.5, and finally, variations of the target generator in Section 6.6. All of these sections showed great agreement in the range dimension and the presence of model-induced spurs in the Doppler spectrum. These Doppler spurs are often higher than the peak Doppler sidelobe and may be a concern based on the radar's processing. Furthermore, it was confirmed that superposition holds with the synthetic targets generated by the quantized model.

The result of the target variation simulations showed that the relative height of the spurs in the Doppler spectrum are dependent on the Doppler frequency. This is a significant result because it means that even with a fixed set of radar and target generator parameters, the undesirable effects due to Doppler are inconsistent and therefore will be difficult to characterize in a testing application.

Varying the radar parameters resulted in predictable changes in the response to the constant target and target generator settings. This satisfying result confirms that the target generator performance and quantized model are independent of the radar. Furthermore, this section exposed the Doppler spurs as immune to the suppression via windowing, a result that agrees with the work in [4]. This conclusion emphasizes the need to develop a method for suppressing the spurs so that this target generator is capable of serving as a test platform for radars with a large amount of dynamic range. Finally, the result of the windowing and BPSK experiments confirmed that the characteristics of the target generator remain constant in the face of modifications to the radar transmission

and processing scheme.

Finally, the changes to the target generator architecture demonstrated the effectiveness of some design trade offs. First, increasing the target generator sampling rate effectively increased the Doppler spur spacing and a 4x sampling rate increase caused the relative power in the largest spur to go from 10 dBc to 24 dBc - a 14 dB improvement. Next, decreasing the target generator's IF resulted in a decrease in spur amplitude. A 50 % decrease in the IF suppressed the largest spur by 7 dB. Finally, the results of the interpolation algorithm in Appendix **??** were demonstrated that reduced the largest magnitude sidelobe by 20 dB in the non-windowed results.

Chapter 7

Conclusions

The goal of this thesis is to analyze the effectiveness of digital target generators for high fidelity target simulations. Conclusions have been drawn by comparing digital architectures to methods that rely on physical delay media in Chapter 3 as well as via simulations that vary the radar and target generator parameters in Chapter 6 in an effort to isolate where the key performance boundaries lie.

In summary, it was concluded in Chapter 6 and throughout this work that the primary short coming of moving target simulations is founded in the minimum delay step size. This impact of the delay step size manifests in limitations to the range rate as well as inducing a periodic phase discontinuity at the range update rate.

Improvements to the overall output signature can be realized via sample rate increases, minimizing the IF, and interpolation methods that minimize the phase discontinuity and the minimum delay step size. The interpolation method outlined in Appendix **??** successfully suppressed the spurious artifacts present in the non-windowed Doppler spectrum by 19 dB.

7.1 Future Work

Many opportunities for future work have been exposed by the results of this thesis. One opportunity would be to vary the radar processing and apply a detection algorithm to see how the non-ideal

nature of the Doppler spectrum impacts more sophisticated radar processing schemes. Similar analysis could be applied to determine the effects of these models on less sophisticated lower fidelity processing as well.

Another area to explore would be further refinement of the interpolation algorithm in Appendix **??** to improve upon the suppression of the spurs in the Doppler spectrum. While the results of that work were significant to improvement of the appearance of the Doppler spectrum, it should be possible to entirely reject the spurs via interpolation as the IM result becomes more and more similar to the QM.

Further refinement of the implementations here could be achieved by reduction of bias. There are small inconsistencies in the measured range delay to the target and latency through various algorithms that have not been completely characterized. These discrepancies were attributed to the quantization effects of the QM and the added noise. The results and characteristics of the various simulated targets generally show good agreement with the natural model, but an exhaustive analysis should be performed to verify the source of the inconsistency.

This work was limited to analyzing targets with a constant radial velocity. Further work remains in simulating a targets with varying range rates as the spectral effects in those cases will likely be different than those shown. There are other ways that the fidelity of the target's location in space could be improved in the HDL model specifically. In the implementation discussed here, the counter for the update rate begins incrementing from zero at the start of the simulation. It should be possible, however, to start the update rate at an offset, so that range changes occur at different points in time in the simulation. This would require a more complicated computation of the Doppler correction frequency, but would reduce the discrepancy in total motion over the simulation between the IM and the quantized range model.

Furthermore, conclusions drawn in the analysis of varying the target generator IF suggest that the Doppler spectrum spurs could be completely suppressed with the use of baseband IQ sampling in the target generator. This method would require exact knowledge of the radar operating frequency to complete the down conversion perfectly, but it is likely that any spurs present due to

a slight inaccuracy in the frequency measurement would sill be suppressed significantly. This is an area for future research. As is investigating the spurious behavior of a simulated target with non-constant velocity.

Finally, the design in Chapter 5 has not yet been implemented on the KC705 board it was targeted for. Testing of the HDL design in hardware will yield a new set of challenges and add a level of fidelity to the results presented here. These results would provide a strong indication as to whether this design and the improved architecture described in Appendix **??** would be appropriate for use in a test environment. This hardware implementation would provide further opportunity for physical measurement of the system latency and other errors to verify the theoretical metrics provided in Chapters 4 and 5.

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Appendix A

Analog Circuit Design Verification

A.1 Noise Power Calculations

Noise power is a significant calculation required so that the simulations in Chapter 6 are representative of the system and hardware presented in Chapter 5. A visual summary of the signal levels through the system is presented in Figure A2 and Tables A2, A3, and A4 provide detailed intermediate calculations. The process used to arrive at these results is described in the following.

The output noise power of a component, $P_{n,out}$, is computed using Equation A.1 where G is the component gain, $k = 1.38x10^{-23}$ is Boltzmann's constant, T_{in} is the input noise temperature, T_e is the equivalent input noise temperature, $T_{out} = G(T_e + T_{in})$ is the output noise temperature, and B is the noise equivalent bandwidth [30] [39].

$$P_{n,out} = kG(T_{in} + T_e)B = kT_{out}B \tag{A.1}$$

The output noise temperature of a system, or cascade of components as shown in Figure A.1, can be computed using a superposition of the contributions from the individual noise sources in the chain. Equation A.2 provides a calculation for T_{out} in the context of the diagram in Figure A.1 [39].

$$\begin{aligned} T_{out} &= ((T_{in} + T_{e1})G_1G_2\cdots G_n) + (T_{e2}G_2\cdots G_n) + \cdots + (T_{en}G_n) \\ &= T_{out1} + T_{out2} + \cdots + T_{outn} \end{aligned} \tag{A.2}$$

Each component in the chain contributes thermal noise and following the notation in Figure A.1, each component in the chain can be modeled as an ideal (noiseless) component with an external noise source.

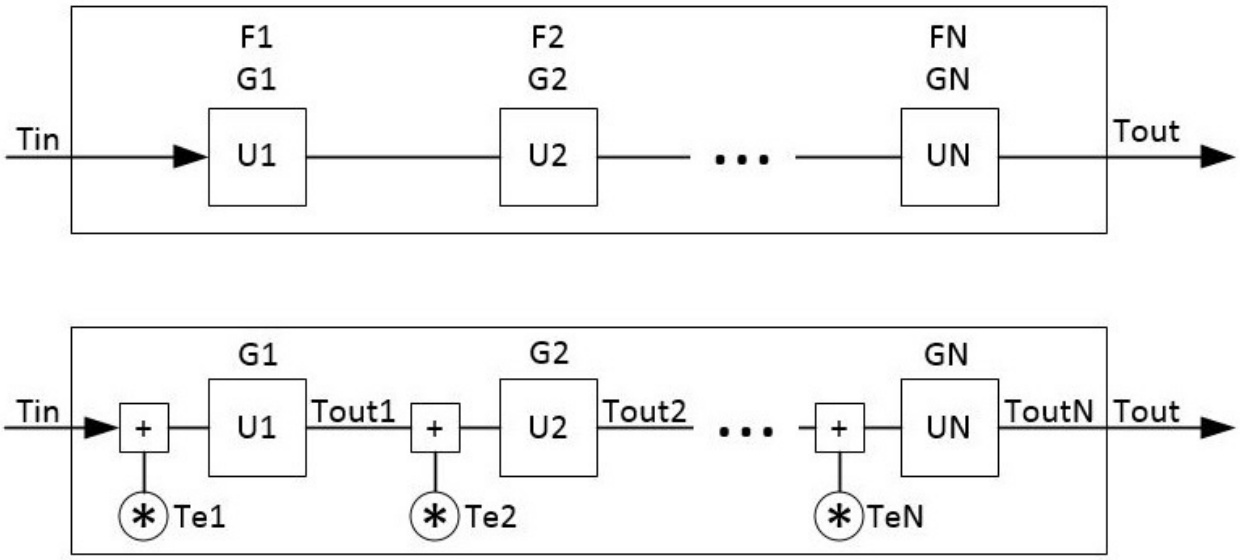


Figure A.1: System Approach to Noise Temperature Calculation [39]

Each value of T_e is computed using Equation A.3 by using the device's noise figure F. This computation is required because F commonly appears on product data sheets while T_e does not.

$$T_{ei} = (F_i - 1)290 \tag{A.3}$$

The remaining unknowns in Equations A.1 and A.2 are the input noise temperature and the bandwidth. The noise equivalent bandwidth is set equal to the bandwidth limiting component in the chain in the case of the receiver this is typically equal to the IF bandwidth. The input noise temperature is determined by the system definition. In the case of a free space receiver, $T_{in} = 290$ K. In all other cases, however, the input noise temperature to the cascade in Figure A.1 is simply

the output noise temperature of the device preceding the chain. In the case considered in Chapter 5 and Figure A2, the first device is a DAC.

Equation 4.3 computes the variance of the quantization noise process σ^2_{ADC}. Assuming the device is designed to be used in a 50-ohm system, the quantization noise power can be computed in Equation A.4 and the equivalent noise temperature associated with this value (alternatively, the output noise temperature of the DAC and the input noise temperature to the system) is computed in Equation A.5.

$$P_{n,DAC} = \frac{\sigma^2_{DAC}}{50} = \frac{V_p^2}{3 * 2^{2N}} \tag{A.4}$$

$$T_{e,DAC} = T_{in} = \frac{\sigma^2_{DAC}}{50kB} \tag{A.5}$$

Finally, these values can be used to compute T_{out} and subsequently $P_{n,out}$. Once $P_{n,out}$ is known, the system's output SNR can be computed. In the case of the radar receiver, conclusions can be drawn about whether the signal processing gain is sufficient to overcome the SNR associated with the furthest targets of interest as discussed in Section 2.2.2.

This method be applied to the system in Figure 5.3 to yield the results in Tables A2 and A3. A detailed version of Figure 5.3 appears in Figure A2. All of the components in these figures have known gain and noise figure values, so all of the equivalent noise temperatures can be found. The output noise temperature of each of the ADC and DAC are summarized in Table A.1 and detailed calculations are shown in Table A4.

Table A.1: ADC and DAC Output Noise Temperatures

Ref. Des.	Description	V_p	N	T_{out}
U1	Radar DAC	0.5	12	71986
U11	TG ADC	1	12	287945
U12	TG DAC	0.5	16	281
U24	Radar ADC	0.5	12	71986

The noise associated with the target generator's digital kernel does not follow the methods described thus far and therefore the noise temperature at the input to U13 requires a slightly different

approach. The value for T_{inU13}, (which is also the output noise temperature from the target generator transmitter into the radar receiver portion of the chain), is computed as shown in Equation A.6. The assumption is made that the algorithm in the digital kernel is simply a feed through from the ADC to the DAC with an ideal (noiseless) attenuation of $G_{ALG} = 6$ dB to account for the mismatch between the difference in V_p for U11 and U12 as indicated in Table A.1. The target generator ADC has more bits of precision than the TG DAC, so sufficient bits exist to represent the new signal and this decrease in power will add no noise. Additive noise from the quantization error associated with the ADC and DAC will contribute to the noise power out. Therefore the resulting input noise temperature to the first component in the target generator transmitter is computed in Equation A.6.

$$T_{inU13} = T_{outU12} = \frac{(T_{outU10} + T_{e,TgADC})}{4} - T_{e,TgDAC} \tag{A.6}$$

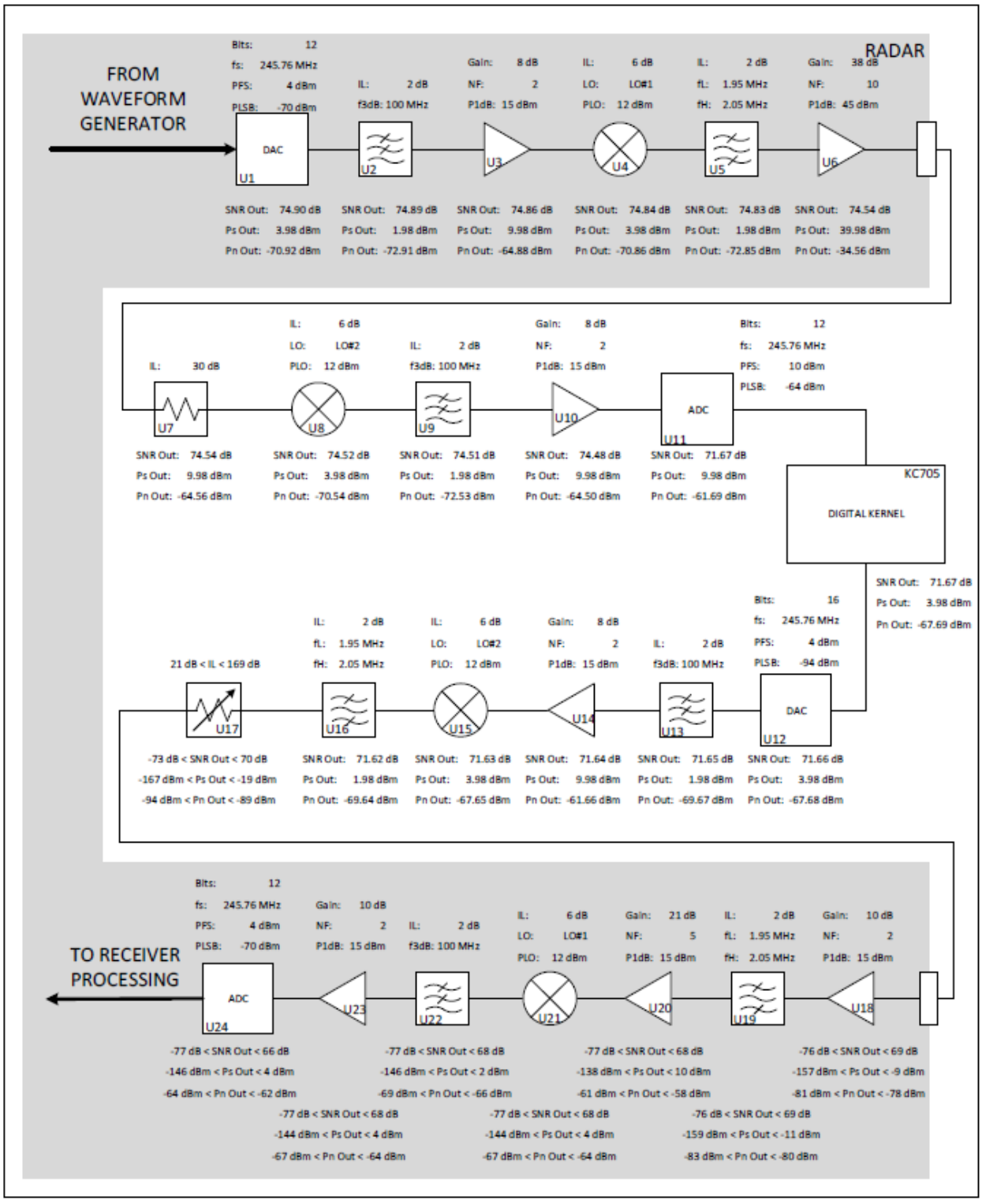
Finally the input noise temperature to the radar receiver (T_{inU18}) can take on a range of values based on the setting of the switched attenuator. All attenuation settings of 55 dB or greater result in a target generator output noise temperature of 290 K. This is significant because it marks the point at which the radar receiver noise dominates and the target generator output SNR becomes truly representative of a free space target at the associated range.

The equivalent noise temperature for the radar receiver T_{eRX}, can be found by manipulating Equation A.2 when N = 1 and inserted into Equation A.3 to compute the receiver noise figure F_{RX}.

$$F_{RX} = \frac{\frac{T_{outRX}}{G_{RX}} - T_{inRx}}{290} - 1 = \frac{T_{eRX}}{290} - 1 \tag{A.7}$$

The following tables and figures document and summarize the noise calculations. First the detailed system block diagram with intermediate signal levels appears in Figure A2. Next, Table A2 shows the calculations for the minimum attenuation setting so that the signal power meets the radar ADC full scale range, Table A3 shows the calculations for the attenuation setting associated with the simulations in Chapter 6 and Table A4 reports the details associated with the quantization noise power calculations for the ADC and DAC.

Figure A.2: Detailed power tracking through the block diagram of the system described in Chapter 5.



Description	Gain (dB)	Gain	ins loss (dB)	NF	Equivalent Noise Temp	Output Noise Temp	Output Noise Power (W)	Output Noise Power (dBm)	Signal Power Out (W)	Signal Power Out (dBm)	SNR (dB)
Radar and Target Generator											
RDR DAC						**71986.29**		-70.03	0.0025	3.98	74.01
lpf	-2	0.6310	2	1.58	170	45527	6.28E-11	-72.02	0.0016	1.98	74.00
amp	8	6.3096	-8	2.00	289	289079	3.99E-10	-63.99	0.0100	9.98	73.97
mixer	-6	0.2512	6	3.98	865	72831	1.01E-10	-69.98	0.0025	3.98	73.96
bpf	-2	0.6310	2	1.58	170	46060	6.36E-11	-71.97	0.0016	1.98	73.95
HPA	38	6310	-38	10	2610	307086702	4.24E-07	-33.73	9.9527	39.98	73.71
attenuator	-30	0.0010	30	1000	289710	307087	4.24E-10	-63.73	0.0100	9.98	73.71
mixer	-6	0.2512	6	3.98	865	77354	1.07E-10	-69.72	0.0025	3.98	73.70
bpf	-2	0.6310	2	1.58	170	48914	6.75E-11	-71.71	0.0016	1.98	73.69
amp	8	6.3096	-8	2.00	289	310448	4.28E-10	-63.68	0.0100	9.98	73.66
TG ADC (12 bit)	0	1	0	1	287945	598393	8.26E-10	-60.83	0.0100	9.98	70.81
Algorithm	-6	0.2512	6			150309	2.07E-10	-66.83	0.0025	3.98	70.81
TG DAC (16 bit)	0	1	0	1	281	**150591**	2.08E-10	-66.82	2.50E-03	3.98	70.80
bpf	-2	0.6310	2	1.58	170	95123	1.31E-10	-68.82	1.58E-03	1.98	70.80
amp	8	6.3096	-8	2.00	289	602009	8.31E-10	-60.81	9.95E-03	9.98	70.78
mixer	-6	0.2512	6	3.98	865	151435	2.09E-10	-66.80	2.50E-03	3.98	70.78
bpf	-2	0.6310	2	1.58	170	95656	1.32E-10	-68.79	1.58E-03	1.98	70.77
variable atten	-21	0.0079	21	1.26E+02	3.62E+04	1048	1.45E-12	-88.40	1.25E-05	-19.02	69.38
lna	10	10	-10	2.00	289	13361	1.84E-11	-77.34	1.25E-04	-9.02	68.32
bpf	-2	0.6310	2	1.58	170	8538	1.18E-11	-79.29	7.91E-05	-11.02	68.27
lna	21	125.8925	-21	5.00	1160	1220846	1.68E-09	-57.73	9.95E-03	9.98	67.71
mixer	-6	0.2512	6	3.98	865	306880	4.23E-10	-63.73	2.50E-03	3.98	67.71
lpf	-2	0.6310	2	1.58	170	193735	2.67E-10	-65.73	1.58E-03	1.98	67.71
amp	2	1.5849	-2	0.63	-107	306880	4.23E-10	-63.73	2.50E-03	3.98	67.71
RDR ADC (12 bit)				WITH RADAR ADC QNOISE		378866	5.23E-10	**-62.82**	2.50E-03	3.98	66.80
						290					
Free Space Receiver											
lna	10	10	-10	2.00	289	5786	7.99E-12	-80.98	1.25E-04	-9.02	71.96
bpf	-2	0.6310	2	1.58	170	3758	5.19E-12	-82.85	7.91E-05	-11.02	71.83
lna	21	125.8925	-21	5.00	1160	619128	8.54E-10	-60.68	9.95E-03	9.98	70.66
mixer	-6	0.2512	6	3.98	865	155735	2.15E-10	-66.68	2.50E-03	3.98	70.66
lpf	-2	0.6310	2	1.58	170	98369	1.36E-10	-68.67	1.58E-03	1.98	70.65
amp	2	1.5849	-2	0.63	-107	155735	2.15E-10	-66.68	2.50E-03	3.98	70.66
RDR ADC (12 bit)				WITH RADAR ADC QNOISE		227721	3.14E-10	**-65.03**	2.50E-03	3.98	69.01

Table A.2: Detailed signal level calculations when the attenuator in the target generator transmitter is set to 21 dB; the level associated with the full scale range of the radar ADC.

Description	Gain (dB)	Gain	ins loss (dB)	NF	Equivalent Noise Temp	Output Noise Temp	Output Noise Power (W)	Output Noise Power (dBm)	Signal Power Out (W)	Signal Power Out (dBm)	SNR (dB)
Radar and Target Generator											
RDR DAC						**71986.29**		-70.03	0.0025	3.98	74.01
lpf	-2	0.6310	2	1.58	170	45527	6.28E-11	-72.02	0.0016	1.98	74.00
amp	8	6.3096	-8	2.00	289	289079	3.99E-10	-63.99	0.0100	9.98	73.97
mixer	-6	0.2512	6	3.98	865	72831	1.01E-10	-69.98	0.0025	3.98	73.96
bpf	-2	0.6310	2	1.58	170	46060	6.36E-11	-71.97	0.0016	1.98	73.95
HPA	38	6310	-38	10	2610	307086702	4.24E-07	-33.73	9.9527	39.98	73.71
attenuator	-30	0.0010	30	1000	289710	307087	4.24E-10	-63.73	0.0100	9.98	73.71
mixer	-6	0.2512	6	3.98	865	77354	1.07E-10	-69.72	0.0025	3.98	73.70
bpf	-2	0.6310	2	1.58	170	48914	6.75E-11	-71.71	0.0016	1.98	73.69
amp	8	6.3096	-8	2.00	289	310448	4.28E-10	**-63.68**	0.0100	9.98	73.66
TG ADC (12 bit)	0	1	0	1	287945	598393	8.26E-10	**-60.83**	0.0100	9.98	70.81
Algorithm	-6	0.2512	6			150309	2.07E-10	-66.83	0.0025	3.98	70.81
TG DAC (16 bit)	0	1	0	1	281	**150591**	2.08E-10	-66.82	2.50E-03	3.98	70.80
bpf	-2	0.6310	2	1.58	170	95123	1.31E-10	-68.82	1.58E-03	1.98	70.80
amp	8	6.3096	-8	2.00	289	602009	8.31E-10	-60.81	9.95E-03	9.98	70.78
mixer	-6	0.2512	6	3.98	865	151435	2.09E-10	-66.80	2.50E-03	3.98	70.78
bpf	-2	0.6310	2	1.58	170	95656	1.32E-10	-68.79	1.58E-03	1.98	70.77
variable atten	-119	0.0000	119	7.94E+11	2.30E+14	290	4.00E-13	-93.98	1.99E-15	-117.02	-23.04
lna	10	10	-10	2.00	289	5786	7.99E-12	-80.98	1.99E-14	-107.02	-26.04
bpf	-2	0.6310	2	1.58	170	3758	5.19E-12	-82.85	1.25E-14	-109.02	-26.17
lna	21	125.8925	-21	5.00	1160	619128	8.54E-10	-60.68	1.58E-12	-88.02	-27.34
mixer	-6	0.2512	6	3.98	865	155735	2.15E-10	-66.68	3.96E-13	-94.02	-27.34
lpf	-2	0.6310	2	1.58	170	98369	1.36E-10	-68.67	2.50E-13	-96.02	-27.35
amp	2	1.5849	-2	0.63	-107	155735	2.15E-10	-66.68	3.96E-13	-94.02	-27.34
RDR ADC (12 bit)				WITH RADAR ADC QNOISE		227721	3.14E-10	**-65.03**	3.96E-13	-94.02	-28.99
Free Space Receiver						290					
lna	10	10	-10	2.00	289	5786	7.99E-12	-80.98	1.99E-14	-107.02	-26.04
bpf	-2	0.6310	2	1.58	170	3758	5.19E-12	-82.85	1.25E-14	-109.02	-26.17
lna	21	125.8925	-21	5.00	1160	619128	8.54E-10	-60.68	1.58E-12	-88.02	-27.34
mixer	-6	0.2512	6	3.98	865	155735	2.15E-10	-66.68	3.96E-13	-94.02	-27.34
lpf	-2	0.6310	2	1.58	170	98369	1.36E-10	-68.67	2.50E-13	-96.02	-27.35
amp	2	1.5849	-2	0.63	-107	155735	2.15E-10	-66.68	3.96E-13	-94.02	-27.34
RDR ADC (12 bit)				WITH RADAR ADC QNOISE		227721	3.14E-10	**-65.03**	3.96E-13	-94.02	-28.99

Table A.3: Detailed signal level calculations when the attenuator in the target generator transmitter is set to 119 dB; the level associated wth the free space loss of a target at 487 m.

Radar ADC and DAC Calcs								
RDR DAC Vpp	1				RDR ADC Vpp	1		
RDR DAC Vp	0.5				RDR ADC Vp	0.5		
RDR DAC FS Vrms	0.354				RDR ADC FS Vrms	0.354		
FS P (dBm)	3.979				FS P (dBm)	3.979		
FS P (W)	0.0025				FS P (W)	0.0025		
RDR DAC Bits	12				RDR ADC Bits	12		
RDR DAC SNR	74.01				RDR ADC SNR	74.01		
RDR DAC LSB Vp	2.44E-04				RDR ADC LSB Vp	2.44E-04		
LSB Vrms	7.04773E-05				LSB Vrms	7.04773E-05		
LSB P (dBm)	-70.03				LSB P (dBm)	-70.03		
LSB P (W)	9.93E-11				LSB P (W)	9.93E-11		
Te	58582.59				Te	58582.59		
T	290	K			T	290	K	
k	1.38E-23				k	1.38E-23		
B	1.00E+08	Hz			B	1.00E+08	Hz	
BDAC	1.23E+08	Hz			BADC	122880000	Hz	
kTeb (noise power)	9.93E-11		-70.03	dBm	kTeb (noise power)	9.93E-11	-70.03	dBm
kT (noise spec dens)	4.00E-21		-173.98	dBm/Hz	kT (noise spec dens)	4.00E-21	-173.98	dBm/Hz
kTB (noise power)	4.92E-13		-93.08	dBm	kTB (noise power)	4.92E-13	-93.08	dBm
Target Gen ADC and DAC Calcs								
TG ADC Vpp	2				TG DAC Vpp	1		
TG ADC Vp	1				TG DAC Vp	0.5		
TG ADC FS Vrms	0.707				TG DAC FS Vrms	0.354		
FS P (dBm)	10				FS P (dBm)	3.979		
FS P (W)	0.01				FS P (W)	0.0025		
TG ADC Bits	12				TG DAC Bits	16		
TG ADC SNR	74.01				TG DAC SNR	98.09		
TG ADC LSB Vp	4.88E-04				TG DAC LSB Vp	1.53E-05		
LSB Vrms	0.000140955				LSB Vrms	4.40483E-06		
LSB P (dBm)	-64.01				LSB P (dBm)	-94.11		
LSB P (W)	3.97E-10				LSB P (W)	3.88E-13		
Te	234330.36				Te	228.84		
T	290	K			T	290	K	
k	1.38E-23				k	1.38E-23		
B	1.00E+08	Hz			B	1.00E+08	Hz	
BADC	1.23E+08	Hz			BDAC	1.23E+08	Hz	
kTeb (noise power)	3.97E-10		-64.01	dBm	kTeb (noise power)	3.88E-13	-94.11	
kT (noise spec dens)	4.00E-21		-173.98	dBm/Hz	kT (noise spec dens)	4.00E-21	-173.98	
kTB (noise power)	4.92E-13		-93.08	dBm	kTB (noise power)	4.92E-13	-93.08	

Table A.4: Detailed calculations of the ADC and DAC parameters.