Josephson Junctions with Tunnel Barriers Grown Via *In Situ* Atomic Layer Deposition

By

Alan J. Elliot

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Chairperson: Judy Wu

____

Hsin-Ying Chiu

____

Siyuan Han

____

Karen Nordheden

____

Hui Zhao

Date Defended: December 12, 2014

The Dissertation Committee for Alan J. Elliot
certifies that this is the approved version of the following dissertation:

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Chairperson: Judy Wu

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Abstract

Since the 1970's, silicon technology has increased processing power by increasing the density of silicon transistors according to Moore's Law. However, silicon transistor feature sizes are approaching a minimum size limit, and a new paradigm is required to continue progress. Quantum computing is a promising paradigm that relies on the entanglement of macroscopic quantum objects, called qubits, to perform calculations. Josephson junction (JJ) based qubits are a promising candidate for the implementation of quantum computers. However, JJ qubits have suffered from poor coherence. A major source of decoherence in JJ qubits is two-level fluctuators in the insulating materials of the JJ circuit, particularly oxygen vacancies and interstitials in the thermally oxidized tunnel barrier. In order to realize the full potential of JJ qubits, an alternative method to thermal oxidation must be found for tunnel barrier growth.

This work explores using atomic layer deposition (ALD) for the growth of ultrathin (~ 1 nm) tunnel barriers in JJs. A unique thin film deposition tool was built which integrates ultra-high vacuum sputtering with ALD *in situ*. The growth of ALD-Al_2O_3 on *in situ* sputtered Al films was studied in depth. Atomic force microscopy and ellipsometry were used to determine that ALD-Al_2O_3 grows conformally on Al, but a ~ 2 nm thermally oxidized interfacial layer (IL) develops between the Al and Al_2O_3 for ALD films > 2 nm. The thickness of this IL decreased when the Al film was < 2 nm, confirming the IL is a thermal oxide. As a proof of concept, Nb/Al/ALD-Al_2O_3/Nb trilayers with ultrathin (< 1 nm) tunnel barriers were grown and processed into JJs. The junction specific resistance and gap current density were found to depend exponentially on the ALD film thickness, indicating that the tunnel barrier thickness can be controlled by ALD. Despite evidence for an estimated 0.8 nm interfacial layer in the ultrathin tunnel barrier, this work incontrovertibly concludes that ALD can be used to produce quality JJs.

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1 Introduction

1.1 Chapter Overview

Since the early 1970's, Moore's law has held that the transistor density of integrated circuit technology doubles approximately every two years. This increase in transistor density brings a correlated increase in processing power. Were this law to hold indefinitely, traditional silicon transistors would be able to eventually satisfy the computational requirements of scientific research. However, Moore's law cannot possibly hold indefinitely as long as silicon transistors are the dominant technology. Transistors can only be made so small before further reduction requires splitting the silicon atom itself. This limits their applicability to certain problems such as cryptography and quantum stimulation. In order to address these problems computationally, a new technology must be adopted.

Quantum computers (QCs) are a possibility for this new technology which would allow for further increases in computational power without requiring nanoscopic reduction. Algorithms for traditionally intractable problems have already been developed for QCs. Shor has demonstrated a method of factoring large numbers, which is interesting to the field of cryptography [1]. His algorithm should factor large numbers in a time that is proportional to some power of the number of digits involved (polynomial time). Contrast this to traditional computers which can, at best, factor in exponential time and the advantages of QCs become obvious. Further, QCs offer a potential quadratic speed up for searching algorithms and an exponential speed up for simulating quantum systems [2].

QCs are built from qubits, the quantum analog of a bit. Unlike traditional bits which can take on values of 1 (on) or 0 (off), a qubit can be placed in a superposition of on and off states.

When multiple superoimposed qubits are entangled, computation can be performed on the entangled ensemble in parallel. Such a level of parallelism is impossible to achieve in traditional computers. Many possible implementation schemes for qubits have been explored, including nuclear spins in solution, trapped ions, nuclear spins in solids, quantum optics, and quantum dots [3-7] to name a few. However, of all of these schemes, the Josephson Junction (JJ) based devices are the most promising. Robust JJ fabrication processes, which are compatible with modern semiconductor processing, have been in place since the 1980s, making the JJ a prime candidate for qubit implementation in terms of scalability.

The JJ is a superconducting tunnel junction (STJ). In its most basic form, the JJ is two superconducting electrodes separated by a very thin (~1 nm) insulator, the "tunnel barrier". However, materials problems, such as oxygen vacancies and interstitials in the tunnel barrier, have been a hindrance to realizing the full potential of the device as a quantum bit. This work addresses these materials problems by proposing a novel method of tunnel barrier growth, atomic layer deposition.

In this chapter, the basic physics of the Josephson junction is presented. The fundamental equations governing the device are derived and discussed in Section 1.2. The Josephson junction as a device is presented in Section 1.3, wherein its current-voltage characteristics, figures of merit, and fabrication are discussed in detail. In Section 1.4, atomic layer deposition is presented as a novel means of growing the tunnel barrier of the Josephson junction, and the primary problems in its implementation are identified.

1.2 Theoretical Foundations of the Josephson Junction

1.2.1 Overview of the Josephson Effect

The Josephson effect is used in a variety of modern devices. Superconducting Quantum Interference Devices (SQUIDs) rely on the Josephson effect to make precise measurement of magnetic fields, the international standard for the Volt is based on the Josephson effect, and the most promising candidate technology for quantum computation relies on the Josephson effect. In this section, the Josephson effect will be described, and important equations governing the effect will be derived.

The Josephson effect occurs in devices called Josephson junctions (JJs). Generally, A JJ is a device that weakly links two superconductors. This weak link can be realized in a number of ways. The most common JJ is the superconductor-insulator-superconductor (SIS) JJ, in which the two superconducting electrodes are separated by a very thin (~1 nm) insulating layer known as the "tunnel barrier", as shown in **Fig. 1.1a**. The weak link can also be realized by separating the superconductors by a thin conductor in the normal state, or an SNS JJ (**Fig. 1.1b**). A weak link can be also established through a constriction in the superconductor to produce a microbridge junction (**Fig. 1.1c**), or by using the native oxide on the electrode as a tunnel barrier and brining a pointed, superconducting rod into contact with it (**Fig. 1.1d**). This work will focus on the SIS JJ.

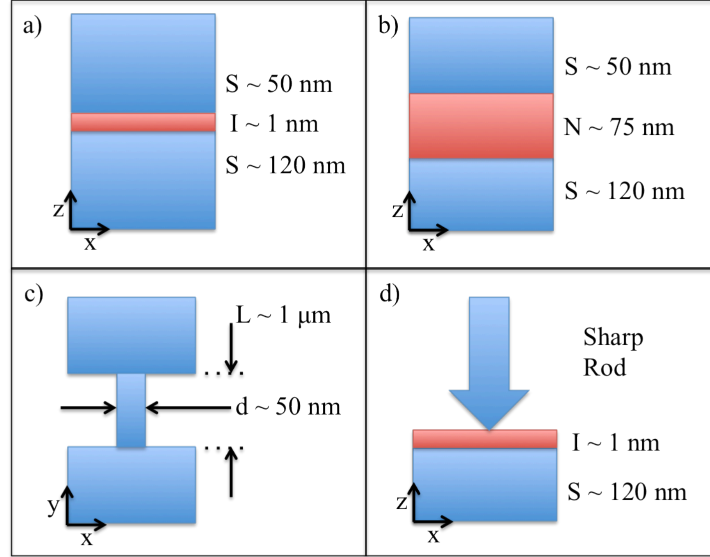


Figure 1.1: Schematic diagram of various Josephson junction architectures; the superconductor-insulator-superconductor (a), the superconductor-normal-superconductor (b), the microbridge junction (c), and the point contact junction (d).

There are two flavors of the Josephson effect; the DC effect, and the AC effect. The DC effect occurs when a finite current flows through the JJ at zero voltage. It is governed by the first Josephson equation

$$I = I_c \sin\phi \qquad (1.1)$$

where I is the current, I_C is the critical current across the JJ, and ϕ is the phase difference between the two superconducting electrodes. I_C is the maximum current that can flow across the JJ at zero voltage and is a function of device parameters such as the tunnel barrier thickness, tunnel barrier material, and the size of the JJ. If the JJ is current biased beyond I_C, it will transition into the "normal state" with a characteristic resistance of R_N. When the superconducting electrodes are of the same material, this transition occurs at the superconducting gap voltage of $V_G = 2\Delta/e$, where Δ is superconductor's gap energy (i.e. the energy required to break a Cooper pair) and e is the elementary charge. The AC Josephson effect, on the other hand,

occurs when an AC current develops across the JJ at a fixed, finite voltage. It is governed by the second Josephson equation

$$V = \frac{\hbar}{2e}\frac{\partial \phi}{\partial t} \tag{1.2}$$

where V is the voltage across the JJ, $\hbar$ is the reduced Plank's constant, e is the elementary charge, and ϕ is again the phase difference between the two superconducting electrodes. When the JJ is driven by microwave radiation of frequency f, the AC effect creates voltage steps of $\Delta V = hf/2e$ in the JJ's IV curve. These steps are the basis for the modern definition of the Volt [8].

In the following sections, the equations relevant to this work will be presented. First, the Josephson equations (eqn. 1.1 and 1.2) will be derived and discussed, followed by a derivation of the relationship between the tunnel barrier thickness and the critical current I_C, and lastly the Ambegaokar-Baratoff formula, which relates I_C, R_N, and Δ, will be presented and discussed.

1.2.2 The Josephson Equations

Brian Josephson derived his equations in 1962, for which he received the Nobel Prize in Physics in 1973. Though his seminal work derives the Josephson equations [9], a more elegant derivation was developed by Richard Feynman [10], which has been lauded and republished [11]. It is Feynman's derivation that will be presented here.

Consider two independent superconductors, *S1* and *S2*. The superconductors can be described by the macroscopic quantum wavefunctions, $\Psi_1(r)$ and $\Psi_2(r)$, respectively. The wavefunctions have the form used in the Ginzburg-Landau theory of superconductors

$$\Psi_j = \sqrt{n_j}\, e^{i\varphi_j(r,t)} \tag{1.3}$$

where n is the charge carrier (Cooper pair) density in the superconductor and $\phi(r,t)$ is the phase function with the form

$$\phi_j(r,t) = \phi(r) - \frac{2E_F}{\hbar}t \tag{1.4}$$

where E_F is the Fermi energy.

Imagine these superconductors are separated by a small vacuum gap of an arbitrary distance d, as shown in **Fig. 1.2**. Let us vary d and consider the three interesting regimes; $d = 0$, $d \rightarrow \infty$, and $d \rightarrow 0$. If $d = 0$, the wavefunctions $\Psi_1(r)$ and $\Psi_2(r)$ completely overlap. *S1* and *S2* act as a single superconductor, so the phase difference $\phi_2 - \phi_1 = 0$. As d approaches infinity, the wavefunctions become independent and the phase difference could take any value. In between these two extremes, as $d \rightarrow 0$, there must exist a range of d such that the superconductors become weakly coupled.

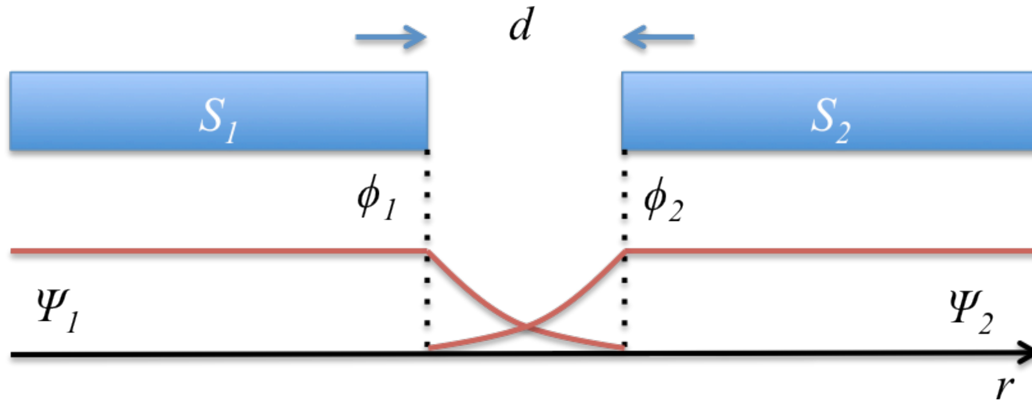


Figure 1.2: Schematic diagram of a theoretical Josephson junction

Applying the Schrödinger equation to the two wave functions and assuming symmetrical coupling yields

$$i\hbar\frac{\partial \Psi_1}{\partial t} = E_1\Psi_1 + k\Psi_2 \tag{1.5}$$

$$i\hbar\frac{\partial \Psi_2}{\partial t} = E_2\Psi_2 + k\Psi_1 \tag{1.6}$$

where E_j is the energy eigenvalue of Ψ_j, and k is a coupling constant. Defining E = 0 midway between E_1 and E_2, and applying a voltage V to the junction, equations 1.5 and 1.6 become

$$i\hbar\frac{\partial\Psi_1}{\partial t} = -eV\Psi_1 + k\Psi_2 \quad (1.7)$$

$$i\hbar\frac{\partial\Psi_2}{\partial t} = eV\Psi_2 + k\Psi_1 \quad (1.8)$$

Substituting the explicit form of the wave functions and separating the real and imaginary parts yields

$$\frac{\partial n_{S1}}{\partial t} = \frac{2}{\hbar}k\sqrt{n_{S1}n_{S2}}\sin(\phi_1 - \phi_2) \quad (1.9)$$

$$\frac{\partial n_{S2}}{\partial t} = -\frac{2}{\hbar}k\sqrt{n_{S1}n_{S2}}\sin(\phi_1 - \phi_2) \quad (1.10)$$

$$\frac{\partial \phi_1}{\partial t} = -\frac{k}{\hbar}\sqrt{\frac{n_{S2}}{n_{S1}}}\cos(\phi_1 - \phi_2) + \frac{eV}{\hbar} \quad (1.11)$$

$$\frac{\partial \phi_2}{\partial t} = -\frac{k}{\hbar}\sqrt{\frac{n_{S1}}{n_{S2}}}\cos(\phi_1 - \phi_2) - \frac{eV}{\hbar} \quad (1.12)$$

The change in Cooper pair density (eqns. 1.9 and 1.10) is counterbalanced by a current source attached to the junction. In this case, the current, I, though both superconductors should be equal to

$$I = 2e\frac{\partial n_{S1}}{\partial t} = -2e\frac{\partial n_{S2}}{\partial t} \quad (1.13)$$

Assuming equal Cooper pair densities in $S1$ and $S2$ ($n_{S1} = n_{S2} = n$), and combining eqn. 1.13 with eqns. 1.09 and 1.10 yields the first Josephson equation

$$I = 2e\frac{\partial n}{\partial t} = 4k\frac{en}{\hbar}\sin\phi \quad (1.14)$$

where $\phi = \phi_1 - \phi_2$, and $I_c = 4ken/\hbar$. Eqn. 1.14 governs the DC Josephson effect, wherein a finite current occurs at zero voltage.

By subtracting eqn. 1.12 from eqn. 1.11, we obtain the second Josephson equation

$$\frac{\partial \phi}{\partial t} = \frac{2e}{\hbar} V \tag{1.15}$$

Eqn. 1.15 governs the AC Josephson effect, wherein the phase change is proportional to the applied voltage by a quotient of fundamental constants.

1.2.3 Relationship Between the Critical Current and Tunnel Barrier Thickness

As can be seen in eqn. 1.14, I_C depends on e, n, $\hbar$, and k. Experimentally, e and $\hbar$ cannot be changed as they are fundamental constants of nature. The superconducting material used for the electrodes sets n, so experimentally varying n is difficult. On the other hand, k depends on the thickness of the tunnel barrier, which can be varied fairly easily with modern thin film technology (e.g. thermal oxidation or atomic layer deposition). In this section, a relationship between the critical current density, J_C, and the tunnel barrier thickness, d, is derived.[12]

Eqns 1.3 and 1.4 specify the wavefunction for Cooper pairs inside the superconductor. However, the wavefunction inside the tunnel barrier differs. If the tunnel barrier is modeled as a rectangular potential barrier with centered at $x = 0$ with a height V_0 and width $d=2a$, the wavefunction inside the barrier is a superposition of exponentials and can be written as

$$\Psi = C_1 \cosh \frac{x}{\zeta} + C_2 \sinh \frac{x}{\zeta} \tag{1.16}$$

where C_1 and C_2 are normalization constants, x is the distance inside the tunnel barrier and ζ is the decay length inside the insulator defined as

$$\zeta = \sqrt{\frac{\hbar^2}{2m(V_0 - E_F)}} \tag{1.17}$$

where m is the mass of the cooper pair. C_1 and C_2 can be found by setting boundary conditions at the edges of the potential barrier. For Ψ to be continuous, it must equal the superconductor wave function at x = ±a

$$\Psi(-a) = \sqrt{n}e^{i\phi_1} \tag{1.18}$$

$$\Psi(+a) = \sqrt{n}e^{i\phi_2} \tag{1.19}$$

Setting eqn. 1.16 at $x = \pm a$ equal to eqns 1.18 and 1.19 yields

$$C_1 = \frac{\sqrt{n}\left(e^{i\phi_1} + e^{i\phi_2}\right)}{2\cosh\left(a/\zeta\right)} \tag{1.20}$$

$$C_2 = \frac{\sqrt{n}\left(e^{i\phi_1} - e^{i\phi_2}\right)}{2\sinh\left(a/\zeta\right)} \tag{1.21}$$

The probability current density, is defined as

$$J_s = \frac{2e}{m}\mathrm{Re}\left\{\Psi^* \frac{\hbar}{i}\nabla\Psi\right\} \tag{1.22}$$

Substituting eqns 1.16, 1.20, and 1.21 into 1.22 yields the familiar Josephson equation

$$J_S = J_C \sin\left(\phi_1 - \phi_2\right) \tag{1.23}$$

where J_C, the critical current density, is now defined as

$$J_C = \frac{e\hbar n}{2m\zeta \sinh(2a/\zeta)} \tag{1.24}$$

A good approximation is a >> ζ [12], which simplifies eqn. 1.24 to

$$J_C = \frac{e\hbar n}{4m\zeta} e^{\frac{-2a}{\zeta}} \tag{1.25}$$

Eqn. 1.25 shows that the critical current density depends exponentially on the tunnel barrier thickness, $2a$, and on the potential barrier of the insulating material, V_0, which is

enveloped in the decay length, ζ. Experimentally, we then expect to see a wide range of critical current values even when the tunnel barrier thickness is only slightly changed.

1.2.4 The Ambegaokar-Baratoff Formula

The critical current through a junction is indeed a very important device parameter. However, it is not the only measurable parameter. For a current $I > I_C$, the JJ's current-voltage relationship becomes ohmic, with a characteristic resistance R_N, the normal state resistance. The $I_C R_N$ product, also called the characteristic voltage, determines the switching speed of the JJ [13], which is incredibly important for computation applications of JJs such as RSFQ logic. Further, I_C is very difficult to measure, and its maximum value can only be measured in an ideal, noise-free laboratory. The gap current, I_G, is the current at the gap voltage, $V_G = 2\Delta/e$. I_G is much more easily measured and can be simply related to I_C.

The Ambegoakar-Baratoff formula is this simple relationship between I_C, R_N, and I_G. In its general form, it describes the temperature dependence of the critical current. Its derivation is laborious [14] and beyond the scope of this work. When the superconducting electrodes are of the same material, the formula takes the form

$$I_C(T) = \frac{\pi\Delta(T)}{2eR_N}\tanh\frac{\Delta(T)}{2kT} \tag{1.26}$$

where I_C is the critical current, R_N is the normal state resistance, T is the absolute temperature, $\Delta(T)$ is the gap energy of the superconductor as a function of temperature, e is the elementary charge, and k is the Boltzmann constant.

For T = 0, eqn. 1.26 reduces to

$$I_C = \frac{\pi\Delta(0)}{2eR_N} = \frac{\pi}{4}\frac{2\Delta(0)}{e}\frac{1}{R_N} = \frac{\pi}{4}\frac{V_G}{R_N} = \frac{\pi}{4}I_G \tag{1.27}$$

which states that I_C is about 80% of I_G. A good approximation of I_C can therefore be made even in the absence of a direct measurement of I_C. Another useful variation of this simplification is

$$R_N A = \frac{\pi\Delta}{2e}\frac{1}{J_C} \tag{1.28}$$

where A is the area of the JJ, and J_C is the critical current density. Therefore, on any given wafer with a uniform J_C, the product $R_N A$ is expected to be a constant. This allows for the approximation of J_C from measurements of the room temperature JJ resistance, R_{300K}.

1.3 Practical Aspects of the Josephson Junction

In this section, the current voltage characteristics (IVCs) and the figures of merit of JJs are presented and discussed. The traditional fabrication method of Nb/Al/AlOx/Nb JJs is reviewed. Outstanding issues in implementing quantum bits with JJs are addressed, and strategies other researchers have used to overcome these problems are discussed.

1.3.1 Overview of the Josephson Junction Device

JJs have a characteristic and unique IVC, as shown schematically in **Fig. 1.3.** Important parameters in the IVC are the critical current (I_C), the normal state resistance (R_N), the gap current (I_G) and the gap voltage (V_G). I_C is due to Cooper pairs tunneling the barrier. The subgap ($|V| < V_G$) current and the normal state current are due to quasiparticle tunneling.

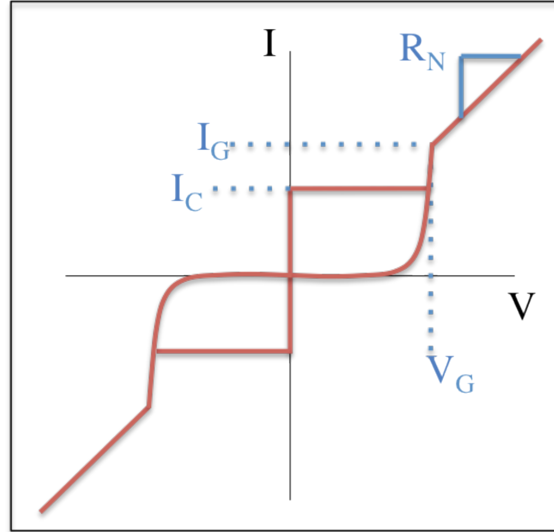


Figure 1.3 Schematic depiction of the current voltage characteristics of a Josephson junction. I_C is the critical current, R_N is the normal state resistance, V_G is the gap voltage, and I_G is the gap current.

There are several figures of merit that can be extracted from the JJ IVC [15]. The first and most widely used is the characteristic voltage, or $I_C R_N$ product, which is a figure of merit used to judge the overall quality of the JJ. For a JJ with thin film Nb electrodes, the ideal $I_C R_N$ = 2.4 mV at T = 0 K, with lower quality JJs having a lower $I_C R_N$. Another figure of merit is the subgap resistance, R_{SG}, defined for Nb SIS junctions as the ratio of voltage to current at V = 2 mV. This, along with the ratio of R_N/R_{SG}, is used to judge the leakiness of the tunnel barrier. An acceptably large value for R_N/R_{SG} = 20, which indicates a good tunnel barrier, while a low R_N/R_{SG} (e.g. R_N/R_{SG} = 10) indicates a tunnel barrier than may be leaky due to pinholes. However, this metric is dependent on both temperature and J_C, and should be used with caution. The gap voltage, V_G, is also a figure of merit that is used to judge the material quality of the electrodes of the JJ. For thin film Nb electrodes, the ideal V_G = 2Δ/e = 3 mV. However, for figure of merit calculations, V_G is defined as the midpoint in the steep current rise in the sub-gap region. These figures of merit will be discussed more in Chapter 4.

1.3.2 Fabrication of Modern Josephson Junctions

The history of JJ fabrication dates back to just after Brian Josephson predicted the Josephson effect in 1962. In fact, the first JJ was produced by Philip Anderson and John Rowell in 1963 at Bell Labs [16]. Their device used superconducting Sn and Pb electrodes with a very thin native SnOx as the tunnel barrier. Since then, many fabrication techniques, device architectures, and materials combinations have been explored by both the research and commercial communities in an effort to produce robust devices. Nb, Al [13], Re [17], and even high-T_C materials such as YBCO [18] have been explored, to name just a few.

In the 1980s, the Nb JJ process was developed and has since become the industry standard [13, 19]. In this process, Nb is used for the superconducting electrodes. Bulk Nb has the highest critical temperature of all elemental superconductors with T_C = 9.26 K [20]. Liquid helium cooling is therefore sufficient to cool the JJ to ~50% of T_C, where the gap energy remains at 90% of its maximum value at T = 0 K. Compare this to Al, which has a T_C = 1.2 K and requires He-3 refrigeration to reach $T < 0.5\ T_C$, and the benefit of using Nb becomes clear. Bulk Nb also has the largest gap energy of the elemental superconductors at Δ = 1.5 meV [20-22], meaning the Cooper pairs are tightly bound and the superconducting state is robust against small thermal fluctuations. Nb is also a relatively abundant metal; it is the 33rd must abundant metal in the Earth's crust with a relative abundance of 20 ppm [23]. Nb is also compatible with modern thin film processing techniques; it can be deposited via sputtering and etched with reactive ion etching in SF_6, a non-toxic gas. It's superconducting properties, abundance, and ease of processing make Nb a natural choice for research and commercial applications of JJs.

The tunnel barrier in the Nb process is aluminum oxide (AlOx) grown by thermal oxidation. Niobium oxide (NbOx) has been explored as a tunnel barrier material [24], but because of its multiple oxidation states [25-27] it was found to be an unreliable material. Instead,

a thin Al layer (~ 5 nm) is added to the bottom Nb electrode. This Al layer is then exposed to a controlled pressure of O_2 to oxidize the surface to form AlOx via thermal oxidation. Because AlOx is denser than Al, the AlOx layer forms an oxygen diffusion barrier, and the oxidation process is self-limited. The thickness of the tunnel barrier, and by extension J_C of the wafer, can be varied by controlling the pressure of O_2 and the exposure time [28]. This oxidation process is able to control J_C over 6 orders of magnitude, from ~10^6 A/cm^2 to ~10 A/cm^2 [29]. **Fig. 1.4** is taken from Reference [29] and shows the dependence of J_C on oxidation dose. The knee in the data represents a transition from a partially oxidized Al surface with pinholes in the tunnel barrier (high-J_C regime) to a completely oxidized Al surface (low-J_C regime). It is worth nothing, however, that oxidation should only be compared at constant pressure since the ultimate thickness of the oxide layer is pressure dependent [28]. The ability to control J_C over such wide range with such a simple process has made thermal oxidation the dominant technology for the growth of JJ tunnel barriers.

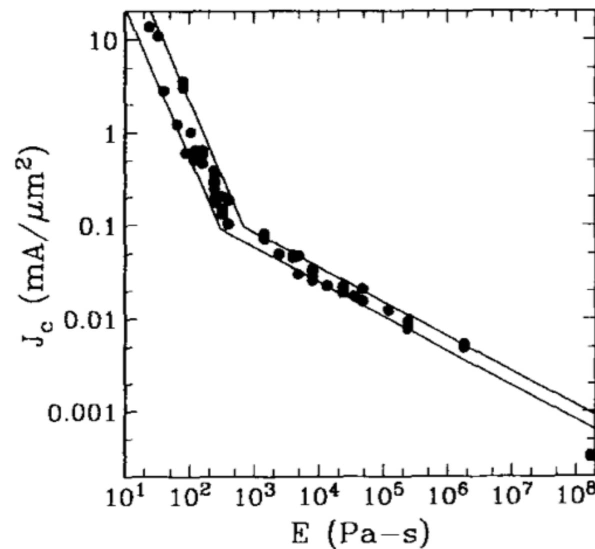


Figure 1.4 Critical current density (J_C) vs. oxidation dose (E) for trilayers processed at room temperature from Reference [29].

1.3.3 The Qubit Noise Problem

Traditionally fabricated JJs (i.e. Nb/Al/AlOx/Nb JJs) have been remarkably successful for magnetometery (SQUIDs), precision metrology (Josephson voltage standards), and high performance computing (RSFQ logic). JJs are also a prime candidate for the implementation of quantum computing (QC). A quantum bit (qubit), i.e. the basic unit of quantum information, must satisfy the DiVincenzo requirements, of which there are five [30]. Five of these requirements (e.g. the qubit must be initialized to a ground state) are trivially satisfied. However, the remaining two are stringent requirements. First, the qubit technology must be scalable so that many qubits can be made on a single chip. The Nb/Al/AlOx/Nb JJ is compatible with modern semiconductor processing technology and is therefore scalable to a massive level. This is in contrast to other candidates for quantum computing, e.g. the trapped ion qubit [31], which are difficult to scale up. Second, the qubits must have long coherence times, i.e. they must be able to be entangled for much longer than it takes to perform a quantum computation. QC algorithms act on entangled quantum states in parallel. If the qubits couple too strongly to the environment, this entangled state is lost, and the computation cannot be performed. While JJ qubits can be entangled, their short coherence times have been problematic.

JJ qubit coherence times have suffered due to coupling to two-level fluctuators (TLFs). It has been shown that defects in the dielectric materials of the circuit, namely oxygen vacancies and interstitials in the tunnel barrier, are the primary source of TLFs [32]. Several techniques have been explored to combat this problem. Specialized microwave shielding has been developed to insulate qubit circuits from the environment, and this strategy has substantially increased coherence times [33]. Quantum error correction algorithms have also been developed to detect and correct decoherence, and a two-qubit gate fidelity of 99.4% has been achieved [34].

Finally, material science techniques, such as epitaxial growth of the tunnel barrier, have been employed to remove the TLFs from the circuit entirely [17].

The materials strategy is particularly promising considering the thermal oxidation scheme for developing JJ tunnel barriers has not changed significantly since the 1980s, despite great strides in thin film processing since then. Further, it has already been shown that using epitaxial techniques can dramatically improve the coherence times of JJ qubits. **Fig. 1.5**, taken from Reference [17], shows a comparison of the qubit noise spectra between amorphous and epitaxial tunnel barriers. The splittings in the spectra indicate the presence of TLFs. The qubits with amorphous tunnel barriers had an average of 24 splittings per GHz while the qubits with single crystal tunnel barriers had an average of only 5 splittings per GHz, a dramatic improvement. However, epitaxial films require a very small lattice mismatch, on the order of ~1%, which disqualifies the traditional and robust Nb and Al_2O_3 combination. To achieve a lattice match with Al_2O_3, the bottom electrode material must be Re with a reduced T_C = 1.4 K [20] compared to Nb with T_C = 9.26 K. Further, epitaxial techniques are laborious and require elevated temperatures, e.g. Re sputtering at 850 °C and Al_2O_3 annealing at 1050 °C [17, 35]. While these techniques are certainly within the realm of possibility, a more convenient method of trilayer fabrication would be more attractive to private industry and enable more researchers to contribute to the problem. To remove TLFs from the tunnel barrier and to truly realize the full potential of the shielding and error correction techniques, it is imperative to find alternative methods of tunnel barrier growth that are compatible with the traditional Nb process.

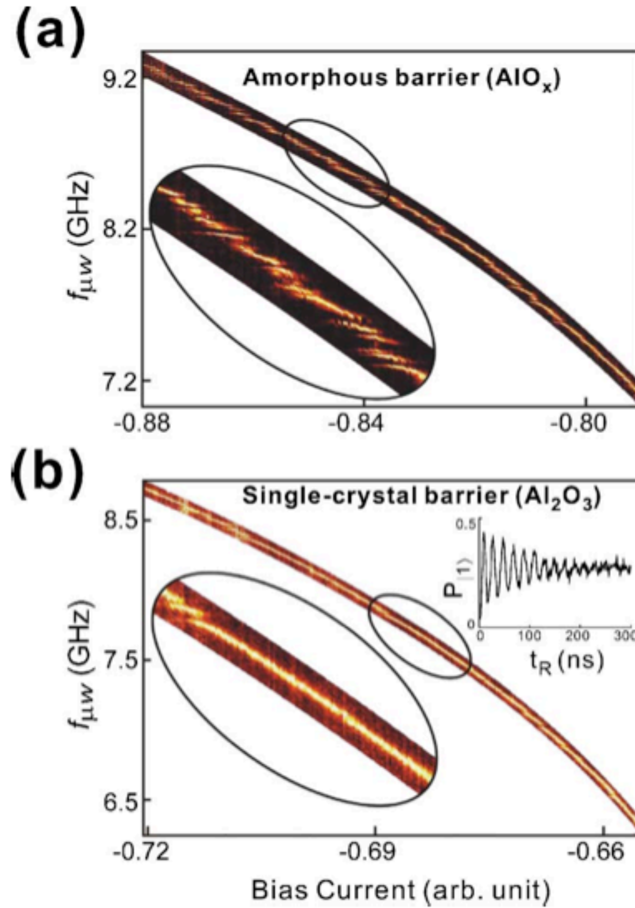


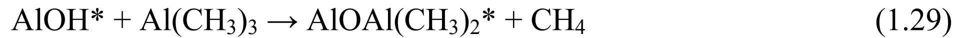
Figure 1.5 Comparison of qubit noise spectrum between identically designed qubits with an amorphous tunnel barrier (a) and a single crystal tunnel barrier (b) taken from Reference [17]. The splittings in the spectrum are indicative of two level fluctuators in the tunnel barrier, which are the primary source of decoherence JJ qubits.

1.4 Atomic Layer Deposition

Atomic layer deposition (ALD) is a promising growth technique for reducing the defect density in JJ tunnel barriers. ALD is a chemical vapor growth process by which a film is grown a single monolayer (ML) at a time. Interestingly, it was invented independently twice [36]. It was first proposed and published by Valentin Borisovich Aleskovskii and his students in the USSR in 1960s under the name “molecular layering”[37]. The first patent for ALD was given to Dr. Tuomo Suntola of Finland in the 1970’s under the name “atomic layer epitaxy”. However, it was not until and 1980’s that ALD research received wide interest, and since then over 100 review

articles have been written on the topic (for example Steven George's overview [38]). Most recently, it has received attention by researchers seeking a method of growing high-κ dielectrics, such as HfO_2.

ALD achieves monolayer growth through self-limited surface reactions. Multiple chemical vapors are pulsed into a reaction chamber and are immediately removed, as depicted schematically in **Fig. 1.4**. The vapors are pulsed separately so that only one chemical source is present in the chamber at a time (**Fig. 1.4 a**). The sources react only on the surface of the substrate before they are purged (**Fig. 1.4 b**). In this way, when the next source is pulsed into the chamber (**Fig. 1.4 c**), it can only react with the surface residue of the previous source. A nearly ideal ALD growth process is ALD Al_2O_3, which uses trimethylaluminum (TMA) and H_2O. It is governed by the reactions



$$AlOH^* + Al(CH_3)_3 \rightarrow AlOAl(CH_3)_2^* + CH_4 \quad (1.29)$$

$$AlCH_3 + H_2O \rightarrow AlOH^* + CH_4 \quad (1.30)$$

where $Al(CH_3)_3$ is TMA, and the asterisk denotes a surface species. These reactions take place cyclically; one cycle is defined as each of the reactions occurring once. These reactions are self-limited only in the correct temperature window. If the temperature is too low, the sources physisorb on the surface and are not purged successfully. If the temperature is too high, the sources decompose and the reactions do not take place. For ALD Al_2O_3, the ideal temperature is near 200 °C, though successful growth has been reported at temperatures as low as 33 °C (with incredibly long purge times)[39].

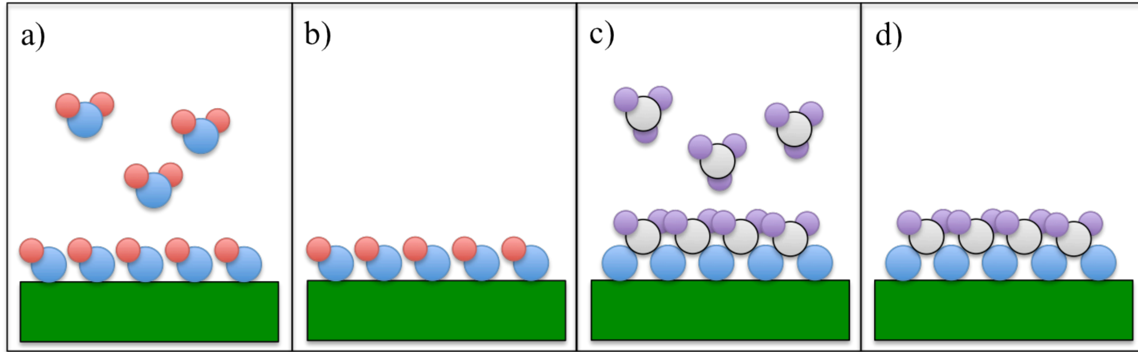


Figure 1.6 Schematic depiction of ALD growth process. The first source (e.g. H_2O) is pulsed into the chamber (a) and then flushed after it reacts with the sample surface (b). The next source (e.g. TMA) is then introduced (c), and again flushed (d) to produce a single monolayer (e.g. Al_2O_3)

Because it relies on self-limited surface reactions, ALD has unique advantages over other methods of oxide growth. One obvious advantage is precision control over film thickness. Because ALD films grow one ML at a time, the thickness can be controlled on the subnanometer level. For example, each cycle of ALD Al_2O_3 produces 0.12 nm of thickness. Another advantage is high conformality. ALD is able to deposit on structures with arbitrarily large aspect ratios, and it preserves the surface roughness of the substrate even for very smooth substrates[40]. Also, because the surface reactions are self limited and complete, ALD films have low defect densities. As long as the growth parameters (e.g. temperature, pulse time, purge time) are well tuned, every active surface site will play in the reaction, reducing the possibility of oxygen vacancies and interstitials. Finally, ALD can be used to grow a wide variety of films, including Al_2O_3, MgO, HfO_2, and ZnO to name a few (see Miikkulainen et al. for a complete list [41]).

These unique advantages make ALD a prime candidate for growing JJ tunnel barriers. The subnanometer thickness control implies precise and reproducible control of J_C. The high conformality and surface reactivity of ALD growth implies the tunnel barrier will be leak-free and have lower defect densities than traditional thermally oxidized AlOx tunnel barriers. The variety of available materials would allow greater flexibility in the design of JJ tunnel barriers. In

fact, while ALD Al_2O_3 grows as an amorphous film, ALD HfO_2 is known to grow in a polycrystalline phase, which could be used to produce single crystal tunnel barriers without the aforementioned difficult epitaxial techniques.

Since JJs require an insulating film only ~1 nm thick, the nucleation of ALD grown tunnel barriers is a critical issue. Thanks to its appeal to the semiconductor industry, there are extensive reports of ALD Al_2O_3 nucleation on Si. Theoretically, Si surfaces are terminated with a layer of hydroxyl groups, which allows TMA to attach readily as governed by eqn 1.29. However, an interfacial layer (IL) between Al_2O_3 and Si substrates has been reported which is typically ~1 nm thick and is composed of an alumina silicate [42]. Interestingly, a long exposure of Si to TMA can reduce the thickness of the IL to ~0.5 nm, while a long exposure to water does not have the same effect [43]. This suggests that the IL is caused in part by the thermal oxidation of the substrate by exposing it to water at elevated temperatures.

However, while ALD growth on Si substrates is a well-studied problem, little work has been done regarding ALD growth on metallic substrates. The most comprehensive work to date on metallic substrates was performed by Groner *et. al.* [44] wherein AL_2O_3 ALD was performed on Au, Co, Cr, Cu, Mo, Ni, NiFe, NiMn, Pt, PtMn, H-Si, stainless steel, and W. It was found that ALD films grew easily on metals with a reactive surface (e.g. Cu, Mo), while nucleation was frustrated on metals with an inert surface (e.g. Au, Pt). Several groups have studied ALD on noble metals in a greater detail [45-48] and found the growth does not initiate during the first few ALD cycles. Instead, an incubation period is required to initiate nucleation. To contrast this, other groups have studied ALD growth on more easily oxidized metals such as W, Co, and Ta [48-50]. It was found that the growth rate during the first few ALD cycles was greater than expected, and an interfacial layer formed between the substrate and the ALD film. This implies

not only that ALD nucleation occurs easily when the substrate metal is easily oxidized, but also that an interfacial layer of thermal oxide is being formed. These interfacial layers are on the order of 1-5 nm, which would be catastrophic for JJ applications due to the requirement that the tunnel barrier be ~ 1 nm. Further, native oxides may form on metallic substrates prior to ALD growth if the ALD process is not carried out *in situ* with the metal deposition. These native oxides can be up to 5 nm thick [40], which again would be catastrophic to JJs. This makes the formation of an interfacial layer a critical issue when applying ALD to JJ tunnel barriers.

This work is intended as a pioneering proof of concept of ALD tunnel barriers. It is unknown if ALD-Al_2O_3 nucleation occurs easily on Al, the traditional wetting layer in Nb JJs. It is also unknown if an interfacial layer develops between the Al and ALD-Al_2O_3. Crucial questions, such as how thick this interfacial layer can become and when in the growth process it develops, are still unanswered. Most importantly, it is unknown whether ultrathin ALD films are uniform enough to act as tunnel barriers. It is entirely possible that, in the nucleation phase, large pinholes develop in the ALD film, which would make them useless as tunnel barriers.

This work addresses and answers these questions. To do this, a novel thin film deposition tool was built to integrate ALD with ultra high vacuum sputtering. The design and construction of this tool is the subject of Chapter 2. This tool was used to grow 20 – 100 ALD cycles on *in* situ sputtered Al substrates, and the film thickness was measured with ellipsometry. These results are presented in Chapter 3. Finally, Nb/Al/ALD-Al_2O_3/Nb trilayers were grown and patterned into JJs, and their IVCs were measured at 4.2 K. These results are presented in Chapter 4.

2 Experimental Description

2.1 Chapter Overview

This chapter describes the relevant experimental procedures of this dissertation. The chapter is separated into three main sections; Nb/Al/ALD-Al_2O_3/Nb trilayer fabrication, Josephson junction device processing, and measurement description. The first section, trilayer fabrication, describes a novel deposition tool that was built for this project and how this tool was used to produce trilayers. The tool integrates sputtering with atomic layer deposition (ALD) *in situ* to produce Nb/Al/ALD-Al_2O_3/Nb, and a detailed description of the tool itself and its use are given. The second section, Josephson junction device processing, describes in detail how these trilayers were processed into JJs with ALD tunnel barriers. The process is divided into three sections; the trilayer etch, the JJ mesa definition, and the top wiring. Details of process parameters and design are given. The third section, measurement description, describes how these devices were characterized at room temperature and 4.2 K. Details of the hardware and procedure are given.

2.2 Nb/Al/ALD-Al_2O_3/Nb Trilayer Fabrication

This section describes a novel thin-film deposition tool used to create Nb/Al/ALD-Al_2O_3/Nb trilayers. The tool integrates viscous flow ALD with UHV sputtering *in situ*, which removes the possibility of native oxides forming in the trilayer due to exposure to the ambient atmosphere. The procedural use of this tool to create Nb/Al/ALD-Al_2O_3/Nb trilayers is also described in detail.

2.2.1 Description of Deposition System

2.2.1.1 System Overview

The ALD-UHV sputtering system developed in this work has four main components; a viscous flow ALD chamber, a UHV sputtering chamber, a load lock, and a sample transportation system. **Fig. 2.1** shows the layout of these components. In particular, the geometries of the sample at different stages of the *in situ* fabrication are depicted including UHV sputtering of metals (**Fig. 2.1a**), possible surface/interface treatment with plasma in the load lock (**Fig. 2.1b**), and ALD growth of the tunnel barrier (**Fig. 2.1c**) with sample transfer from chamber to chamber provided by the sample transport system (**Fig. 2.1d**). Three gate valves shown in **Fig. 2.1** allow each of the three cambers for sputtering, load lock, and ALD to be sealed completely during the corresponding operations. Not shown in **Fig. 2.1** is a second UHV sputtering/ion beam chamber for MTJs, which is connected to the left of the first UHV sputtering for superconductors (**Fig. 2.1a**). With another sample transportation system attached to the second sputtering chamber, a sample can be transported between different chambers for fabrication of Josephson junctions (JJs), magnetic tunnel junctions (MTJs), and more complicated devices such as magnetic Josephson junctions [51, 52]. This means the current design of the ALD-UHV sputtering system is very versatile and a cluster of UHV chambers may be integrated to this system for fabrication of multiple functional materials.

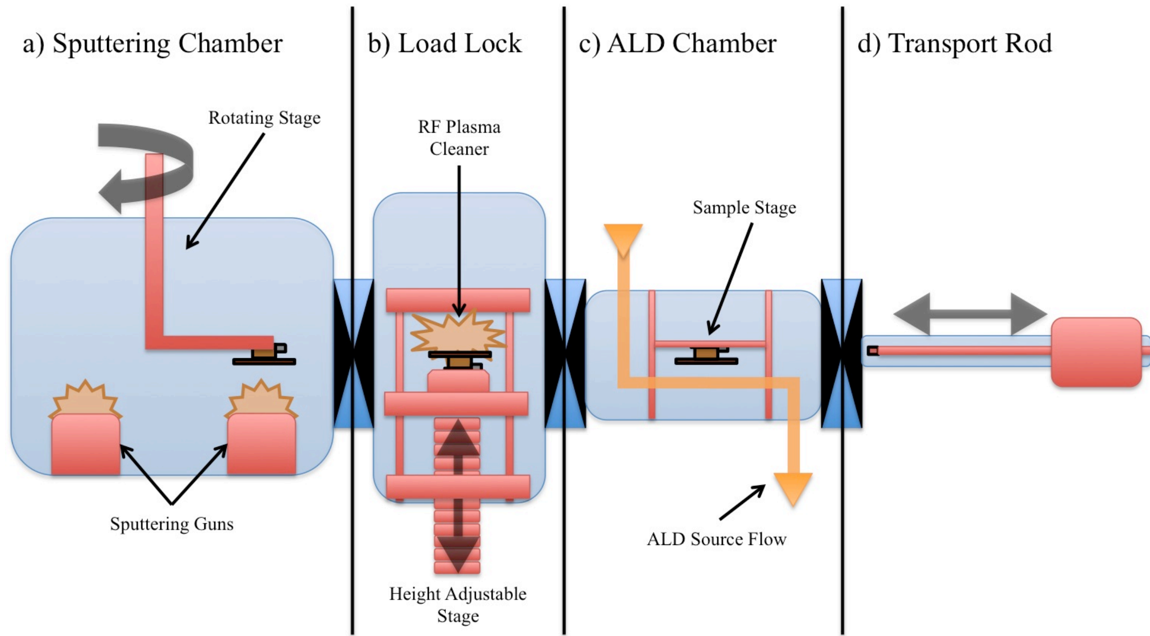


Figure 2.1 A schematic diagram of the ALD-UHV sputtering system. The UHV sputtering chamber (a) has three sputtering guns and a rotatable, water-cooled stage. It is kept at constant UHV by a cryopump. The load lock (b) is used for sample loading and unloading and contains an RF plasma treatment stage with an adjustable height stage. It is quickly brought between atmospheric pressure and high vacuum by a turbomolecular pump. The ALD chamber (c) is isolated from the other chambers by two gate valves to ensure a proper flow profile of the ALD sources, and it is heated by heat rope wrapped around its exterior (not shown). ALD is a low vacuum process, so the ALD chamber is pumped by a mechanical pump. Finally, the magnetically coupled transport rod (d) allows for UHV sample transfer from one chamber to another.

2.2.1.2 ALD Chamber

The ALD chamber is a viscous flow reactor with the ALD source handling similar to that previously described by Elam et al[53]. However, our ALD chamber differs significantly from those previous reported in its dimensions, sample mounting, and heating system. In order to accommodate 2 inch wafers and to integrate with the necessary UHV gate valves, the chamber itself is constructed from a 3 inch outer diameter, 8 inch long stainless steel tube with two CF flanges welded to the two ends for interfacing with the load lock and sample transport through gate valves. On the inner side of the tube, rails were installed to catch a specially designed sample chuck (described in detail in Section 2.2.1). During ALD growth, the rails suspend the entire chuck with the wafer at the center of the chamber. The chamber is blackbody heated,

instead of the common solution of using a pancake heater to heat only the sample, by heat tape wrapped around the external wall of the chamber. This hot-wall ALD chamber has advantages in uniform sample heating across the wafer and much reduced condensation of the ALD sources on the chamber wall. This design can be readily expanded to accommodate larger wafers using larger stainless steel tubes to make the ALD chamber.

A schematic diagram of the chamber is shown **Fig. 2.2**. **Fig. 2.2a** presents a cartoon schematic to demonstrate the layout of the relevant sensors, gate valves, and heaters. **Fig. 2.2b** and **Fig. 2.2c** show engineering schematics from isometric and front angles, respectively, with the main chamber tube removed to show the inner details of the chamber to scale. For completeness, the ALD valves are presented schematically in **Fig. 2.2d**, and will be discussed presently. As seen in **Fig. 2.2a**, on either side of the ALD chamber are two 4.625 inch CF flanged UHV gate valves which allow the ALD system to be totally isolated from the other chambers during operation. One of these gates is interfaced directly to the load lock,while the other is interfaced to the transport rod. These gate valves are critical to avoid contamination of the other chambers and components with ALD films and source chemicals. Sample docking is achieved by rails housed in a cylindrical inset which is held inside the ALD chamber with set screws (**Fig. 2.2b**). There are four smaller flanges in the chamber. The top and bottom flange are for source delivery and exhaust, respectively. The other two small flanges are for a thermocouple and a quartz crystal monitor (QCM).

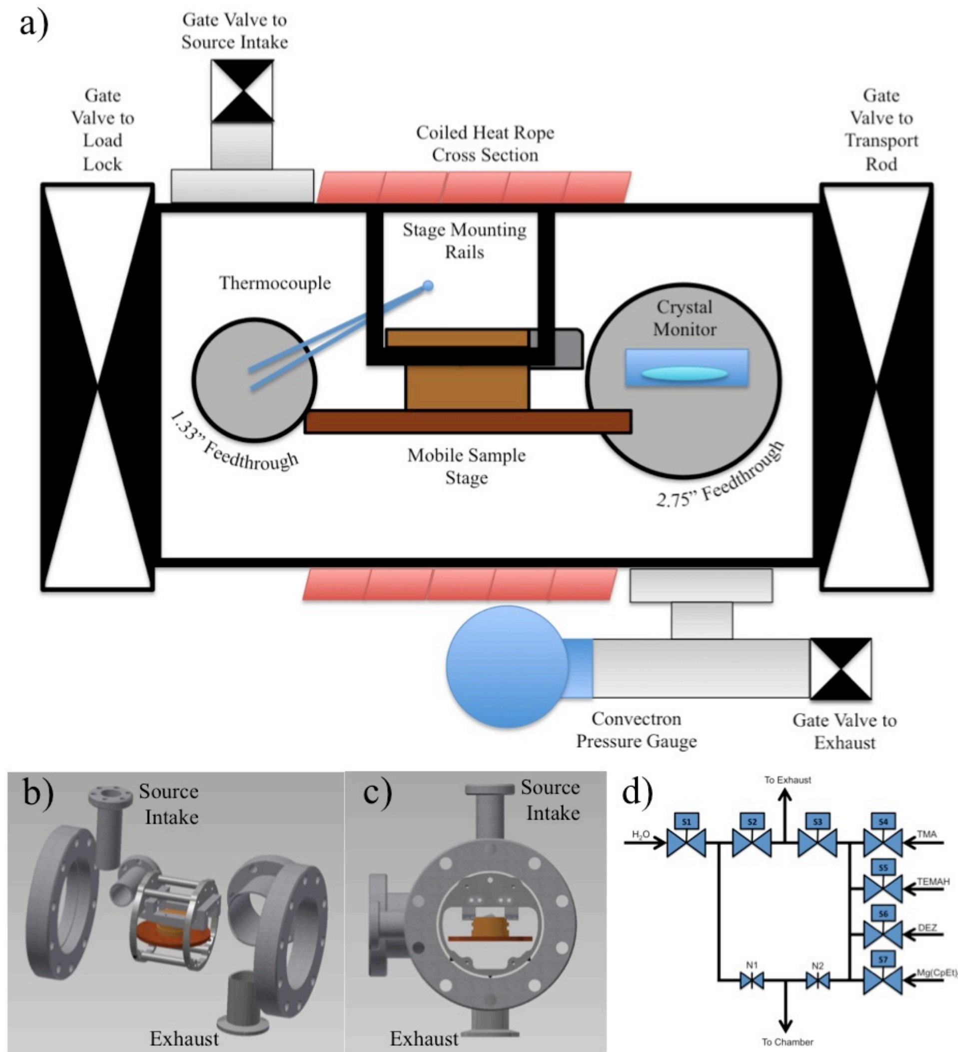


Figure 2.2 A schematic cross section (a) isometric (b) and front (c) views of the ALD chamber with the main chamber body removed. The sample stage (copper) is mounted on a cylindrical rail assembly. The sources are delivered through a computer controlled solenoid manifold (d) and a 1.33 inch CF flange on the top of the chamber. The internal temperature of the chamber is measured via thermocouple mounted to a 1.33 inch CF flange on the front left side of the chamber. Growth is monitored with a quartz crystal monitor (QCM) mounted on a 2.75 inch CF flange on the back left side of the chamber. The exhaust port is a QF flange on the bottom for the chamber, and it is fitted with a convectron pressure gauge. Gate vales to the load lock are mounted on 4.625 inch CF flanges on the front and back of the chamber.

ALD usually occurs at elevated temperatures, inside the chemical reaction window or "ALD window" defined by the given precursors [38]. To achieve these temperatures, the chamber is heated using resistive heat tape (McMaster-Carr) wrapped around the outside of the chamber. The power to the heater was provided by a variac and the temperature of the ALD chamber wall was controlled using an Omega temperature controller and a K-type thermocouple

inside the chamber. This blackbody heating is a simple and cost effective solution which replaces the more popular pancake heater in commercial ALD systems. The benefit of the blackbody heating is in flexibility of sample chuck design. In the specific case of Nb/Al/Al_2O_3/Nb SIS JJs, the chuck needs to be cooled efficiently during Nb electrode sputtering and can be readily heated to 200-300 ºC in the ALD chamber. An additional benefit of this blackbody heating for ALD, as we have mentioned earlier, is in ease of expansion of the chamber for larger wafers while maintain the uniformity of heating across the wafer. The source delivery tubing was also heated with resistive tape to prevent condensation of the sources. In order to achieve ALD growth, the delivery tubing must be heated to above the boiling point of the source but below its decomposition temperature. Heating the delivery tubing is particularly important to increase the flow of the sources with low vapor pressures such as TEMAH, which is used for ALD growth of HfO_2. An example of the temperature of the chamber and one section of tubing while preheating for ALD-AL_2O_3 growth is given in **Fig. 2.3**. ALD AL_2O_3 growth occurs best around 200 ºC, which the chamber (top curve, black circles) achieved through blackbody heating after only 90 minutes of heating at 150 W. For the delivery tubing (bottom curve, red squares), a temperature of 90 ºC was selected for TMA to minimize condensation. Because of the low thermal mass of the tubing, this temperature can be achieved and adjusted quickly, as shown by the shoulder in the curve at 40 minutes when the delivered power was increased. Using heat tape and blackbody radiation to heat the ALD chamber is a cost effective strategy for achieving a uniform temperature for an arbitrary chamber size, and heat tape on the delivery tubing allows fast changes in temperature for the sequential deposition of ALD films using different sources.

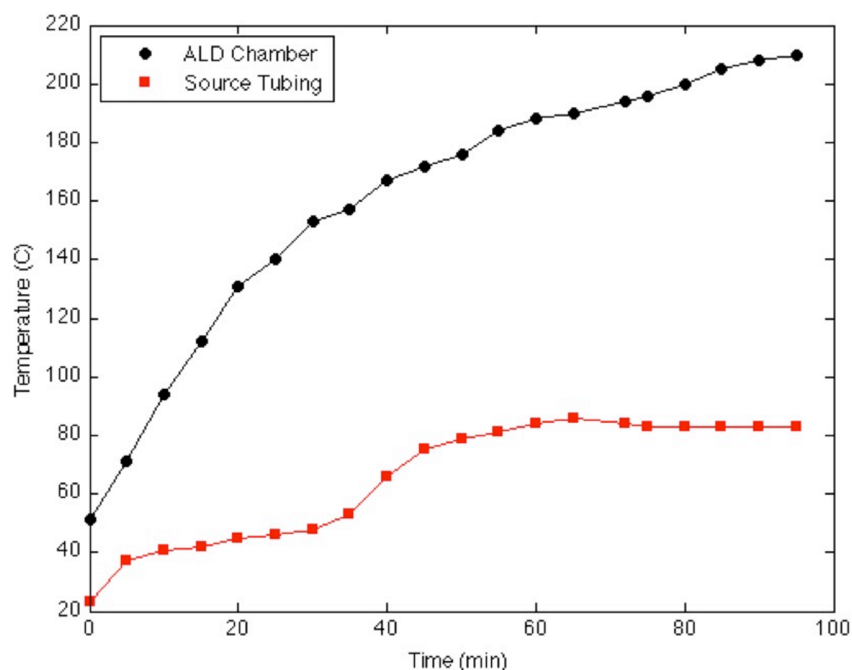


Figure 2.3 Temperature vs. time while heating the ALD chamber (top, black circles) and delivery line (bottom, red squares). The ALD chamber is heated externally with resistive heaters. The temperature is measured via internal thermocouple which is heated only by radiation from the chamber walls. The delivery tubing is heated in the same way, but measured by external thermocouple. Its smaller thermal mass allows faster, more responsive heating, as seen by the shoulder in the data when the delivered current was adjusted.

At sample temperatures within the ALD window, the reaction between the ALD sources produces self-limited growth, but only if the sources are delivered into the chamber correctly. A schematic of the valve system is given in **Fig. 2.2d**. The delivery tubing is made from ¼" outer diameter (OD) seamless stainless steel tubing and stainless steel compression fittings (Swagelock). The sources enter into the delivery tubing through high speed solenoid valves (Parker Series 99) with a switching time of 100 ms, which are controlled by a custom solenoid controller and a labview program. The pressure pulse height of the sources in the chamber is controlled by two needle valves (Swagelok). Installed sources (**Fig. 2.2d** S1, S4-S7) include H_2O (Ultima grade, Fischer Scientific), TMA (Sigma-Aldrich) for Al_2O_3, TEMAH (Sigma-Alrich) for HfO_2, Diethyl Zinc (DEZ, Akzo Nobel) for ZnO, and $Mg(CpEt)_2$ (Strem Chemicals) for MgO. New sources can easily be added by simply installing another valve onto the already existing line

of source valves, making this delivery system flexible and scalable. But during the ALD process, only one of these sources may enter the chamber at a time, and after such an exposure the chamber and delivery tubing must be purged. To do this, the source solenoids are closed and the exhaust solenoids (**Fig. 2.2d**, S2 and S3) are opened. This creates a path from the valve assembly directly to exhaust to quickly purge the system of any remaining source vapor. Using ALD AL_2O_3 as an example, one ALD cycle consists of opening the H_2O valve (S1), opening the purge valves (S2 and S3), opening the TMA valve (S4), followed by opening the purge valves again. Other films can be grown using an identical cycle, but replacing the TMA valve with another source's valve. Typically, 1-5 second source exposures and 30-60 second purges are performed. These are significantly higher than cycle times reported by other groups (typically reported values are 10s or 100s of milliseconds) due to the significantly longer tubing we used to satisfy safety guidelines. It is worth noting that these tubes should be as short as possible to minimize "dead volume" and to decrease the time it takes to complete one cycle. Further, any area that is exposed to both sources is in danger of becoming contaminated with the product of the bulk reaction between the sources, which in the case of water and TMA is a very fine alumina powder. So far, we have found no effective remedy for this problem aside from discarding contaminated parts.

To ensure the delivery system is operating correctly, a quartz crystal monitor (QCM) was installed inside the ALD chamber. QCMs are resonating quartz crystals with a resonant frequency that decreases when mass is added to the surface of the crystal. QCMs are often used to monitor the growth rate during PVD and CVD, but the resonant frequency of standard "AT cut" crystals is very sensitive to increases in temperature making them poorly suited for ALD growth at temperatures above 200 ºC. The quartz crystal used in this system is an "RC cut"

crystal (Colnatech) specifically designed to withstand higher temperatures than "AT cut" crystals. **Fig. 2.4**. shows the output from our QCM (**Fig. 2.4** top) and the pressure inside the chamber (**Fig. 2.4** bottom) as the sources are pulsed for 4 cycles. The first peak corresponds to a water exposure, and the exchange of CH_3 groups for OH groups, so the mass on the crystal changes very little, ~2 Hz/cycle. However, the second peak is a TMA dose, which corresponds to the deposition of Al, and as such the QCM frequency drops significantly, ~7 Hz/cycle. The sharp peaks in the QCM data are transient noise in response to the sudden change in chamber pressure. The QCM data shows a steadily decreasing linear trend at ~9 Hz/cycle, and the pressure pulses show consistent duration and magnitude. The QCM is therefore sensitive to sub-Angstrom changes in thickness and confirms that ALD growth is occurring consistently throughout the deposition.

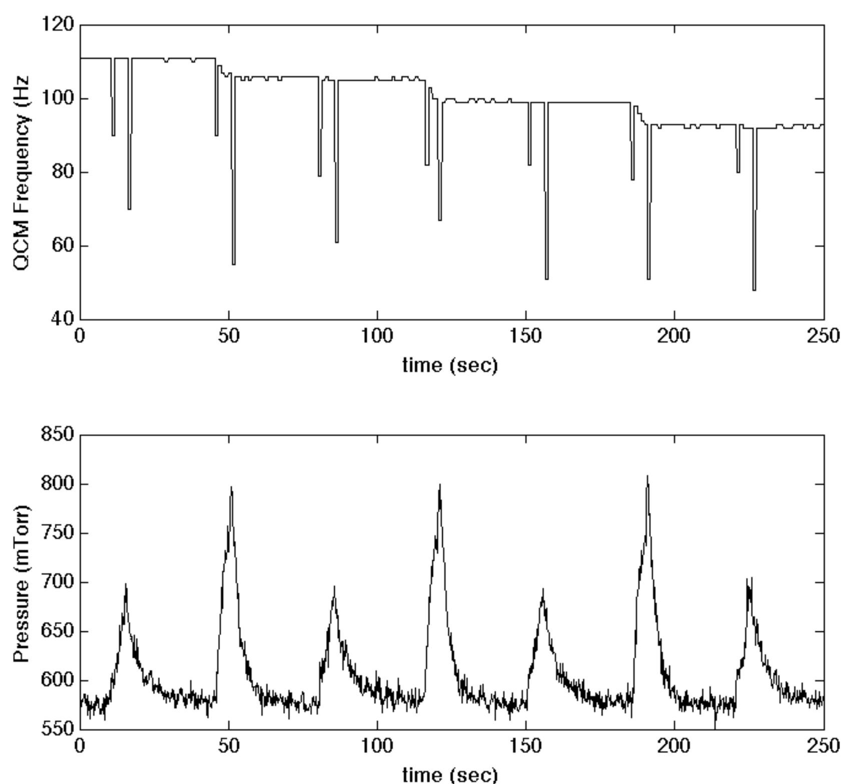


Figure 2.4 QCM frequency (top) and pressure data (bottom) of 4 ALD cycles. The QCM frequency drops ~9 Hz/cycle. The sharp spikes in the data are noise caused by a sudden increase in chamber pressure. The first pulse in the pressure data is H_2O, followed by TMA, and so on. The QCM frequency drops correspond exactly in time to the pressure pulses.

2.2.1.3 Sputtering Chamber

On the other side of the load lock from the ALD chamber is the sputtering chamber. It is made from 20 inch OD stainless steel cylinder and is continuously kept at UHV, with a base pressure of ~10^{-8} Torr or better with baking, by a cryopump (CTI cryogenics). The deposition pressure is controlled by a throttle valve (MKS type 653) and a mass flow controller (MKS type 1159B), and is typically 10-100 mTorr. The pressure inside the chamber is sensed with a micro-ion gauge (Brooks Automation) for high vacuum up to 10^{-10} Torr, a convectron gauge (Brooks Automation) for low vacuum from atmospheric pressure to 10^{-4} Torr, and a capacitance manometer gauge (MKS Instruments) to accurately cover the sputtering pressure range. Multiple

gas lines, including Ar, N_2, and O_2, enable sputtering of elemental sources, nitrides, and oxides. There are three magnetron sputtering guns in the chamber, two 3 inch guns and one 2 inch gun (Torus® from Kurt J. Lesker). The sputtering guns are mounted 90º apart and with their central axes 6 inches from the center of the chamber. They can be driven either with DC or RF power supplies. The DC power source (MDK 1.5K from Advanced Energy) has a useful range of 14 – 1500 W, while the RF power source (R601 from Kurt J. Lesker) has a useful range of 8 – 600 W at 13.56 MHz. The docking coupler in the sputtering chamber is a chilled-water cooled, copper U-shaped hard-stop which allows the sample chuck to enter and lock in place. The stage can be cooled to ~8 ºC, which is critical for depositing stress-free Nb films with good superconducting properties. The temperature is sensed with a k-type thermocouple (Omega Co). The stage, which rests ~6 cm above the sputtering target surface and on the central axis of the entire ALD-UHV sputtering system, can be manually moved into and out of the sputtering plasma with a rotating handle. This allows controlled exposure to individual sputtering guns. With three sputtering guns installed in the chamber, a wide variety of multilayer films may be grown including Al-wetted Nb, which is essential to $Nb/Al/Al_2O_3/Nb$ JJs.

2.2.1.4 Load Lock Chamber

Integrating the UHV sputtering chamber with the ALD chamber was achieved through a load lock. The load lock, pictured in **Fig. 2.5a** and **Fig. 2.5b**, is made from an 8 inch OD stainless steel tubing with 10 inch CF flanges on its top and bottom, a 6 inch CF gate valve on its left that interfaces with the sputtering chamber, and a 4.265 inch CF gate valve that interfaces with the ALD chamber. It can be brought to ~10^{-6} Torr in 10 minutes by a mechanically backed turbomolecular pump (TMP) from Edwards (nExt 240). This pressure can be held with an ion pump (Kurt J. Lesker LION 301) for vibration reduction. The pressures are sensed with a

convectron gauge for low vacuum and a cold cathode gauge for high vacuum. An O-ring sealed door is installed on the front of the load lock for easy sample installation and removal.

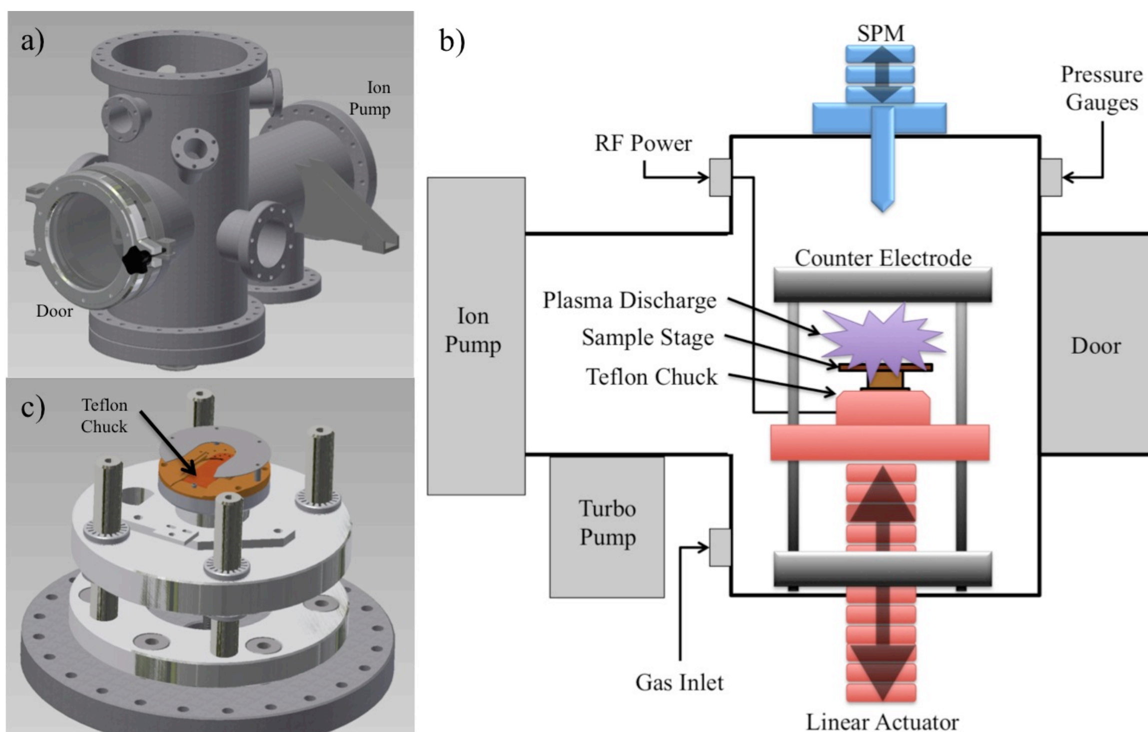


Figure 2.5 Engineering drawings of an external view of the load lock chamber (a), a schematic cross section of the load lock (b), and engineering drawings of the adjustable height chuck inside (c). The load lock (a, b) is crafted from an 8 inch OD stainless steel tube. The door on the front is sealed with an O-ring and allows for quick and easy transfer of the sample stage. The 10 inch flange on top is designed for scanning probe microscopy instrumentation such as atomic force microscopy or scanning tunneling microscopy. The rear flanges are for the installation of a turbomolecular pump for fast pumping and an ion pump for a vibration free vacuum. The sample chuck (c) is fitted with a Teflon, U-shaped hard stop so the sample stage can lock in place. Teflon was chosen to electrically isolate the sample from the chamber during RF plasma treatments. The chuck's height is adjustable so that the sample may be engaged by instrumentation, or to adjust processing parameters during a plasma treatment.

Beyond its key role in connecting the ALD and sputtering chambers, the load lock has a docking chuck for RF plasma treatments, pictured in **Fig. 2.5b**. The coupler chuck, pictured in **Fig. 2.5c**, is made entirely of Teflon and has a U-shaped hard-stop identical to that in the sputtering chamber. A copper-beryllium spring rests inside the chuck to make electrical contact with the sample stage. A 20 gauge copper wire was driven through the Teflon to connect this spring with an RF electrical feedthrough to electrically isolate the sample stage from the

chamber. Thus, during RF plasma treatments, the sample stage itself acts as one electrode. A removable, grounded stainless steel plate can rest above the docking chuck to act as the counter electrode. The distance between the sample stage and this steel plate can be controlled by a 6 inch stroke linear actuator which moves the chuck vertically (LSM from Kurt J. Lesker). The plasma is driven with an RF power supply and matching network (R601 from Kurt J. Lesker). Gas lines supply either O_2, N_2, or Ar for a variety of plasma treatment options including oxygen plasma cleaning and Ar ion milling. A metered gate valve on the TMP allows control of the load lock pressure. At 30 mTorr of Argon, 150 W RF power, and a sample-to-electrode distance of 3 cm, an ion etch rate of 1 nm/min for Nb has been measured. An *in situ* plasma stage is indispensible to tunnel junction fabrication since hydrous plasma treatments are critical for achieving a quality interface when growing ALD films on noble metals, [45] and ion milling is often required to remove native oxides from metal films to make good electrical contact, i.e. Nb during JJ fabrication.

In addition to *in situ* plasma cleaning, this load lock was designed for *in situ* sample characterization with scanning probe microscopy (SPM), particularly RHK Technology's line of atomic force microscopes (AFM), the designed placement of which is pictured in **Fig. 2.5c**. The U-shaped chuck in the load lock is compatible with RHK's sample chuck for easy sample transfer. The linear shift on this stage can raise the sample to the scan head, which could be mounted on the 10 inch CF flange on top of the load lock. Further, the ion pump in the chamber would allow for *in situ*, vibration free, high vacuum characterization of sputtered and ALD films at various points in their growth. Beyond AFM, the load lock could be configured for scanning tunneling microscopy or spectroscopic ellipsometry, which would provide valuable insight into the microstructure, electrical, and optical properties of ALD films as they grow.

2.2.1.5 Sample Transportation

Seamless integration of the chambers, and transportation between them, is a critical function of this system. Each chamber is connected to its neighbors by a CF flanged circular gate valve. The ALD chamber uses the smallest gate valve on a 4.625 inch CF flange. The internal diameter of the valve is 3.52 inch, which sets the maximum sample stage diameter. However, this dimension could easily be increased by choosing a larger OD for the ALD chamber. Rectangular valves, or slot valves, are also available. But, the circular gate allows for a more versatile stage design, allowing easier integration with UHV-sputtering. The sample stage is moved through these gates, and from chamber to chamber, with a magnetically coupled linear shift (transport rod) from UHV Designs with a 3 feet stroke length.

The sample stage itself is shown in **Fig. 2.6** and has three main features of interest; the sample platform, the docking coupler, and the transportation coupler. The sample platform is a 2 inch copper disk with six equally spaced threaded holes on its perimeter which allow the sample to be clamped to the platform. Copper was chosen for its excellent thermal conductivity to create a uniform heat profile during ALD and water-chilled sputtering. The docking coupler is a copper, U-shaped protrusion screwed to the sample platform, and it acts as the male half of the stage docking mechanism. The U-shape allows for hard-stop docking in the sputtering chamber and load lock chucks, and it is compatible with RHK UHV scanning probe microscope systems. Slots are cut into the walls of this protrusion to allow soft-stop docking with the ALD chamber's rails. The stage transportation coupler is a stainless steel threaded hole that mates with the terminating screw on the transport rod (rod transportation coupler). This stage design, along with the hard-stop and soft-stop docking couplers in the sputtering chamber, load lock, and ALD chamber, allow for easy and reliable sample transfer from chamber to chamber.

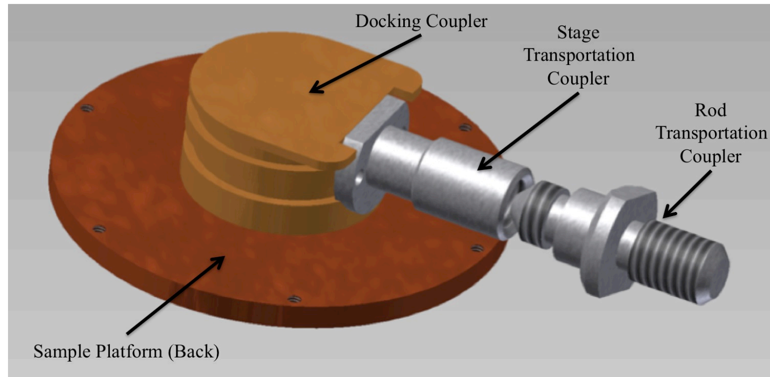


Figure 2.6 An engineering schematic of the sample stage. The sample is mounted onto the bottom side of a 2 inch disk of copper, chosen for its thermal conductivity. The docking coupler, also made of copper for its thermal conductivity, is screwed onto the 2 inch disk. The coupler's U-shape mates with the hard-stop chucks in the sputtering chamber and load lock, and it is compatible with RHK UHV scanning probe microscopy systems. Slots are cut into the side of the docking coupler to catch the mounting rails in the ALD chamber. The stage transportation coupler is stainless steel, and it is screwed to the back of the docking coupler. The rod transportation coupler is also stainless steel, and its dovetail shape helps to engage the sample stage.

2.2.2 Trilayer Deposition Description

As a proof of concept of this ALD-UHV sputtering system, Nb/Al/ALD-AL_2O_3/Nb trilayers were fabricated. First, the Nb and Al films were sputtered as presently described. Next, the sample was transferred *in vacuo* to the ALD chamber where it was heated to the deposition temperature. Finally, the top Nb film was sputtered to create the trilayer.

The Nb films were sputtered under conditions to optimize the Nb's superconductive properties, e.g. the gap energy. To do this, care was taken to reduce impurities in the film and to minimize the intrinsic stress in the films. A fast deposition rate, which depends on the pressure in the chamber, the power delivered to the sputtering gun, and the distance between the sample and the sputtering gun, is required to minimize the formation of NbOx from traces of oxygen in the sputtering chamber. NbOx has three oxidation states[25]; one is conducting, one is semiconducting, and the last is insulating [26, 27], so preventing the formation of NbOx is critical to reproducible junction fabrication. The intrinsic stress in DC sputtered Nb films is a function of the pressure in the chamber, the temperature of the sample, and the bombardment energy with which the Nb atoms strike the sample surface [54]. Optimized parameters for high

quality, stress free niobium were found. The sputtering power was 330 W (46 W/in^2), the pressure was 14 mTorr Ar, and the sample-to-gun distance was 6 cm. The samples were cooled for 45 minutes before sputtering began and for an additional 45 minutes after each 60 seconds of sputtering to maintain a sample temperature of 8 °C. The bottom Nb film was sputtered to 150 nm, and the to Nb film was sputtered to 50 nm.

The Al wetting layer was sputtered under conditions to optimize the formation of the tunnel barrier. Unlike Nb sputtering, there are no stringent requirements to consider. The wetting layer need only be thick enough to facilitate nucleation of the Al_2O_3 film and to protect the underlying Nb film from oxidation. The Al films were sputtered at 90 W (13 W/ in^2) in 14 mTorr Ar at a sputtering rate of 0.5 nm/sec to a thickness of 7 nm.

The sample was then transferred *in vacuo* to the ALD chamber where the tunnel barrier was grown. The ALD growth parameters were chosen to minimize the formation of a thermally oxidized interfacial layer between the Al film and the ALD-Al_2O_3 film. To minimize thermal oxidation during the heating stage, the samples were heated under high vacuum using the TMP in the load lock over the course of 2 hours. Once the operating temperature of 200 °C was achieved, high purity N_2 gas was fed into the chamber at 5 sccm for an operating pressure of ~ 600 mTorr. H_2O and TMA were then pulsed into the chamber sequentially for 1 second each producing pressure pulse heights of ~300 mTorr above the base pressure. After ALD growth, the samples were cooled to ~50 °C over the course of 30 minutes . The samples were then transferred back into the sputtering chamber for deposition of the top Nb layer, completing the Nb/Al/ALD-Al_2O_3/Nb trilayer.

The surface morphology of these trilayers was studied with contact mode atomic force microscopy (AFM). The AFM characterizations show the surface roughness of the bottom Nb

layer was not substantially increased by growing ALD-Al_2O_3 on top of the Al wetting layers. The surface of the bottom Nb layer is smooth with an average roughness R_{rms} of ~1 nm. The Al wetting layers still have comparable smoothness with R_{rms} of ~1.1 nm. With 14 cycles of ALD-Al_2O_3 the R_{rms} is ~1.3 nm. These morphologies confirm that ALD growth does not significantly damage the smoothness of the base surface and excludes the possibility of island growth modes.

CIPT measurements [55] were taken on the unpatterened trilayers to confirm the integrity of the tunnel barrier at room temperature. CIPT measurements were performed on trilayers with the number of ALD cycles ranging from 2-20. A monotonic increase of the tunneling resistance with the number of the ALD cycles was observed [56]. In addition, uniform tunneling resistance with a small standard deviation of less than 10% was observed on most samples with diameters up to 50 mm confirming good control of the tunnel resistance by varying the number of ALD cycles.

2.3 Josephson Junction Device Processing

2.3.1 Josephson Junction Device Processing Overview

Selected trilayers were processed into JJs using a 12 step process flow, shown schematically in **Fig. 2.7**. To briefly summarize, the trilayers are patterned using photolithography to define the main wiring of the JJ circuit (**Fig. 2.7b**). A combination of reactive ion etching (RIE) and wet etching is used to etch through the entire trilayer (**Fig. 2.7 c-e**). The photolithography mask is then removed, and electron beam lithography (EBL) and RIE are used to define the JJ mesa (**Fig. 2.7 f-g**). The JJ is then insulated with evaporated SiO_2, which is lifted off (**Fig. 2.7 h-i**). EBL is used to define the top wiring of the JJ, and Nb is sputtered and lifted off to complete the device (**Fig. 2.7 j-l**). **Fig. 2.8** shows micrographs and profilometry of the devices during processing (a-f) and the finished devices (g,h).

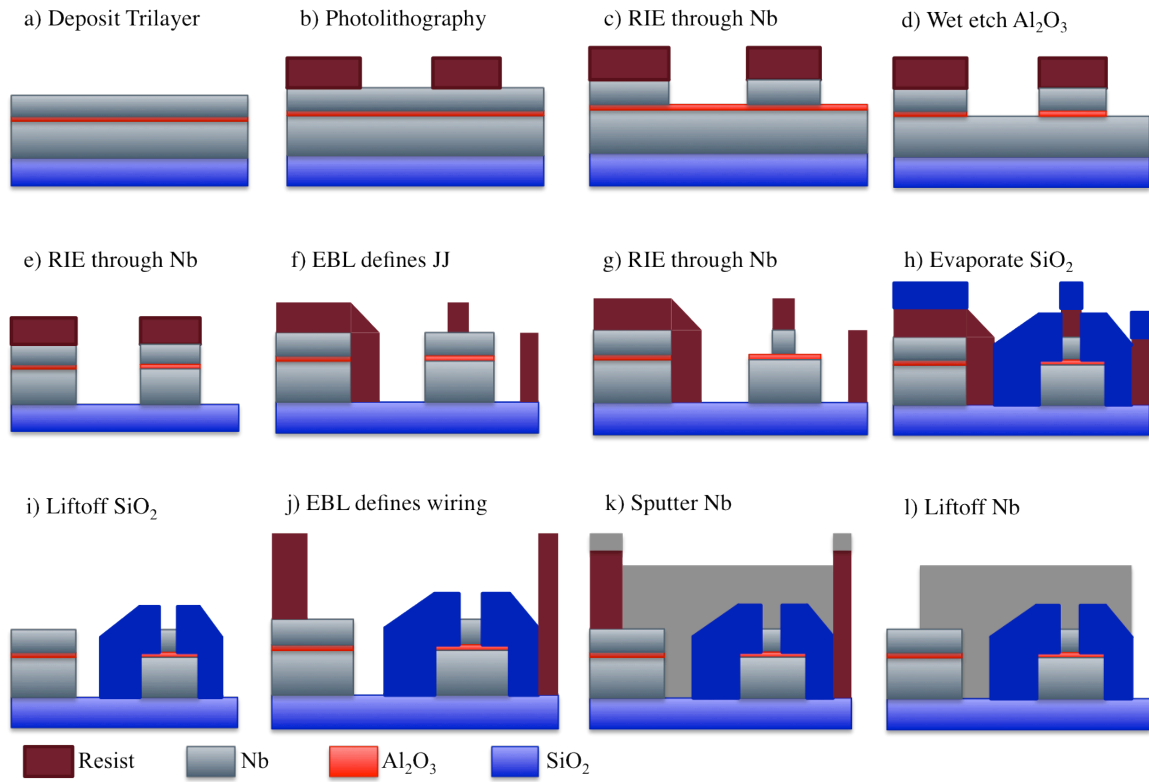


Figure 2.7 Schematic diagram of Josephson junction process flow.

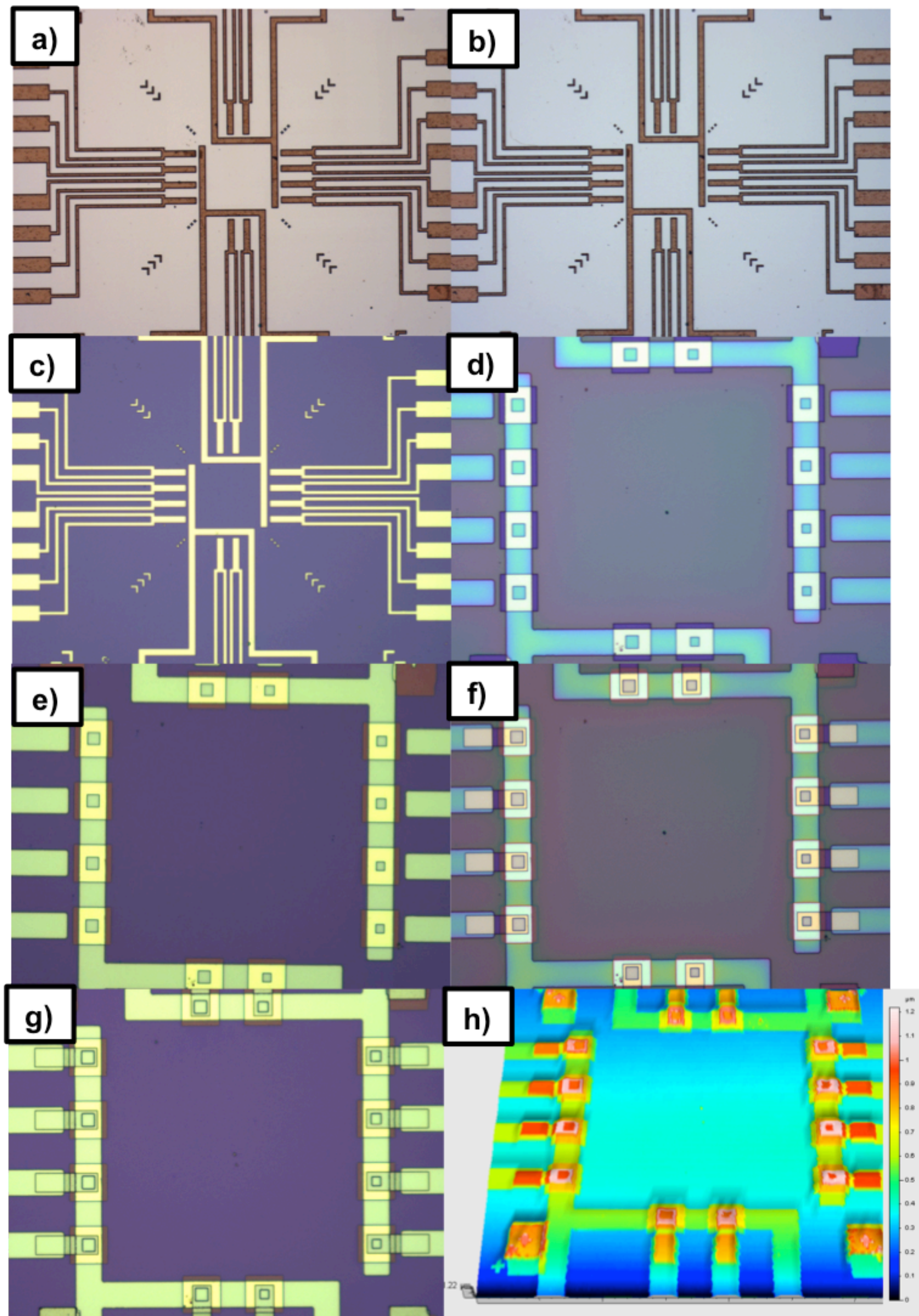


Figure 2.8 Micrographs (a-g) and 3D profilometry (h) of a sample JJ during key points of the process flow. (a-c) show 10x micrographs of the JJs after photolithography, wet etching, and the 2nd RIE, respectively. (d-g) show 20x micrographs of the JJs after the first EBL, SiO2 liftoff, 2nd EBL, and Nb liftoff, respectively.

2.3.2 Photolithography

Photolithography was used to define the main wiring of the JJ circuit, and the photomask used is shown in **Fig. 2.9**. The photomask was designed for a 4 point measurement of 12 JJs on each circuit. The pads on the perimeter of the photomask were designed to allow for triply redundant wirebonding on each pad. Each JJ has a pair of smaller pads associated with it that act as the I_+ and V_+ terminals in the 4 point measurement. The larger pads serve as I_- and V_-, and each pair of large pads is shared among 6 JJs. To begin the photolithography process, the trilayers were diced into 15 x 15 mm squares, large enough to fit four of the patterns shown in **Fig. 2.9**. These samples were then spincoated with S1813 photoresist (Shipley) at 4000 rpm for a resist thickness of 1.3 µm. The resist was softbaked at 90 °C for six minutes before exposure to a 500 W UV lamp for 80 sec. The samples were developed in a 1:3 solution of M351 microposit developer and water for 100 sec. The samples were then rinsed in deionized water and blown dry with N_2.

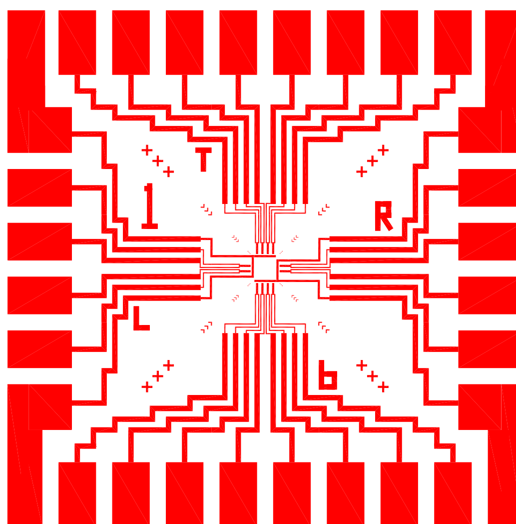


Figure 2.9 Photomask used to define the main wiring of the JJ test circuit. Each JJ has a dedicated pair of electrodes, and 2 groups of 6 JJs share two ground electrodes. In this manner, each JJ can be measured with a four point configuration.

2.3.3 Trilayer Etch

RIE and wet etching were used to etch through the trilayer (**Fig. 2.7 c-e**). RIE was used to etch through the Nb films of the trilayer. The films were etched in 15 mTorr of SF_6 at 50 W RF. The etch rate for Nb was approximately 0.5 nm/sec. Because of nonuniformities in the etch rate due to fluctuations in pressure, power, and chamber cleanliness, a series of optical checks were developed to ensure the etch was complete. When etching through the top Nb, the sample turned brown just before the etch was complete, and regained a silvery color when the Al_2O_3 layer had ben reached. Likewise when etching through the bottom Nb, the etch proceeded until the underlying SiO_2 was revealed, and its color matched the original wafer's color. The etch times for the top and bottom Nb layers were ~90 sec and ~120 sec respectively.

Since neither Al nor Al_2O_3 etch in SF_6 RIE, wet etching was used to etch through the Al and Al_2O_3 layers (**Fig. 2.7 d**). H_3PO_4 was selected as the etchant because it etches both Al and Al_2O_3 but does not etch photoresist. Commercial 85% H_3PO_4 was diluted with deionized water to a concentration of 8%. The etch rate was approximately 0.04 nm/sec. The samples were placed in a carrier and submerged into the H_3PO_4 solution. The solution was mildly agitated for 5 minutes, then the samples were rinsed in deionized water and blown dry in N_2. Immediately after, the samples were placed back in the RIE chamber to complete the etch through the trilayer.

2.3.4 Josephson Junction Mesa Definition

EBL was used to define the active area of the JJ, also called the JJ mesa. Square JJs with lateral dimensions ranging from 5 – 10 μm were written onto the pattern defined by the trilayer etch process. ZEP520A EBL resist (Zeon Chemicals) was spincoated onto the samples at 1000 rpm for a thickness of ~ 1 μm. This is thicker than typical processes with ZEP520A to facilitate liftoff of SiO_2, described presently. The resist was then exposed to an electron beam and

developed to reveal the pattern (**Fig. 2.7 f**, **Fig. 2.8 d**). This pattern was used as a mask for a third round of RIE, following the aforementioned recipe, to define the JJ mesa (**Fig. 2.7 g**).

After definition of the mesa, the JJ must be electrically insulated. To isolate the JJ, the same EBL mask was used for SiO_2 liftoff. Immediately after the third RIE, the sample was mounted to a water cooled stage with silver paste and loaded into an evaporation chamber. SiO_2 was evaporated onto the sample at operating pressures were on the order of 10^{-6} Torr with deposition rates of approximately 5 nm/sec, monitored *in situ* with a quartz crystal monitor. To ensure a consistent deposition rate and film quality, fresh SiO_2 was ground into a powder before each deposition and placed into the evaporator's crucible. After the evaporation was complete, the sample was brought to room temperature gradually over the course of 30 minutes, after which it was removed from the evaporation chamber.

Liftoff was then performed on the sample to remove excess SiO_2. Prior to liftoff, the silver paste left on the sample was removed by rinsing in acetone. The sample was then placed in ZDMAC, which strips ZEP520A, for 3 hours. This long soaking time was found to reduce the ultrasonication time required, which in turn increased device yield. After soaking, the sample was suspended in solution and ultrasonicated for 60 seconds. The resulting films are shown in **Fig. 2.8 e**.

2.3.5 Top Wiring

To finish the devices, the top of the JJ mesa must be electrically connected to the wiring leads defined by photolithography. A second round of EBL was used to define the area of the top wiring, shown in **Fig. 2.7 j** and **Fig. 2.8 f**. During processing, the top Nb film was exposed to air and chemicals, producing a dirty NbOx native oxide. This top oxide layer was removed with plasma etching in the load lock chamber (**Fig. 2.5**) before Nb was sputtered onto the samples.

During plasma cleaning, the sample was placed 2 cm away from the top electrode, and an 80 W RF plasma was ignited from 30 mTorr Ar. The samples were cleaned for 2 minutes, then transferred into the sputtering chamber for the deposition of 300 nm. Liftoff was then performed to complete the device.

2.4 Measurement Description

2.4.1 Room Temperature Measurements

Current-voltage characteristics (IVCs) were taken at 300 K for quality control and analysis. The measurement description is presented here, and the data are discussed in Chapter 4. IVCs were taken using a 4-point configuration shown in **Fig. 2.9**. A semiconductor device analyzer (Agilent B5015A) was used to obtain the IVCs. 25 μm diameter tungsten probes were connected to four channels of the device analyzer. These probes were moved from pad to pad inside a homemade chamber equipped with linear motion controls with micrometer precision. The JJs were current biased from 0 – 100 μA, and the voltage was measured. From the slope of the IVC, the JJs' room temperature resistances (R_{300K}) were calculated. The measured resistance includes some residual resistance from the wiring leads, it is not truly the normal state resistance (R_N) of the JJs. However these data are useful for quality checks. The product of the resistance and the area should be constant across the wafer, and the resistance itself should be inversely proportional to the area of the junction.

2.4.2 Low Temperature Measurement

Low temperature IVCs were taken to measure R_N and I_C, the normal state resistance and critical current, respectively. The JJs were mounted and wire bonded to a custom 24 pin sample holder, shown in **Fig. 2.10a**. The sample holder was placed in a homemade probe designed to minimize environmental noise. Shown in **Fig. 2.10b**, the probe tip uses pi-filters installed on

each pin to minimize high frequency noise. Each pin has 2 capacitors, 1 nF each, isolating the pin from ground. A resistor of 250 Ω was placed between the pin and capacitors to complete the pi-filter with a cutoff frequency of 4 MHz. Photographs of the probe tip and the sample holder inserted into the probe tip are shown in **Fig. 2.11.** The entire probe is approximately 6 feet long with a 0.9 inch diameter designed to fit inside a liquid helium (L-He) dewar. 24 wires lead from the probe tip to the top of the probe, where they connect to a 27 pin Fisher connector. These wires are twist paired to reduce magnetic coupling to the environment. The entire assembly is then inserted into an L-He dewar to cool the sample to 4.2 K.

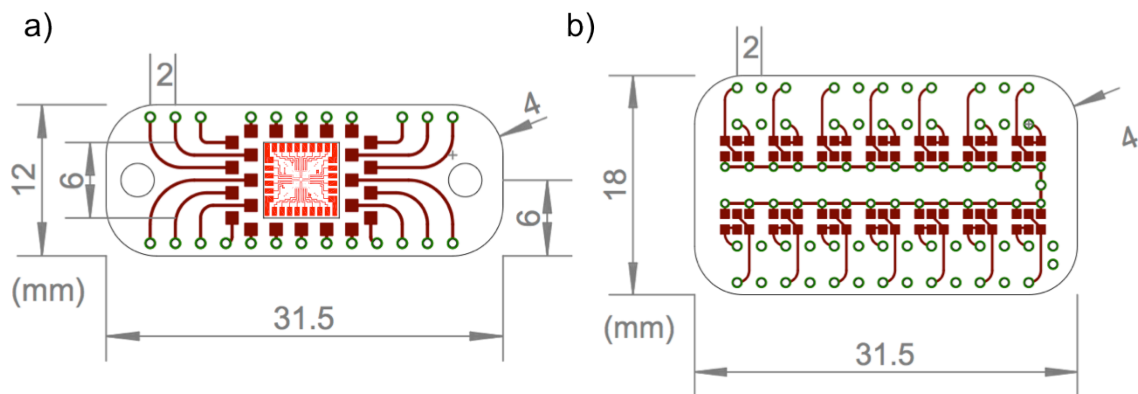


Figure 2.10 : Engineering schematic of sample holder (a) and probe tip (b) used for low temperature measurements.

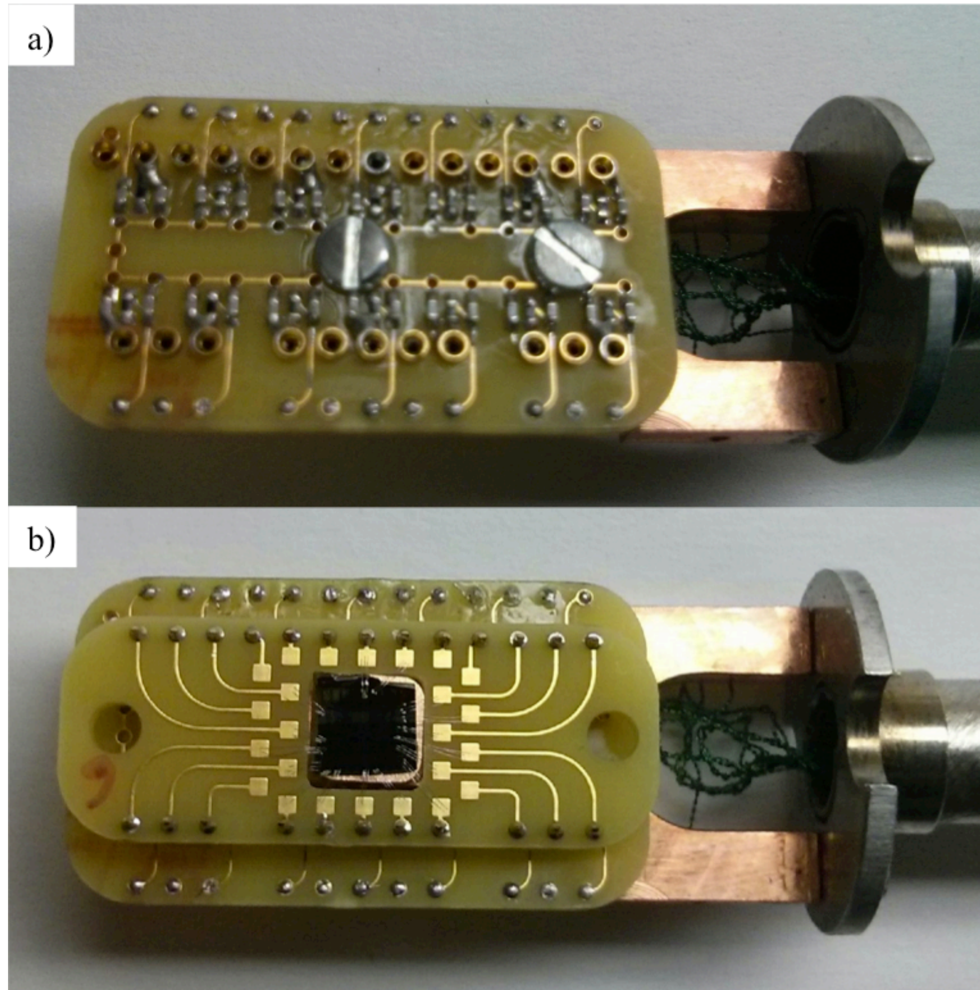


Figure 2.11 Photographs of the empty probe tip (a) and a sample wire bonded to a sample holder and placed inside the probe tip. (b)

A schematic of the low-temperature measurement system is given in **Fig. 2.12**. The JJs were current biased with a function generator (Agilent 33120A) running a 10 Hz triangle wave with a variable amplitude from 50 mV – 12 V. The current to the JJ was limited with a limiting resistor (R_L in **Fig. 2.12**) which could be set to 1 MΩ, 100 kΩ, 10 kΩ, 1 kΩ ,100 Ω, or 0 Ω . The magnitude of the current was measured using a sensing resistor (R_S in **Fig. 2.12**) which could be set to 10 kΩ, 1kΩ, 100 Ω, 10 Ω, or 0 Ω. The voltage signals from R_S and the JJ were fed into independent low-noise amplifiers (UCSD PES 010720), and the data was collected using either an oscilloscope (Tektronix TDS 2012B) or data acquisition system (Agilent 34970A). The amplitude was varied from sample to sample to achieve the best measurement in two separate

regions of the JJs IVC. Low voltage ($|V| < 3$ mV) scans were performed to measure the subgap region of the IVC with high resolution. Higher voltage scans were performed to achieve an accurate measurement of R_N, which requires voltages of 6Δ, or approximately 9 mV.

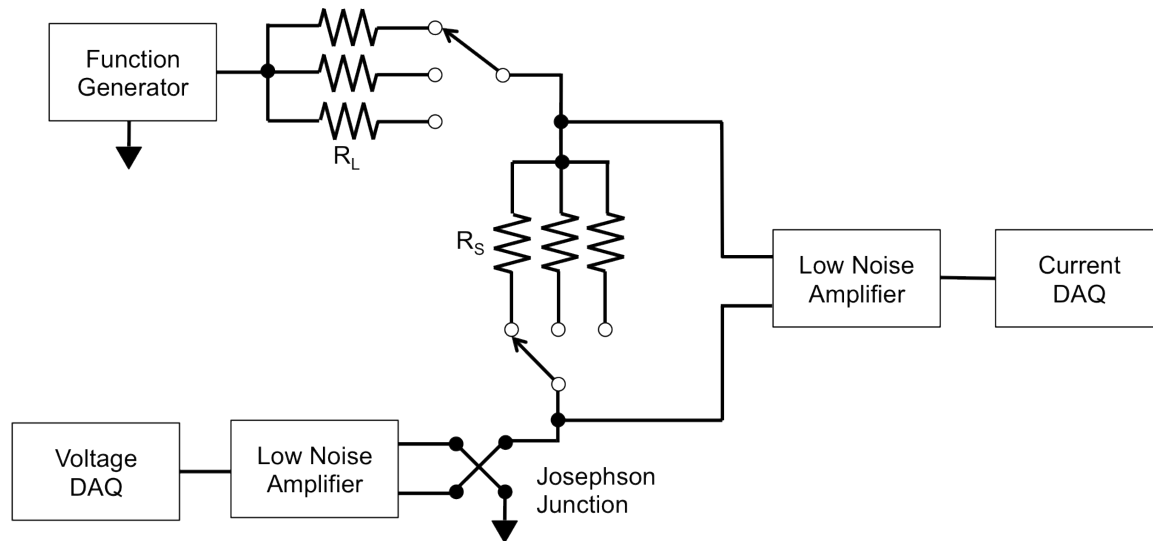


Figure 2.12 Schematic of measurement system for low temperature characterization. The junctions were current biased by a function generator, which produced a triangular wave at ~10 Hz. RL works as a current limiting resistor, and RS works as a sensing resistor to measure the current. The junction was wired in a 4-piont configuration to eliminate contact resistance from wire bonding. The voltage signals from RS and the junction were fed into low-noise amplifiers, and their output was supplied to a data acquisition system.

3 The Al / Al_2O_3 Interface

3.1 Chapter Overview

In this chapter, the interfaces relevant to JJs with ALD tunnel barriers are studied. In particular, the surface of ALD-Al_2O_3 films grown on Al, SiO_2, and Si were characterized with atomic force microscopy (AFM). The surfaces were found to be very smooth, with the ALD-Al_2O_3 film copying the surface roughness of its substrate. Further, the thickness of the ALD-Al_2O_3 films were measured with ellipsometry. By comparing the films grown on Al and SiO_2 substrates, evidence for an interfacial layer (IL) of up to 2 nm was found. By varying the thickness of an Al wetting layer on Si, it was found that the thickness of this IL depends on the thickness of the Al, confirming that the IL is caused by thermal oxidation of the Al substrate. The formation of this IL and its possible impacts on JJ devices is then discussed.

3.2 ALD-Al_2O_3 on Al

To study the surface morphology and IL of ALD-Al_2O_3 films on Al substrates, 50 nm Al was sputtered directly onto SiO_2(500nm)/Si(100) substrates at 90 WDC from a 3 inch sputtering gun in 14 mTorr Ar. 50 nm Al were used to ensure the film was optically opaque during ellipsometric studies. The Al films were then transported *in situ* to the ALD chamber, where 20 – 100 cycles of ALD-Al_2O_3 were grown. Separately, 5 – 100 cycles of ALD-Al2O3 were directly grown on SiO_2(500nm)/Si(100) substrates for reference. The surface roughness of the films was measured with an atomic force microscope (AFM) from WiTec. The thicknesses of the ALD-Al_2O_3 films were measured with a Horiba UVISEL spectroscopic ellipsometer (SE) between 2.75 eV and 4 eV.

Fig. 3.1 shows the surface morphology of the ALD Al_2O_3 films of various thicknesses grown on 50 nm thick sputtered Al measured using *ex situ* AFM over 5 μm x 5μm and 500 nm x

500 nm scan windows. The root-mean-square roughness (R_{rms}) was measured over the 5μm x 5μm scan area. **Fig. 3.1(a,e)** shows the Al substrate with no ALD growth. The native oxide on Al, formed when the sample was exposed to air, has an R_{rms} of 1.1 nm. Ripples can be seen with a lateral dimension of ~40 nm, a longitudinal dimension of ~100 nm, and height of ~5-10 nm. These ripples are randomly oriented and homogenously distributed across the surface. **Fig. 3.1(b-d, f-h),** show Al_2O_3 films obtained with 20, 60, and 100 cycles of ALD growth, on which an R_{rms} of 1.3 nm, 0.7 nm, and 0.8 nm were observed, respectively. The surface features on all samples are similar in size and shape. R_{rms} was measured over other scan windows, and comparable results were obtained. These data show there is no correlation between surface morphology and Al_2O_3 thickness in this regime. The comparable R_{rms} values across all samples and reappearance of surface ripples is confirmation that ALD Al_2O_3 growth is conformal on Al surfaces.

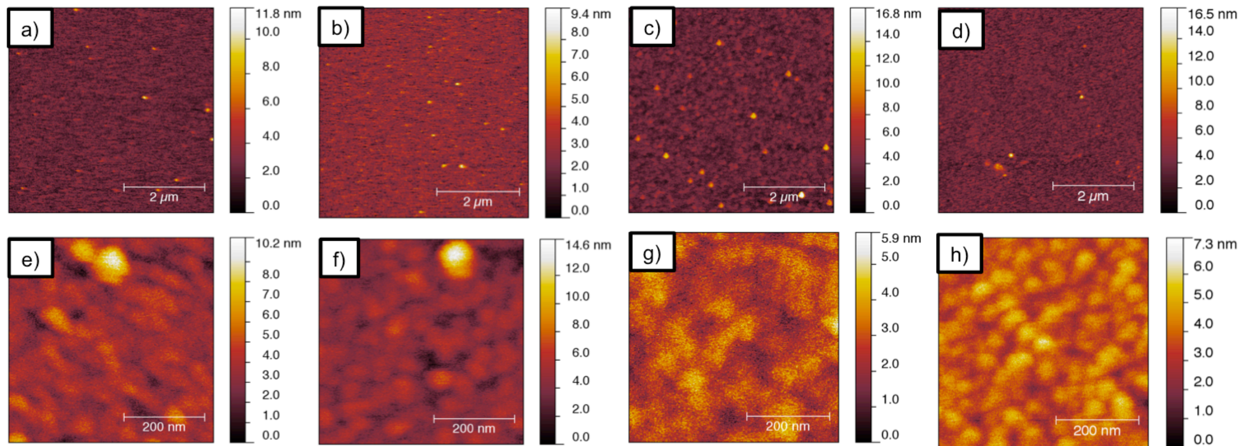


Figure 3.1 Atomic force microscopy of Al_2O_3 over 5 μm x 5μm (top row) and 500 nm x 500 nm (bottom row) scan windows. The native oxide on Al is shown in (a,e) with Rrms = 1.1 nm. (b,f) shows 20 ALD cycles, Rrms =1.3 nm. (c,g) shows 60 ALD cycles, Rrms = 1.1 nm. And (d,h) shows 100 ALD cycles, Rrms = 1.0 nm.

Fig. 3.2 shows the results of the SE study of the ALD-Al_2O_3 films of various thicknesses grown on SiO_2(500 nm)/Si and Al(50nm)/SiO_2/Si substrates. The red line shows the ALD Al_2O_3 growth rate on the SiO_2 surface is 1.2 Å/cycle calculated from the slope of the curve, which is

comparable to previously reported values [57]. The scatter in the data is a result of poor optical contrast between Al_2O_3 and SiO_2 due to their similar refractive indices. For sputtered Al substrates, exposing the film to ambient conditions for a few days formed a native oxide. This native oxide was measured to be 49 Å, and this set the lower limit for measuring ALD-Al_2O_3 on Al due to oxygen's ability to diffuse through thin oxide layers. The blue line in **Fig. 3.2** shows the ALD-Al_2O_3 growth rate on Al is also 1.2 Å/cycle, shown clearly in the figure since the two curves are parallel to each other. Thus, the growth rate of ALD-Al_2O_3 is independent of the substrate after nucleation for the case of SiO_2 and Al. However, there is significantly more growth of Al_2O_3 on Al than there is on SiO_2, which can be calculated by extrapolating the curve towards zero number of cycles. In fact, there is a systematic ~2 nm offset between the two curves. Since an equal growth rate was observed for ALD Al_2O_3 on Al and SiO_2 surfaces, this additional 2 nm of oxide on Al may be attributed to oxygen diffusion into Al. The oxidation of the substrate after the ALD fabrication may be ruled out as the cause of this IL since 20 cycles of ALD produced an Al_2O_3 film of comparable thickness to the native oxide. Further, since the thickness of the IL is less than half of the thickness of the native oxide, the difference may be attributed to the lower partial pressure of oxygen in the vacuum chamber for ALD as compared to the ambient atmosphere. In addition, a thinner IL was observed on trilayers with fewer number of ALD cycles[56], suggesting the IL thickness correlates to the ALD growth time at 200 °C consistent to the expectation of the thermal oxidation process [6]. Therefore, when ALD-Al_2O_3 is grown on Al substrates in excess of 20 ALD cycles, a 2 nm IL develops between the Al substrate and the ALD-Al_2O_3 film. This substrate is attributed to thermal oxidation during the ALD growth process.

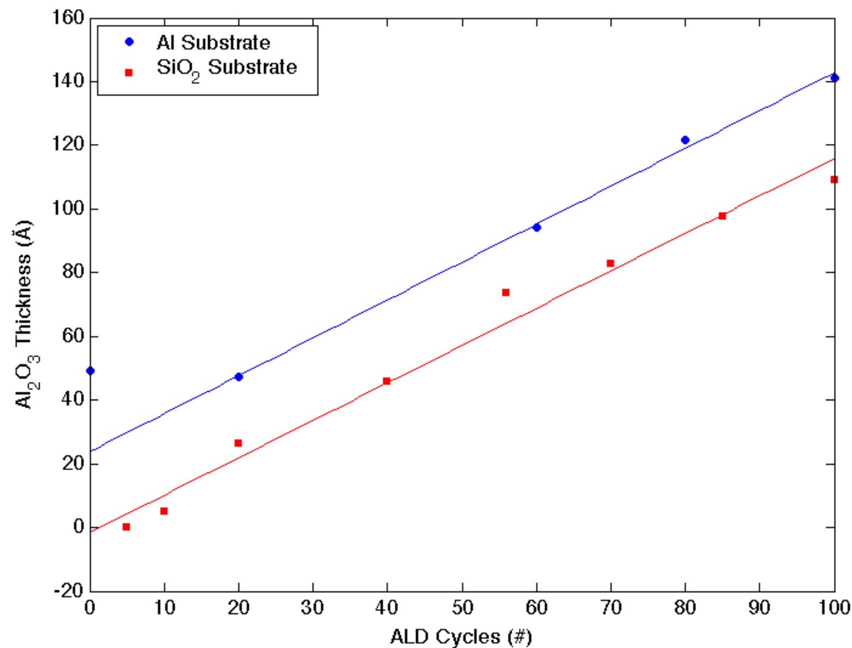


Figure 3.2 ALD-Al2O3 thickness vs. ALD cycles for Al substrates (blue) and SiO_2 substrates (red). The growth rate on both substrates is 1.2 Å/cycle, but ~2 nm of additional oxide has grown on Al substrates.

3.3 ALD-Al_2O_3 on Al-wetted Si(100)

To explore ways to reduce the thickness of this IL, a wetting layer of ultrathin (< 1 nm) Al was sputtered onto Si(100) substrates before ALD growth. **Fig. 3.3** shows the surface morphology of a bare Si(100) substrate **(a,e)** and 60 cycles ALD Al_2O_3 on a Si(100) with ultrathin Al wetting layers of approximately 1.4 Å, 3.5 Å, and 9.8 Å **(b,f; c,g; e,h)**, respectively. The thickness of the wetting layers was not directly measured. Instead, it was approximated using a previously calibrated sputtering rate. The R_{rms} values over 5 μm x 5 μm are 0.6 nm, 0.5 nm, 0.5 nm, and 0.4 nm, respectively. There is no apparent trend between the morphology and the wetting layer thickness. Furthermore, comparing **Fig. 3.1** to **Fig. 3.3**, the R_{rms} values of Al_2O_3 on ultrathin Al wetting layers is significantly smaller than on 50 nm Al. This is because R_{rms} for Si(100) is significantly smaller than R_{rms} for 50 nm Al, and because ALD growth is conformal. **Fig. 3.4** shows the Al_2O_3 thickness vs. wetting layer thickness. Interestingly, the Al_2O_3 thickness

decreases monotonically with the Al wetting layer thickness, confirming that the IL is indeed formed via oxidation of the Al surface layer. In particular, the IL could be almost removed and the surface roughness could be improved by using an extremely thin Al wetting layer.

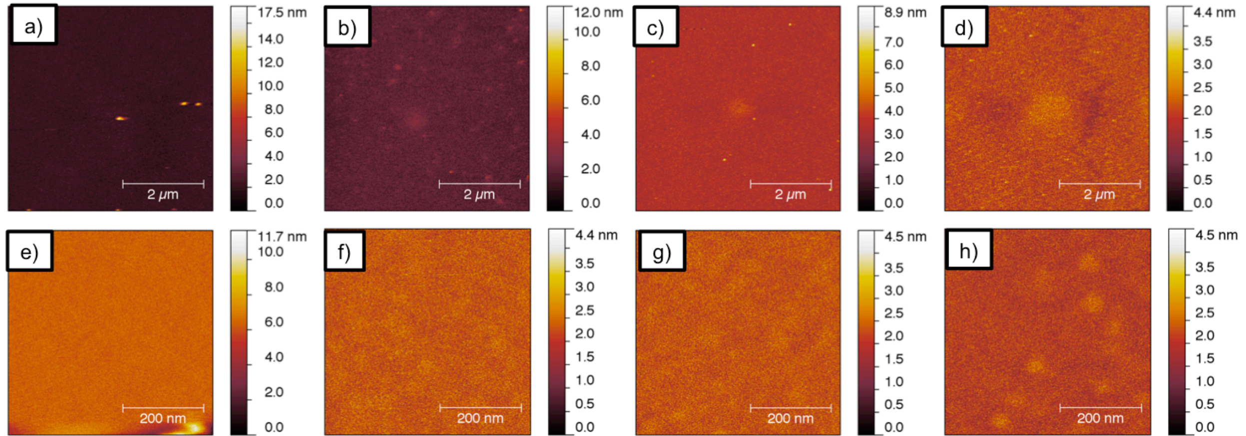


Figure 3.3 Atomic force microscopy of 60 ALD-Al2O3 cycles grown on Si(100) with ultrathin Al wetting layers over 5 μm x 5μm (top row) and 500 nm x 500 nm (bottom row) scan windows. (a,e) shows ALD-Al2O3 on bare Si(100), Rrms = 0.6 nm. (b,f) shows ALD-Al2O3 on 1.4 Å Al, Rrms = 0.5 nm. (c,g) shows ALD-Al2O3 on 3.5 Å Al, Rrms = 0.5 nm. And (d,h) shows ALD-AL2O3 on 9.8 Å Al, Rrms = 0.4 nm.

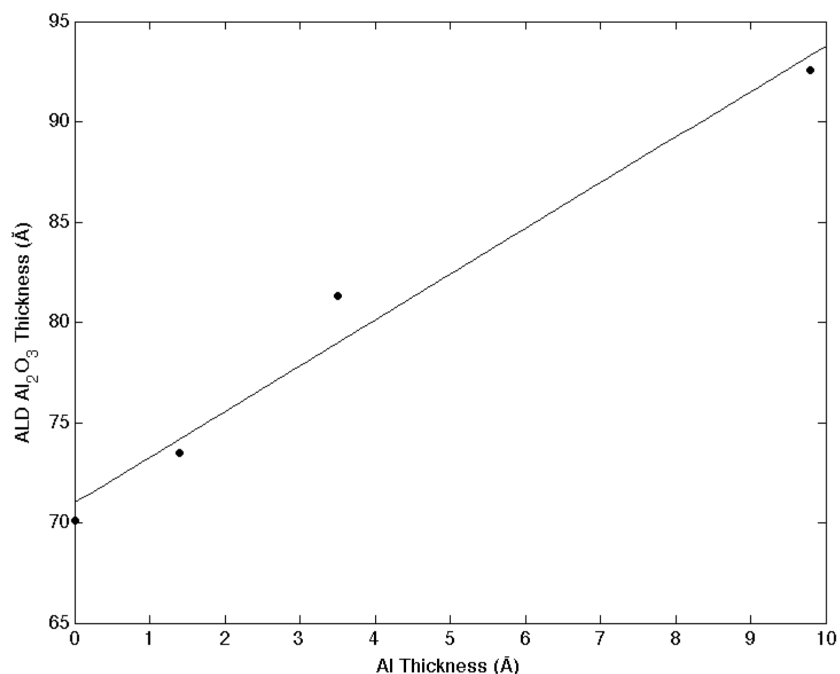


Figure 3.4 Spectroscopic Ellipsometry of 60 ALD-Al_2O_3 cycles grown on Al-wetted Si(100). The trendline is intended to be a guide to the eye and does not represent a rigorous model

3.4 Interfacial Layer Development

From the results in **Fig. 3.2** and **Fig. 3.4** it is clear that an IL develops between the Al and ALD-Al_2O_3 films, and this IL is caused by oxidation of the underlying Al film. However, it is not abundantly clear from these data when and how this IL develops. We hypothesize that this IL is thermally grown aluminum oxide (AlOx) that results from a combination of two growth mechanisms. The first mechanism is simple thermal oxidation while heating up the ALD chamber. In order to confirm this, a Nb/Al bilayer sample was heated to 200 ºC in the ALD chamber over the course of ~2 hours, but it was not exposed to the ALD reactions. Nb was sputtered on top to create an Nb/Al/Nb trilayer. Josephson junction (JJ) arrays were fabricated from this trilayer using the micro-fabrication procedure detailed in Chapter 2, and the current-voltage characteristics of these JJs were measured (presently discussed in Chapter 4). The

measured critical current density of 9.5 kA/cm^2 is far too large for a ~2 nm tunnel barrier, suggesting the formation of a substantial AlOx IL during ALD heating is unlikely. The second mechanism we propose, depicted schematically in **Fig. 3.5**, is diffusion oxidation during the ALD process, or "co-growth". Since a bare Al surface is exposed to H_2O at 200 ºC, some oxidation will occur. The total thickness of the AlOx IL depends on the temperature, the partial pressure of oxygen, and the total number of ALD cycles performed. This is in stark contrast to SiO_2 substrates, which are already densely packed with O_2, and their further oxidation is thermodynamically unfavorable under the conditions of ALD growth. We hypothesize that the additional ~2 nm of Al_2O_3 in **Fig. 3.2** can be explained by co-growth, and this mechanism is consistent with previous reports of high growth rates during the nucleation of ALD on other, easily oxidized metals [48-50].

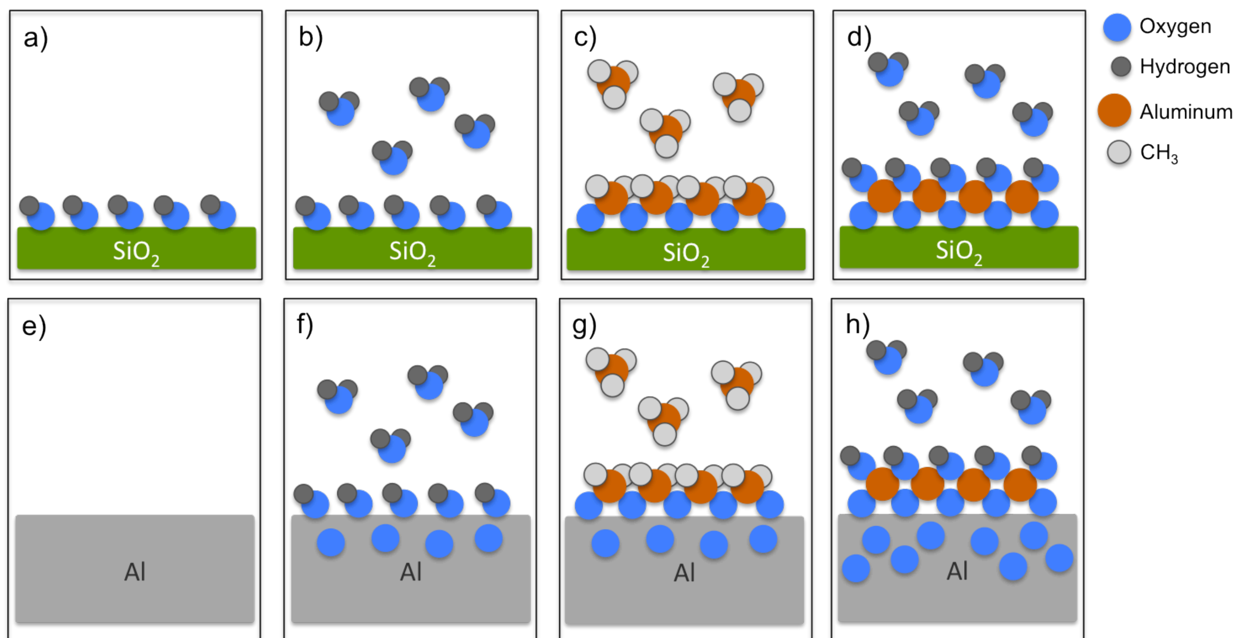


Figure 3.5 Schematic depiction of ALD-Al_2O_3 growth on SiO_2 (a-d) and Al (e-h) substrates. Since the SiO2 is densely packed with O_2, diffusion of O_2 into the SiO_2 is unlikely. However, a oxidation of a bare Al substrate is thermodynamically favorable when it is exposed to H_2O at 200 °C. Thus, during the H_2O pulses of ALD, (f,h), it is likely that O_2 from the H_2O pulse can diffuse into the Al film, causing a thermally oxidized AlOx interfacial layer. This could explain the difference in Al_2O_3 thickness seen in Fig. 3.2.

Ab-initio molecular dynamics (AIMD) simulations were used to study the changes in Al surface chemistry that occur after an H_2O pulse, and the results are given in **Fig. 3.6**. The AIMD simulations adopted the Bohn-Oppenheimer molecular dynamics implemented in VASP [58, 59] and used a 2x2 supercell of FCC Al under constant equilibrium volume and temperature (473 K). To simulate the initial Al surface, one H_2O molecule was placed on the supercell to simulate the expected traces of H_2O in the ALD chamber **(Fig. 3.6a**). After 6 ps of simulation time, no dissociation of H_2O into OH was observed (**Fig. 2.6b**). However, when multiple H_2O molecules were placed on the surface to simulate an H_2O pulse (**Fig. 3.6c**), dissociation occurred almost immediately. After only 3 ps of simulation time, the H_2O molecules dissociated into OH^- (**Fig. 3.6d**). We note the main mechanism of OH^- formation during this initial period of AIMD simulation appears to be proton transfer between molecules, forming H_3O^+, which almost instantly dissociates into H_2O_{ad} and H^+_{ad}. These simulations suggest the formation of Al_2O_3 becomes thermodynamically favorable under typical ALD processing conditions, even without the presence of TMA. These simulations corroborate the hypothesis that the observed IL in **Fig. 3.2** and **Fig. 3.3** is caused by thermal oxidation of the Al substrate.

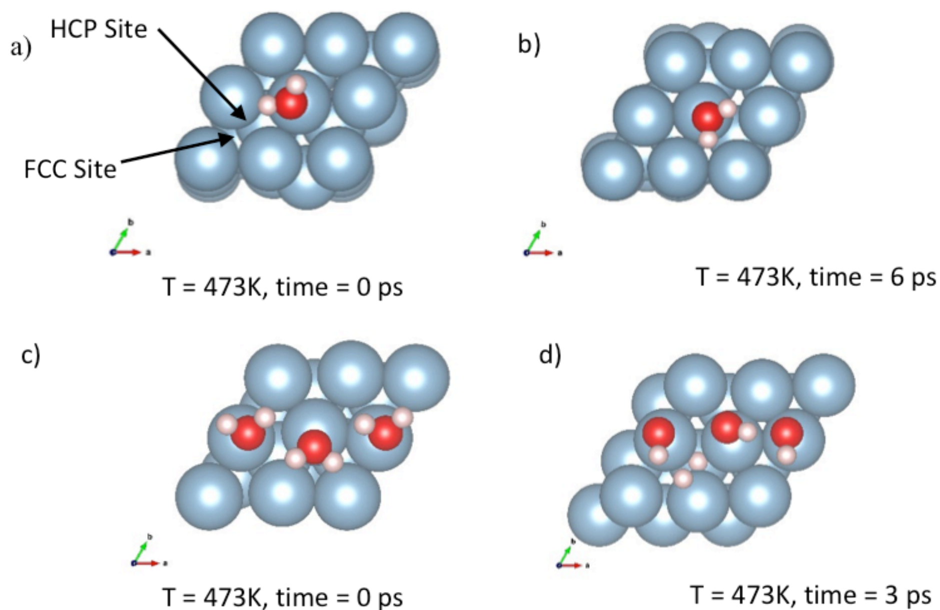


Figure 3.6 Ab-Inito Molecular Dynamics (AIMD) simulations of H_2O absorbing onto an Al surface. When only one H_2O molecule is present on the Al surface, dissociation is thermodynamically unforable (a,b). However, when H_2O molecules are in close contact with eachother on the surface, dissociation into OH and H is nearly instantaneous (c,d).

The two IL growth mechanisms, thermal oxidation before ALD growth and co-growth during ALD, in combination with oxidation upon exposure to ambient atmosphere, produce four scenarios for ultrathin ALD film growth on Al. **Fig. 3.7** is a cartoon representation of these scenarios. **Fig. 3.7a**, shows an AlOx IL formed from *in situ* oxidation that occurs during the ALD heating process from traces of H_2O in a heated chamber; a very thin oxide is formed on the Al surface. If an ALD film is grown that is too thin to prevent diffusion of ambient oxygen, then a native oxide will form from *ex situ* oxidation underneath the ALD film when the sample is removed (**Fig. 3.7b**). For longer ALD depositions and thicker films, ALD growth and diffusion oxidation will occur together during the ALD process, producing co-growth and a substantial AlOx IL (**Fig. 3.7c**). However, if a thin ALD film is grown and then capped with a diffusion barrier such as an Al or Nb top electrode (**Fig. 3.7d)**, both co-growth and ambient oxidation can be minimized, possibly producing a tunnel barrier that is dominated by ALD growth.

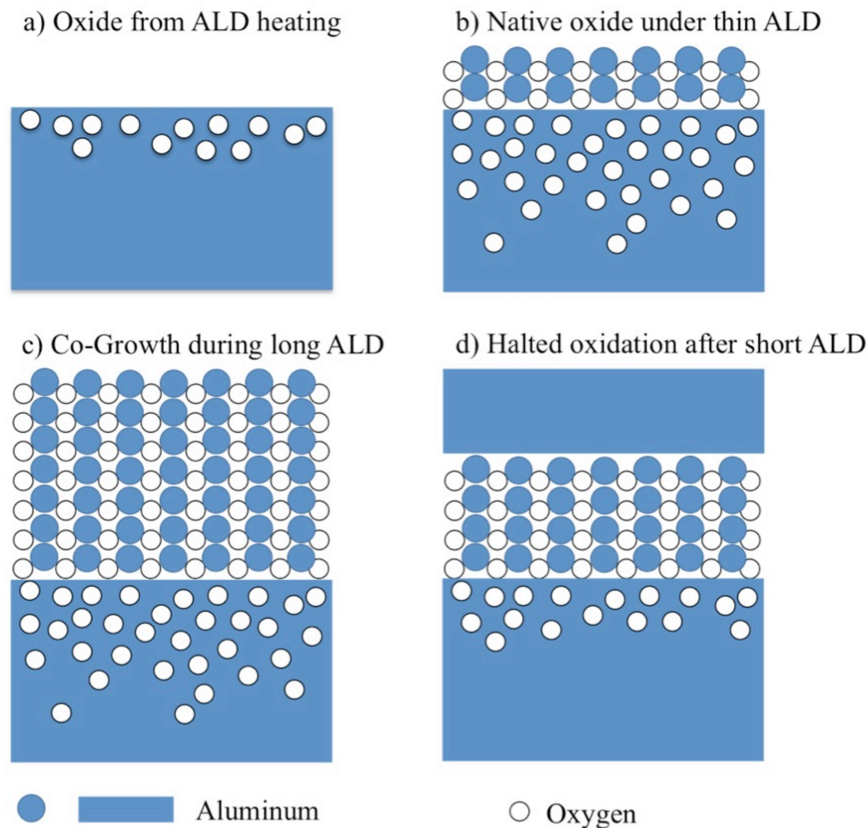


Figure 3.7 Four distinct oxidation regimes exist when growing ALD Al_2O_3 in situ on Al substrates. A very thin thermal oxide forms during the ALD heating process from trace H_2O in the chamber (a). If the ALD film is not thick enough to act as a diffusion barrier against ambient oxygen, a native oxide will form underneath the ALD film (b). During long ALD depositions, ALD growth and thermal oxidation occur together, which forms a significant interfacial layer (c). However, if a thin ALD film is capped with a diffusion barrier, both co-growth and ambient oxidation can be minimized (d), as is the case with tunnel junction fabrication.

Due to the thermodynamic favorability of Al_2O_3 formation in the ALD growth window, it is likely that the IL develops quickly and that substrate engineering will be necessary to grow a tunnel barrier dominated by the ALD film. One possible strategy is adding a diffusion barrier composed of a noble metal (e.g. Pd, Ag) between the substrate and the ALD film. Since oxidation of noble metals is thermodynamically unfavorable, the formation of the IL would be frustrated. However, since ALD nucleation is known to be difficult on noble metals [45-48], this diffusion barrier would require a wetting layer to facilitate nucleation of the ALD film. From **Fig. 3.4**, an ultrathin Al layer of only ~1 Å is sufficient for ALD-Al_2O_3 nucleation. This would

limit the thickness of the thermally oxidized IL to ~ 1 Å, an order of magnitude thinner than the tunnel barrier itself. Therefore, a wetting bilayer with a noble metal diffusion barrier and an ultrathin Al wetting layer is a possible strategy for producing ultrathin ALD tunnel barriers with minimized interfacial layers.

3.5 Conclusion

In conclusion, ALD-Al_2O_3 was grown *in situ* on sputtered Al, and SiO_2/Si substrates. AFM was used to confirm the ALD growth was conformal, and all R_{rms} measurements yielded values of ~1 nm. Through SE and by varying the number of ALD cycles, the growth rate was found to be 1.2 Å/cycle on both Al and SiO_2 substrates. However, a 2 nm IL developed on the Al substrates. By varying the thickness of Al films on Si(100) substrates, it was confirmed that this IL is due to the thermal oxidation of the Al film. We hypothesize that thermal oxidation and ALD growth are occurring in tandem on these substrates, and the IL thickness may be much smaller when thinner (~1 nm) ALD films are grown. AIMD was used to model the Al surface in the nucleation phase of ALD growth, and the model corroborates the hypothesis. Therefore, clever substrate engineering, such as adding a noble metal diffusion barrier, is likely necessary to minimize the IL in tunnel barriers.

4 Electrical Properties of Josephson Junctions with ALD Tunnel Barriers

4.1 Chapter Overview

In this chapter, the electrical characterization of Josephson junctions (JJs) with ALD tunnel barriers is presented. Trilayers were fabricated with tunnel barriers ranging from 0 – 10 ALD cycles and then processed into JJs. The JJs current voltage characteristics (IVCs) were taken at 300 K and 4.2 K. From the 300 K data, the junction resistance at room temperature (R_{300K}) and the junction specific resistance ($R_{300K}A$) were calculated to confirm the quality of the devices. From the 4.2 K data, the gap current density (J_G), and normal state resistance, R_N, were calculated. The expected exponential relationships were found between ALD cycles (i.e. tunnel barrier thickness) and the metrics J_G and R_NA. However, the data suggests the presence of an interfacial layer between the Al wetting layer and tunnel barrier that significantly increases R_N. Despite this challenge, the data confirm that ALD can be used to fabricate JJs with variable tunnel barrier thicknesses.

4.2 Introduction

The Josephson Junction (JJ), is a strong candidate for the implementation of quantum bits (qubits) due to its compatibility with modern semiconductor processing technology. But the tunnel barrier must be ultrathin (~1 nm) in order to maintain phase coherence across the superconducting electrodes and because the critical current through the JJ decays exponentially with tunnel barrier thickness [29]. Producing an ultrathin, uniform, and leak-free tunnel barrier is difficult on metal substrates due to the naturally formed native oxides on most metals. However, traditional JJ fabrication techniques have cleverly used the easy oxidation of Al to produce the

tunnel barrier by thermally oxidizing a thin (~5 nm) "wetting layer" of Al to form Nb/Al/AlO_x/Nb JJs. This thermal oxidation scheme has been used to create high quality JJs for commercial applications such as SQUIDs and voltage standards. [8, 60]. However, when JJs are employed for qubits, a more stringent requirement for lower noise arises to avoid superconducting phase decoherence, which makes meaningful quantum computation impossible. One major source of noise is two-level fluctuators (TLFs) in the insulating films of the qubit circuit [32]. Defects in the tunnel barrier arise from the process of thermally oxidizing aluminum and are a primary cause of TLFs [32, 35, 61, 62]. Recent efforts to reduce noise from TLFs have focused on either decoupling the qubit circuit from the environment by carefully designed microwave cavities or designing qubit circuits that can detect and correct errors caused by decoherence [33, 34, 63]. These efforts have made great strides in recent years, nearly reaching the fault tolerance limit for quantum computation. However, the root cause of the decoherence, and thus its ultimate solution, lies in the insulating materials used in the circuit, primarily the tunnel barrier. Because thermal oxidation is the primary source of defects in the tunnel barrier, it is imperative to find novel methods of ultrathin tunnel barrier fabrication.

Atomic Layer Deposition (ALD) is a promising and unexplored alternative to thermal oxidation for producing tunnel barriers with lower defect densities. Discussed at length in Section 1.4, ALD is chemical vapor growth method that uses self-limited surface reactions to grow films one molecular layer at a time, yielding subnanometer thickness control [38, 41]. Further, these reactions occur at every reaction site on the sample surface, yielding a conformal film with complete surface coverage. The self-limiting and complete nature of the ALD reactions suggests that ALD Al_2O_3 films will have fewer oxygen vacancies and dislocations than thermally oxidized AlO_x, making it a promising technology for producing high quality JJ tunnel barriers. In

addition, while thermal oxidation limits tunnel barrier material selection to AlOx, ALD can be used to grow many interesting tunnel barrier materials, such as MgO which has a small loss tangent and HfO_2 which grows in a polycrystalline phase. These advantages make ALD a prime candidate for fabricating next generation JJ qubits with lower defect densities and higher coherence times.

A key problem in using ALD for tunnel barrier growth is the interfacial layer that develops between the ALD Al_2O_3 film and the Al wetting layer, as discussed in Chapter 3. However, for JJ tunnel barriers, less than 10 ALD cycles are required for a thickness of ~1 nm. In this thickness regime, it is unknown whether AlO_x or ALD-Al_2O_3 dominates the film. Furthermore, at the end of ALD growth the surface is populated with either hydroxyl or methyl groups. The hydrogen in these surface groups may act as TLFs [64] or charge scattering centers [56], which could cause poor coherence in qubit applications or decrease the tunneling current through the JJ, respectively. The key challenges in using ALD for JJ tunnel barriers are then to minimize the thickness of the AlO_x IL and to produce a pristine Al_2O_3 top surface.

There are several possible ways to minimize the thickness of the IL and to clean the top surface of the ALD films, such as ion milling or processing condition optimization. However, we must first understand the influences on JJ performance before designing a solution. A correlation between electrical performance and ALD growth parameters is critical to this understanding. This work approaches the problem by testing the effect of substituting ALD tunnel barrier growth for thermal oxidation in the traditional Nb/Al/AlOx/Nb JJ fabrication process. ALD was performed *in situ* to produce Nb/Al/ALD-AL_2O_3/Nb trilayers, which were then patterned into JJs. The number of ALD cycles performed was varied between 0 and 10, and the current-voltage characteristics (IVCs) of the devices were taken at 300 K and 4.2 K. At both 300 K and 4.2 K the

specific junction resistance ($R_{300K}A$ and R_NA respectively, where A is the JJ area), was found to vary exponentially on the number of ALD cycles performed. Further, the gap current density, J_G, was also found to depend exponentially on ALD cycles. However, despite observing the expected trends in these parameters, the data suggest that an interfacial layer of ~1 nm exists between the Al and ALD-Al_2O_3 layers, which significantly increases R_NA and decreases J_G.

4.3 Experimental Description

Nb/Al/ALD-Al_2O_3/Nb trilayers were fabricated in a homemade deposition system, which integrates UHV sputtering and ALD *in situ* [56, 65]. The Nb films were sputtered onto a water-cooled sample stage at 1.7 nm/s to minimize the formation of NbOx from trace oxygen. The bottom Nb was 150 nm, and the top Nb was 50 nm. The 7 nm Al wetting layers were sputtered at 0.5 nm/s. For trilayers with ALD tunnel barriers, 0 – 10 cycles (0.6 – 1.6 nm) of ALD-Al_2O_3 growth occurred at 200 °C with TMA and H_2O. See 2.2 for a thorough description of the deposition system and process.

The trilayers were patterned into JJ arrays using lithography and etching, as previously described in Section 2.3. Nominal JJ dimensions ranged from 3 – 10 μm. UV Photolithography was used to define the main wiring of the circuit, which includes four electrical leads for each of the 12 JJs on the circuit. The Nb films were etched using reactive ion etching in 15 mTorr SF_6 at 0.4 W/in^2. The Al_2O_3 and Al films were wet etched in 8% H_3PO_4. Electron Beam Lithography was used to define the junction mesa and the top wiring leads. The junctions were insulated by electron beam evaporated SiO_2. The tops of the junctions were cleaned in Ar^+ plasma before the top Nb wiring was sputtered. Also, a bare trilayer with an 8 cycle tunnel barrier was sent to collaborators for JJ processing following an alternate processing recipe [66].

The completed devices were characterized at room temperature and low temperature. At room temperature, current-voltage curves (IVCs) were taken using a semiconductor device analyzer (Agilent B5015A) with 25 μm tungsten probes. The resistance at room temperature (R_{300K}) was extracted from the slope of the IVC. The samples were then cooled to 4.2 K using a homemade probe and liquid helium, described in Section 2.4.2. Current voltage characteristics were obtained to measure R_N and J_G.

4.4 Room Temperature Characterization

R_{300K} was measured at room temperature for samples with 0 – 10 ALD cycles tunnel barriers. **Fig. 4.**1 shows $R_{300K}A$ vs. ALD cycles. Because the contact pads shown in the photomask of Fig. 2.9 were used to make electrical contact, there was a small residual resistance in the 4 point configuration. This resistance was measured by skipping the junction definition phase of JJ processing and, it was found to be 9 - 23 Ω, depending on the location of the JJ on the circuit. For JJs with less than 5 ALD cycles, R_{wire} dominated the measurement as indicated by the flattening of the data for lower cycle numbers. These low resistance data points set an upper limit on the junction resistance for < 5 ALD cycles. R_{300K} is expected to increase exponentially with increasing tunnel barrier thickness [12], so the data were fit to a simple, two-parameter exponential function, as shown in **Fig. 4.1**. Since each ALD cycle is expected to add 0.12 nm to the tunnel barrier, ALD cycles can be used as a proxy for tunnel barrier thickness. However, this does not take into account the formation of an interfacial layer, the thickness of which may increase with an increasing number of ALD cycles. Nevertheless, an exponential trend is apparent. The constant multiplicative factor of 0.30 ± 0.6 kΩ-μm^2 and the exponential factor of 0.41 ± 0.2 will be presently discussed in comparison to low temperature data. This exponential

dependence suggests that the thickness of the tunnel barrier can be controlled by varying the number of ALD cycles performed.

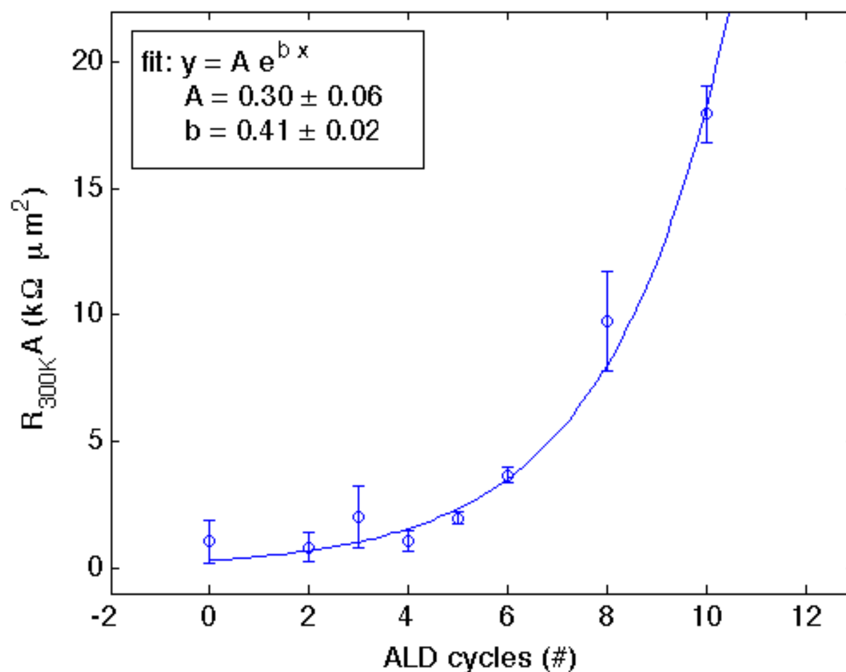


Figure 4.1 $R_{300K}A$ vs ALD cycles with simple two parameter exponential fit.

The exponential trend in $R_{300K}A$ vs ALD cycles indicates that the tunnel barrier thickness is changing between wafers, but it does not yield information about the uniformity of the tunnel barrier on a given wafer. If the tunnel barrier is uniform, $R_{300K}A$ should be independent of A. **Fig. 4.2** shows a plot of $R_{300K}A$ vs. A for JJs with 5-10 ALD cycle tunnel barriers. The slight positive slope attributed to the inclusion of R_{wire} in the measurement, which disporpotionatly affects $R_{300K}A$ for larger JJs. The slight negative slope in the trendline for 6 cycles is due to a small device yield on that wafer. From these data, we conclude that $R_{300K}A$ is independent of the JJ area, indicating a uniform tunnel barrier had been grown. This confirms the conformality of ALD

growth for small cycle numbers (< 10), in agreement with the AFM data for large cycle numbers (> 20) presented in Chapter 3.

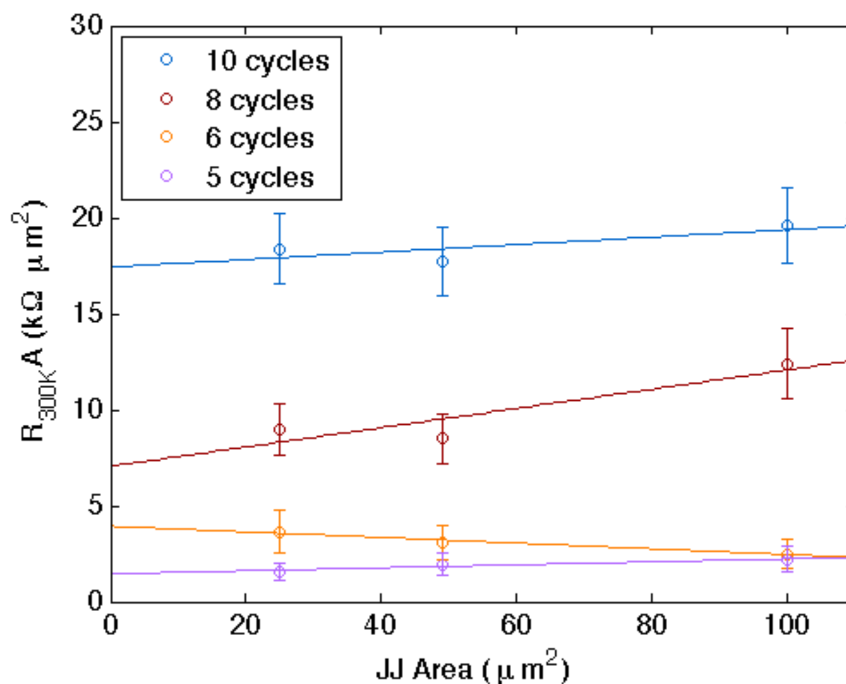


Figure 4.2 Junction specific resistance at 300K ($R_{300K}A$) vs JJ area for JJs with greater than 4 ALD cycle tunnel barriers.

4.5 Low Temperature Characterization

While measurements of resistivity at room temperature provide important information about the quality of ALD Al_2O_3 tunnel barriers, and the results strongly indicate the formation of uniform tunnel barriers, a low temperature measurement of quasi-particle tunneling characteristics is the ultimate test to determine the integrity of the tunnel barrier. IVCs were obtained at 4.2 K for JJs with 2 – 10 ALD cycle tunnel barriers and lateral dimensions ranging from 3 – 10 μm. JJs with 8 ALD cycle barriers were fabricated and measured by collaborators. JJs with 10 ALD cycle barriers were fabricated at KU, but measured by collaborators. From the IVCs, R_N was calculated from the slope of the IVC past the gap voltage $V_G = 2\Delta/e \approx 3$ mV. The

gap current, I_G, was measured at V_G. J_G was calculated by dividing I_G by the nominal JJ area. The measurement system is described in greater detail in Chapter 2.

The IVCs used in this study are presented in **Fig. 4.3 – Fig. 4.7**. **Fig. 4.3** presents the IVC of a standard sample with a thermally oxidized tunnel barrier. Its nominal I_C = 50 µA, and its measured I_C = 40 µA. This reduction of the measured value from the nominal value is attributed to magnetic noise in the measurement system. **Fig. 4.4** presents the IVC of a 5 µm JJ with a 2 ALD cycle tunnel barrier. The measured I_C = 1 mA. The reduced V_G = 2.2 mV is attributed to overheating of the sample caused by biasing it with a large current. **Fig. 4.5** presents the IVCs of 10 µm, 8 µm, and 7 µm JJs with 5 ALD cycle tunnel barriers. **Fig. 4.6** presents the IVCS of 8 µm, 5 µm, 4 µm, and 3 µm JJs with 8 cycle ALD tunnel barriers as measured by collaborators. **Fig. 4.7** presents the IVCs of 10 µm and 7 µm JJs with 10 cycle ALD tunnel barriers. The results of **Fig. 4.4 – 4.5** will be discussed at length presently.

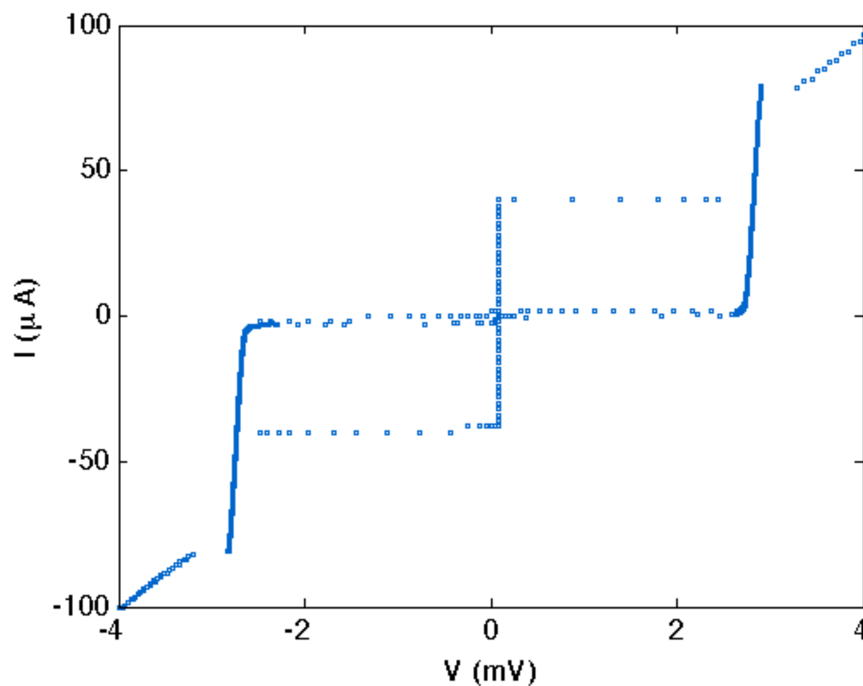


Figure 4.3 Current voltage characteristics of a standard sample with a thermally oxidized tunnel barrier and target I_C = 50 µA as measured by the system used in this study.

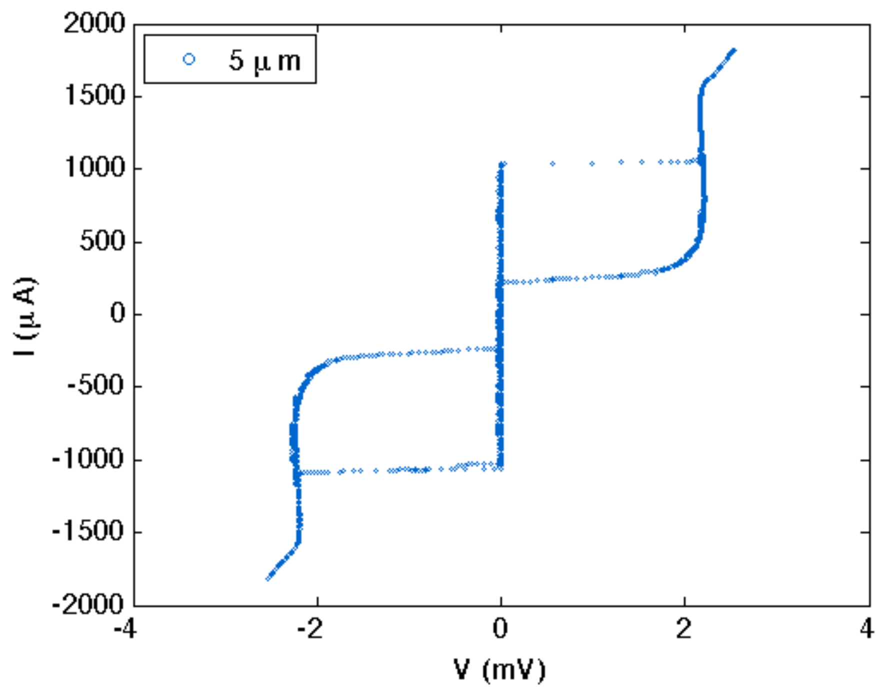


Figure 4.4 IVC of a 5 µm JJ with a 2 ALD cycle tunnel barrier. The reduced gap voltage is due to heating of the sample at high current.

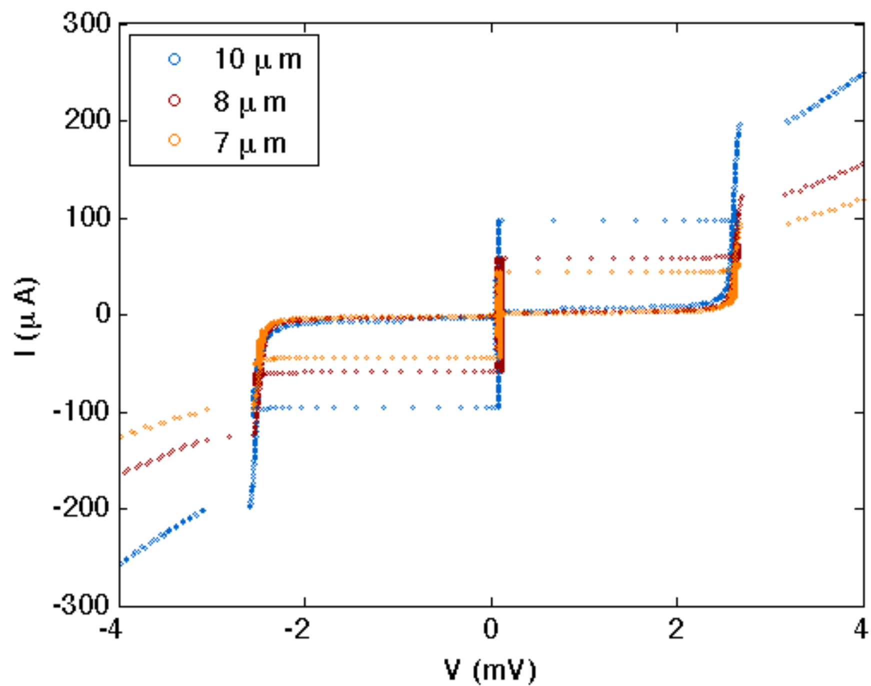


Figure 4.5 IVCs of a 10 µm , 8 µm , and 7 µm JJs with 5 ALD cycle tunnel barriers.

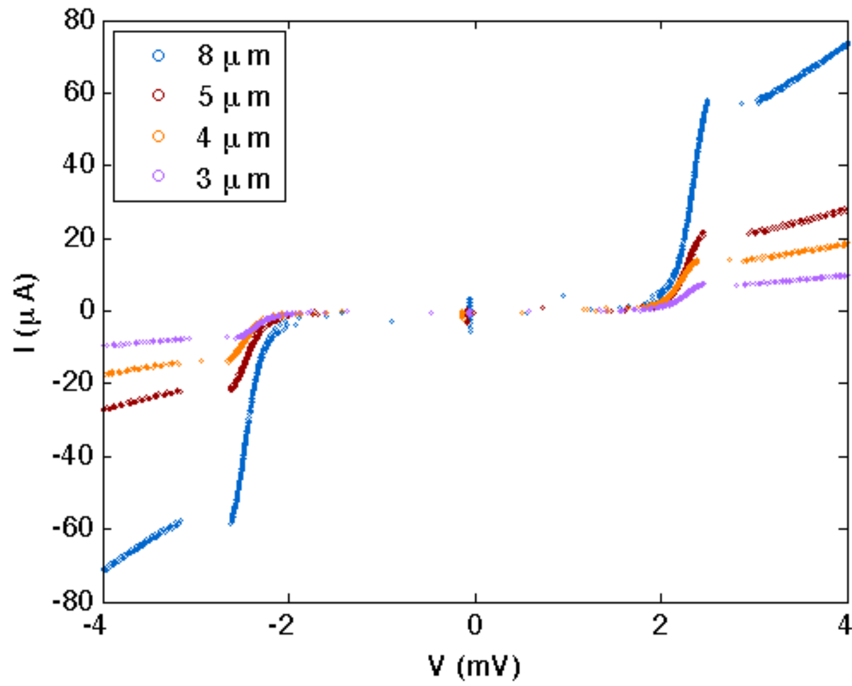


Figure 4.6 IVCs of a 8 µm , 5 µm , 4 µm, and 3 µm JJs with 8 ALD cycle tunnel barriers. The trilayers for these samples were made at KU, but the JJs were processed and measured by collaborators.

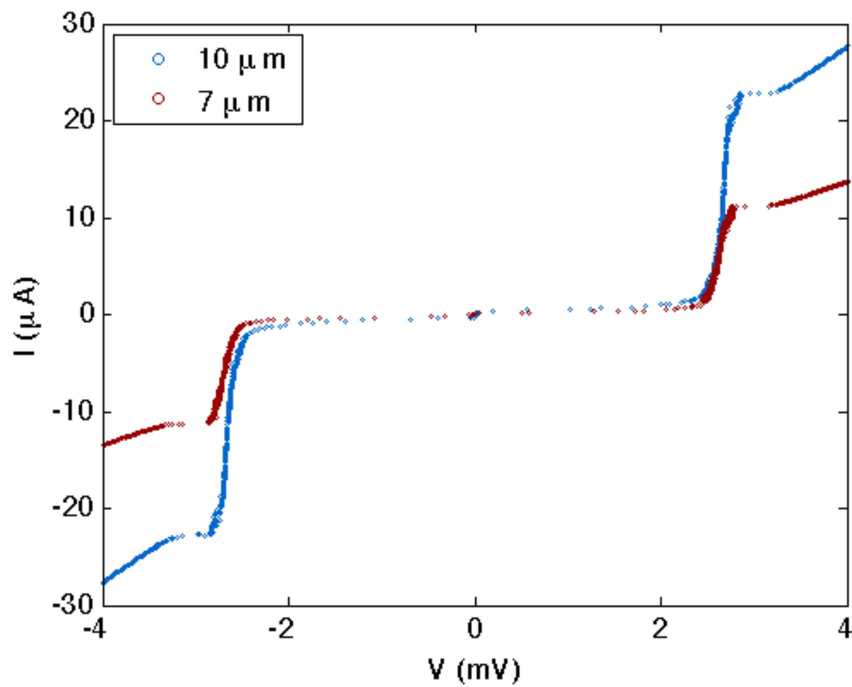


Figure 4.7 IVCs of a 10 µm and 7 µm JJs with 10 ALD cycle tunnel barriers. These JJs were processed at KU, but were measured by collaborators.

The first step to proving ALD tunnel barriers are viable is showing that ALD tunnel barriers produce the expected trends in device parameters. Since there are no previous reports of ALD JJs, it is vital to prove that the tunnel barriers are uniform with respect to size and R_N. One check for tunnel barrier consistency is the product IR_N. According to the Ambegaokar-Baratoff formula (eqn. 1.26), the product I_CR_N is expected to be constant. Likewise, the product IR_N is expected to be independent of tunnel barrier thickness and JJ area. **Fig. 4.8** shows IR_N for all JJs with 5 ALD cycles and sizes ranging from 7 – 10 μm. All of the curves collapse to a single curve. Further, the gap voltage is nearly the ideal value at V_G = 2.7 mV. These data show that ALD tunnel barriers are uniform across the entire wafer.

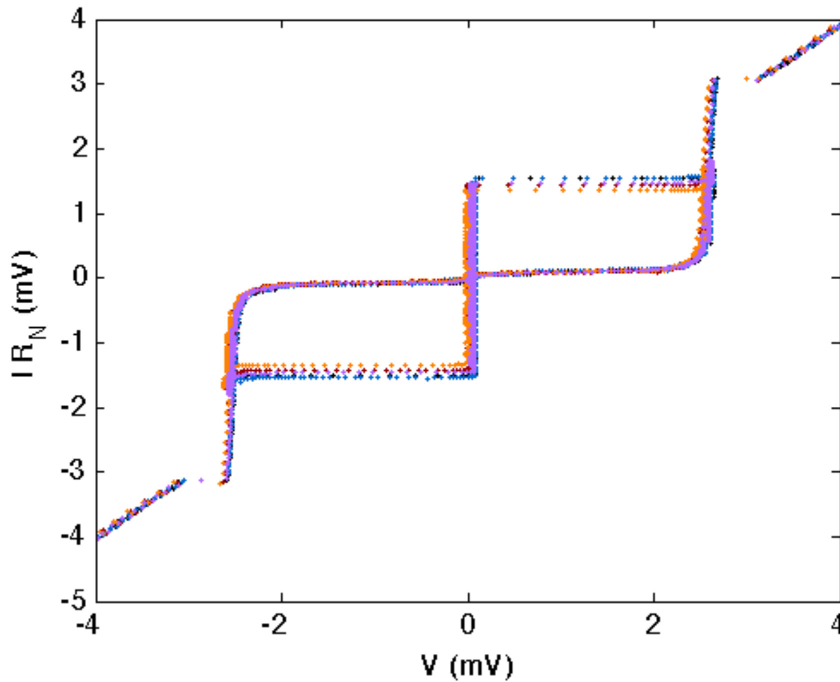


Figure 4.8 IR_N vs V for all 5 cycle JJs in this study.

IVCs for JJs with varying areas are presented in **Fig. 4.5 – Fig. 4.7**. The expected trends of increasing I_C and I_G and decreasing R_N with increasing JJ area are apparent. In particular, I_C, I_G, and A all scale by the same factor when comparing any two of the JJs. For example,

comparing the 7 μm and 10 μm JJs in **Fig. 4.5**, I_C and I_G and A differ by a factor of 2, exactly as expected. For the JJs with 5 cycle tunnel barriers, $I_C R_N$ = 1.5 mV, which is reduced from the ideal $I_C R_N$ = 2.4 mV. However, from the Ambegaokar-Baratoff formula, $I_C = \pi/4\ I_G$ in the ideal case. If this substitution is made when calculating the $I_C R_N$ product for these JJs, we obtain $(\pi/4\ I_G) R_N$ = 2.4 mV. Therefore, the reduced $I_C R_N$ is due entirely to suppression of I_C. This suppression will be discussed presently in the context of variable ALD cycles. Finally, R_{SG} = 330 Ω and R_{SG}/R_N = 17, indicating an acceptably good tunnel barrier has been grown. Together, these data and figures of merit show unequivocally that ALD can be used to grow JJ tunnel barriers.

To establish ALD as a viable method of tunnel barrier growth, it is not enough to show that ALD tunnel barriers are uniform and leak free. For ALD to be successful, it must be proven that controlling the number of ALD cycles controls the JJ device parameters at low temperature, specifically R_N and I_C. **Fig. 4.9** shows $R_N A$ vs. A for JJs with tunnel barriers ranging from 5 – 10 ALD cycles and nominal areas ranging from 9 – 100 μm^2. These data corroborate the similar room temperature data shown in **Fig. 4.2**. Again, $R_N A$ is independent of JJ area, and $R_N A$ increases with increasing ALD cycles. **Fig. 4.10** shows $R_N A$ vs. ALD cycles, similar to **Fig. 4.1**. Again we see an exponential increase in $R_N A$ with increasing ALD cycles, as expected. However, the fitting equations in **Fig. 4.1** and **Fig. 4.10** disagree. In the simple two-parameter fit, the multiplicative pre-factor represents the specific resistance of a junction with a zero ALD cycle tunnel barrier. The precision of this pre-factor is therefore limited by the smallest measureable resistance. In the case of the room temperature measurements (**Fig 4.1**), the pre-factor's precision is limited due to the inclusion of the wire resistance in the measurement, which will artificially increase the measured specific resistance by 225 – 2300 Ω-μm^2, a range which includes the room temperature pre-factor of 300 ± 60 Ω-μm^2. At 4.2 K, we expect this prefactor to be 0, since the

wires become superconducting and no longer contribute to the measured resistance. The resulting value of 30 ± 30 Ω is inline with this prediction. We therefore attribute the disagreement of the pre-factors in **Fig. 4.1** and **Fig. 4.10** to the inclusion of the wire resistance in **Fig. 4.1.** The disagreement in the exponential term will be discussed presently with a comparison to the trend in the gap current. Despite the disagreement in fitting equations, the exponential trend strongly suggests that varying the number of ALD cycles used to grow the tunnel barrier can control the low temperature resistivity of JJs.

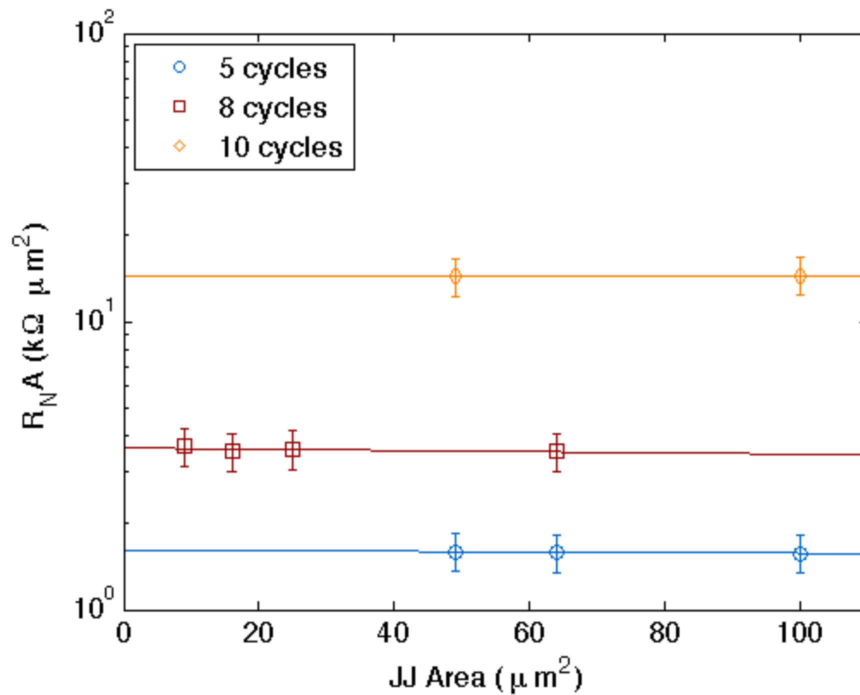


Figure 4.9: R_NA vs A for JJs with ALD tunnel barriers ranging from 5-10 cycles. R_N was measured at 4.2 K.

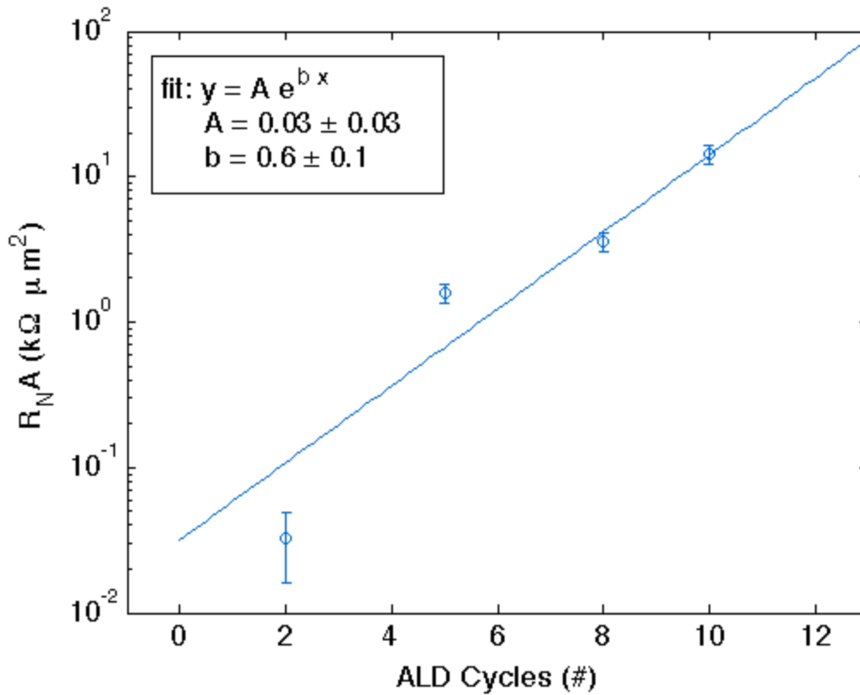


Figure 4.10 R_NA vs ALD cycles calculated from low temperature data.

In addition to showing that ALD JJs have uniform specific resistance at low temperature, the tunneling properties of ALD JJs must be proven. **Fig. 4.11** shows current density vs. voltage for JJs with tunnel barriers ranging from 5 – 10 ALD cycles. The 2 cycle data was omitted because its current density is an order of magnitude larger, and including this data obscured the trend. The spread in the data for JJs with the same number of ALD cycles in the tunnel barrier is due to variation in the JJ area away from nominal values induced by the etching steps of processing. The decreased V_G of the 8 cycle JJs is due to differences in processing; the 8 cycle samples were processed by collaborators and made from trilayers grown a year apart from the rest of the samples. There is a clear trend toward decreasing J_G and increasing specific resistance with increasing ALD cycles, discussed presently. Notably missing are supercurrents for the JJs with 8 cycles and 10 cycles. A very small J_C = 10 A/cm^2 was measured on the 8 cycle JJs while no supercurrent was observed on the 10 cycle JJs. All samples' supercurrents deviate from the

expected $J_C/J_G = \pi/4$ by varying degrees. In fact, the ratio of J_C/J_G decreases with increasing ALD cycles. We have previously hypothesized earlier [56] that this reduction in J_C is due to charged scattering centers resulting from the ALD growth process (e.g. lingering OH* groups on the ALD film surface). However, this hypothesis was made when only the 8 cycle data (**Fig 4.6**) was available. With this expanded dataset, it is far more likely that electromagnetic noise in the measurements is entirely responsible for supercurrent suppression. When a standard sample with a thermal tunnel barrier was measured in the same system (**Fig. 4.3**), $J_C/J_G = 0.5$, confirming that supercurrent suppression independent of ALD growth was occurring during measurement. Further, the decreasing trend in J_C/J_G can be well explained by a constant current noise level in the measurement system, which will suppress I_C by an approximately constant amount and disproportionately affect junctions with lower I_C. However, these data are not conclusive, and a more systematic study with tight control of magnetic fields and lower noise levels is required to draw a firm conclusions.

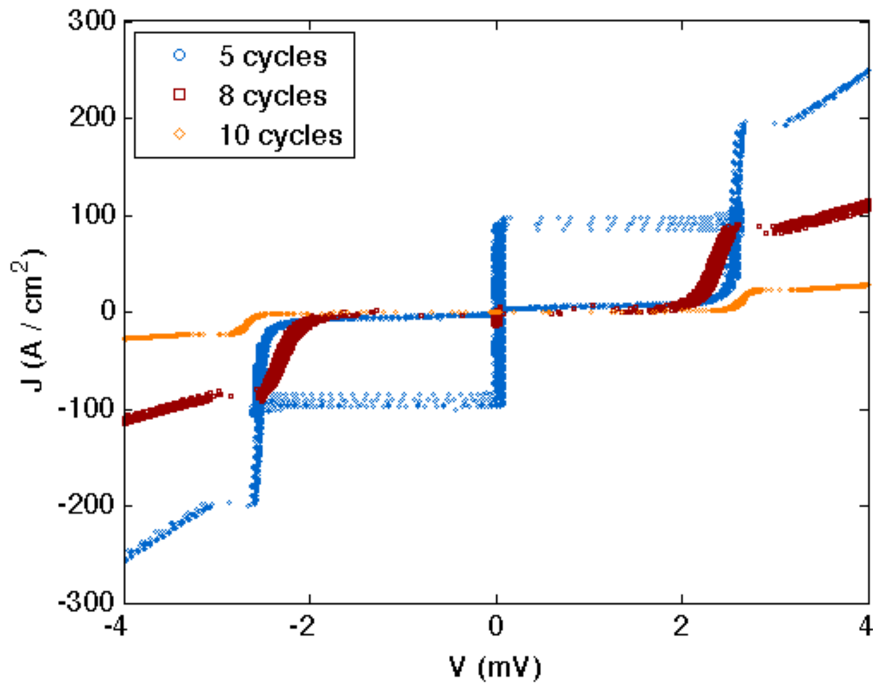


Figure 4.11 Current density vs. voltage for all JJs measured at low temperature. The 2 cycle data was omitted for scaling.

Since the maximum value of J_C could not be measured reliably, J_G will be used as a proxy to compare the tunneling properties of these JJs since J_G and J_C are theoretically proportional. In **Fig. 4.11** there is a clear trend of decreasing J_G with increasing ALD cycles. J_G vs. ALD cycles is shown in **Fig. 4.12a**, and the data are fit to a simple exponential function. Notably, the exponent of this fit (0.5 ± 0.2) agrees with the exponent of the fit in **Fig. 4.7** (0.6 ± 0.1) within their respective uncertainties, despite being calculated from separate data sets. This exponent is related to the decay length inside the tunnel barrier, as shown in eqns. 1.17 and 1.25, which is a material parameter related to the energetic barrier height of the tunnel barrier material. Even though the exponential factor from the low temperature datasets agree, both of them disagree with the exponent from **Fig. 4.1** (0.41 ± .02). We attribute this discrepancy again to the inclusion of the wire resistance in the room temperature measurements. The data in **Fig. 4.**1 level off for < 4 ALD cycles, which obscures the exponential trend in that region, biasing the fit

toward a more slowly growing model. Notably however, the exponents in **Fig. 4.7** and **Fig. 4.12a** are near a previously reported value of 0.42 correlating low temperature J_C measurements with the thickness of thermally oxidized tunnel barriers measured by TEM [67], shown in **Fig. 4.12b**. However, both of the values in **Fig. 4.7** and **Fig 12a** are greater than 20% higher than the literature value. There are three possible explanations for this discrepancy. The first possibility is that the dataset presented in this work is too small to run thorough statistics, and the fitting parameters are biased from the small sample size. The second possibility is that using ALD cycles as a proxy for tunnel barrier thickness is inaccurate because of the development of an IL during ALD growth. Finally, the third possibility is that ALD Al_2O_3 films grow more densely (i.e. have a higher barrier height) than thermally oxidized AlO_x films. A more thorough study beyond this proof of concept is necessary to distinguish the possibilities. Nevertheless, the exponential decrease in J_G and the agreement of the exponential dependence of J_G and R_NA lead to the conclusion that the tunneling properties of JJs can indeed be controlled by altering the number of ALD cycles used to grow the tunnel barrier.

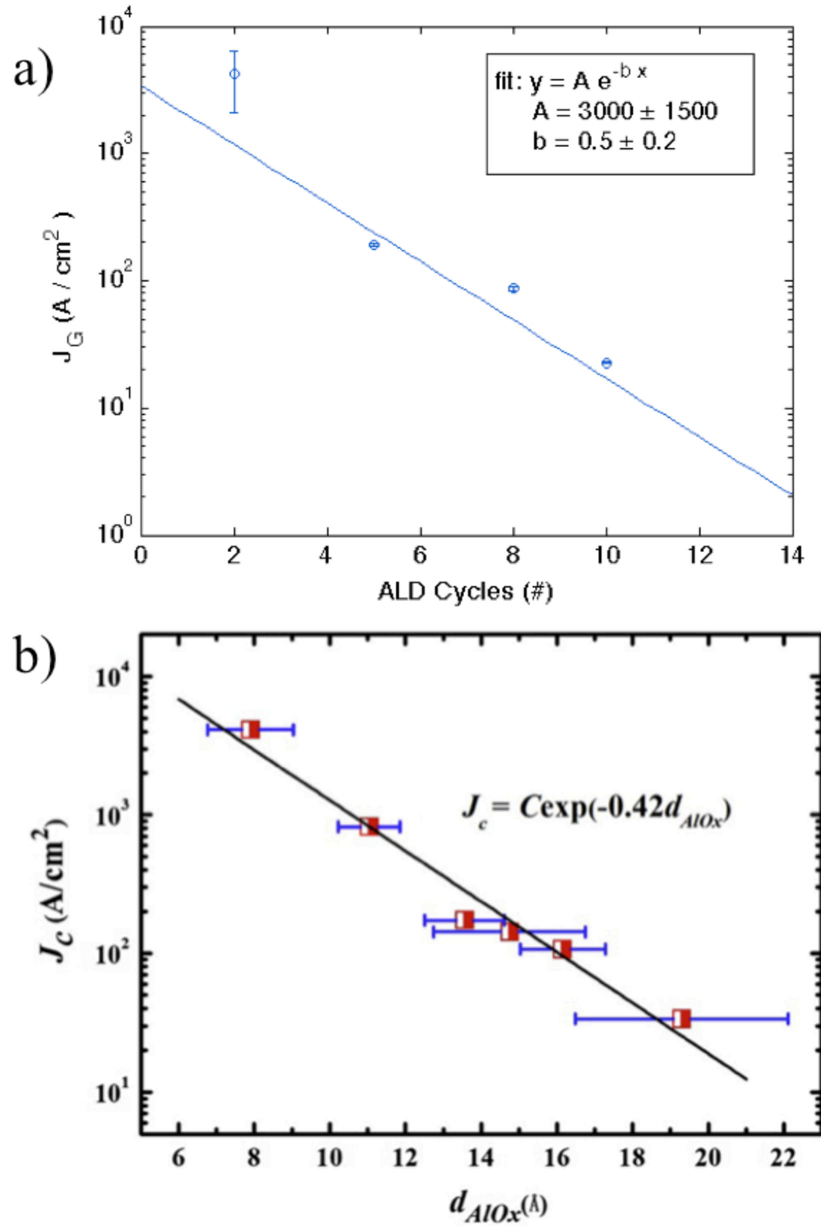


Figure 4.12 J_G vs ALD cycles measured at low temperature (a) and Jc vs. tunnel barrier thickness from Reference [67] (b).

By extrapolating the fit in **Fig. 4.12a** to 0 ALD cycles, some indication about the thickness of the interfacial layer between the ALD Al_2O_3 film and the Al wetting layer can be seen. At 0 ALD cycles, the fit predicts a J_G ~ 3000 A/cm^2, or J_C ~ 2400 A/cm^2 (0.024 mA/µm^2). This is current corresponds to an oxidation dose of ~10^4 Pa-sec [29] and a tunnel barrier thickness of ~0.8 nm [67]. For convenience, the relevant figures from References [29] and [67]

are given in **Fig. 1.4** and **Fig. 4.12b**, respectively. Though this conclusion is an extrapolation of a fit from a small dataset and its accuracy is suspect, it can be corroborated by the low current densities measured. For example, 5 cycles of ALD should grow only 0.6 nm, which corresponds to a J_C = 6000 A/cm^2 [67]. However, from the data in **Fig. 4.11** and **Fig. 4.12a**, a JJ with a 5 ALD cycle tunnel barrier is expected to have a maximum J_C ~ 150 - 300 A/cm^2, which corresponds to a tunnel barrier of ~ 1.4 nm. We can then estimate that the thicknesses of the ALD-Al_2O_3 layer and the AlOx interfacial layer as 0.6 nm and 0.8 nm, respectively, which agrees reasonably with the estimate of the interfacial layer thickness from the extrapolation. Estimated values of the interfacial layer thickness for all tunnel barriers with 2-10 ALD cycles are presented in **Table 4.1**. The average value of the estimated interfacial layer thickness is 0.74 nm, and the average value for tunnel barriers with 5 – 10 ALD cycles is 0.83 nm. Beyond the reduction in J_C, this interfacial layer is problematic for qubit applications because it must be a thermal oxide, which is suspected to have a large density of TLFs compared to the ALD film. In order to realize the full potential of ALD tunnel barriers, the formation of this interfacial layer must be frustrated, for example by using one of the strategies outlined in Section 3.4. But despite this interfacial layer, it is clear that ALD can be used to grow Josephson tunnel barriers with variable thickness.

Table 4.1 Measured gap current density (J_G), calculated critical current density (J_C), estimated tunnel barrier thickness ($d_{barrier}$), estimated ALD layer thickness (d_{ALD}) and estimated interfacial layer thickness (d_{AlOx}) with respect to ALD cycles.

ALD Cycles	J_G (A/cm^2)	J_C (A/cm^2)	$d_{barrier}$ (nm)	d_{ALD} (nm)	d_{AlOx} (nm)
2	30000	24000	0.75	0.24	0.51
5	2000	1500	1.40	0.60	0.80
8	80	60	1.70	0.96	0.74
10	20	16	2.10	1.20	0.9

4.6 Conclusion

In conclusion, JJs with nominal areas between 9 – 100 μm^2 were fabricated with ALD tunnel barriers ranging from 0 – 10 cycles. Room temperature and low temperature measurements of the specific resistance confirm the tunnel barrier thickness was controlled by varying the number of ALD cycles, and the expected exponential increase in resistivity with increasing tunnel barrier thickness was observed. Further, measurements of the current density showed the gap current density decreased exponentially with increasing ALD cycles. The exponential dependencies were found to agree within 15%. However, despite seeing the expected trends, clear evidence of an interfacial layer of ~0.8 nm was observed. This interfacial layer must be removed if ALD JJs are to become practical for qubit applications. However, it is clear that ALD can be used to control the resistivity and tunneling properties of Josephson junctions.

5 Conclusion

Since the 1970's, silicon technology has increased processing power by many orders of magnitude by increasing the density of silicon transistors according to Moore's Law. However, silicon transistor feature sizes are approaching a fundamental minimum size limit, and a new paradigm in computer technology is required to tackle problems that are intractable to classical computers. Quantum computing is a promising paradigm that relies on the superposition of macroscopic quantum objects, called qubits, to perform parallel calculations. Josephson junction (JJ) based qubits are compatible with modern semiconductor processing, so they are a very promising technology for the implementation of qubits. They are superconductor-insulator-superconductor (SIS) trilayer structures with an insulating tunnel barrier of only ~ 1 nm, allowing Cooper pairs to tunnel through according to the Josephson equations. JJs are a mature technology that have been used for SQUID magnetometers and voltage standards since the 1970s. However, JJ qubits have suffered from short coherence times, making reliable computation an issue. A major source of decoherence in JJ qubits is two-level fluctuators (TLFs) in the insulative materials of the JJ circuit, particularly the tunnel barrier. Traditionally, the tunnel barrier has been grown by thermally oxidizing aluminum, which produces an inhomogeneous distribution of defect sites, such as oxygen vacancies and interstitials. These defect sites act as TLFs, which give rise to decoherence. In order to realize the full potential of JJ qubits, an alternative method of tunnel barrier growth is required.

A promising alternative to thermal oxidation for tunnel barrier formation is atomic layer deposition (ALD), a chemical vapor growth method that uses self-limited surface reactions to grow conformal films one molecular layer at a time. ALD is suspected to produce fewer point defects than thermal oxidation when growing aluminum oxide due to the self-limited and

complete nature of the chemical equations governing ALD. However, to grow ALD films on metallic substrates, such as the superconducting electrodes used in JJs, the metallic substrates must be protected from atmospheric exposure prior to the ALD growth process. To that end, we have built a thin film deposition tool, which integrates ultra-high vacuum magnetron sputtering with ALD *in situ*, allowing the growth of multilayer sputtered and ALD films without atmospheric exposure. This tool was used to grow ALD Al_2O_3 on sputtered Al, SiO_2, and Si substrates. The ALD Al_2O_3 film was measured with *ex situ* ellipsometry to measure the growth rate of the film on the various substrates. Though the average growth rate was found to be equal on all substrates for ALD films of 2 – 10 nm, evidence for a 2 nm interfacial layer was found on Al substrates. By varying the thickness of the Al layer on Si substrates, it was confirmed that this interfacial layer was formed by the thermal oxidation of Al, and that only 0.15 nm of Al is sufficient to initiate ALD Al_2O_3 nucleation.

As a proof of concept that could be easily compared to the standard Nb/Al/AlOx/Nb JJ process technology, Nb/Al/ALD-Al_2O_3/Nb SIS trilayers fabricated and processed into JJs using advanced lithography and etching techniques. The JJs' current-voltage characteristics were then taken at 300 K and 4.2 K. By varying the ALD-Al_2O_3 thickness, trends between the tunnel barrier thickness and the resistivity of the JJs were observed. In particular, the specific normal state resistance (R_NA) and the gap current density (J_G) were found to be exponential functions of the number of ALD cycles performed, as predicted by theory. However, the critical current densities were lower than would be expected in the absence of an interfacial layer. By comparing the data to literature correlating JJ current density to tunnel barrier thickness, evidence for a thermally oxidized interfacial layer of ~ 0.8 nm was found.

The interfacial layer between the Al wetting layer and the ALD film is the key problem going forward with ALD tunnel barriers for JJs. This interfacial layer is caused by the thermal oxidation of the Al wetting layer during the H_2O pulses during ALD growth. There are at least two strategies to solve this problem. The first is to reduce the thickness of the Al wetting layer; however, this introduces the possibility of oxidizing the underlying Nb electrode which would be catastrophic. A second strategy is to frustrate the formation of thermal oxides on by inserting an oxygen diffusion barrier between the Nb base electrode and an ultrathin Al wetting layer. A diffusion barrier composed of a noble metal such as Pd or Ag would prevent the formation of NbO_x. Since ALD films are known to nucleate poorly on noble metals, an ultrathin (~1 Å) Al layer on top of the diffusion barrier could act as a seed layer for nucleation and limit the AlO_x thickness to ~1 Å. This would make ALD Al_2O_3 the dominant film in the tunnel barrier after only 2 ALD cycles (2.4 Å). Future work should optimize strategies to reduce the interfacial layer thickness and more thoroughly characterize ALD JJs at low temperature.

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