Fabrication of Semiconductors by Wet Chemical Etch

Selective Etching of GaAs Over InGaP in Dilute H_2SO_4:H_2O_2

Fabrication engineering of semiconductor devices has made possible optoelectronic instruments, laser diodes and wireless communication devices among many other modern devices. Beginning with Bardeen, Brittain and Shockley's invention of the transistor in Bell Labs in 1947 and Kilby and Noyce's introduction of the integrated circuit about a decade later, semiconductor devices have dramatically advanced the computing and electronics industries.

Semiconducting materials, such as silicon, germanium, gallium arsenide, and indium phosphide, are neither good insulators nor good conductors, but they have intrinsic electrical properties so that by controlled addition of impurities, their conductivity can be altered. With the need to manufacture devices at the micro- and nanoscale, the semiconductor industry has followed "Moore's Law," the trend that the number of transistors placed on an integrated circuit increases exponentially about every two years. Production of the tiny features to create these integrated circuits is achieved by plasma etching of semiconductor material. The plasma etch process is carried out in a chamber in which a gas mixture is partially ionized to create a plasma, or glow discharge. High energy ions in the plasma bombard the semiconductor material and chemically reactive components in the gas mixture form etch products with the semiconductor. The process produces accurately etched features and is one of the primary reasons for the reduction in device size that has made technology such as cell phones and laptop computers possible.

INTRODUCTION

Semiconductors such as InGaP and InGaAsSb are important for light-emitting devices as well as communications devices and electronics. Fabrication of these devices is achieved by plasma etching in which an ionized gas mixture etches the substrate by both chemical reaction and physical bombardment. In plasma etching for these purposes, indium products are not as volatile and are usually more difficult to remove than other semiconductor materials. For this experiment, only wafers with an existing

LAURA FRANCOVIGLIA is a senior in chemical engineering at the University of Kansas.

epitaxial GaAs cap layer grown over an underlying InGaP layer were available. For the development of an Inductively Coupled Plasma (ICP) etch process for the InGaP layer, the top GaAs layer must first be etched off to expose the underlying InGaP layer. A common technique used to do this isnvolves a selective wet chemical etch that will remove the GaAs layer without etching or damaging the InGaP layer.[1] Determining the selectivity and etch rate for removing the GaAs layer are the primary goals of chemical wet etch development. Once this has been accomplished, a "recipe" for removing the epitaxial GaAs layer can be created.

Chemical wet etching selectively removes the cap layer of the wafer through a series of chemical reactions in a liquid solution. For this etch process, H2SO4:H2O2:deionized water, a common solution for removing GaAs, was used in the proportions of 1:8:640. The reaction occurs in a sequence of steps involving an oxidation reaction of the hydroxide ions when the semiconductor is immersed in an electrolyte system to produce Ga2O3 and As2O3. These oxides dissolve in the acid of the etchant solution and form soluble salts.[2]

Wafer samples with a 750Å cap layer of GaAs on top, middle layer of InGaP and thick base layer of GaAs were used. The layer structure of these wafers is shown below. Later etching will use InGaAsSb wafers. However, because indium is the most difficult layer to etch, InGaP is a good starting point.

Epi Layer Structures of V3338

350 Å GaAs	5E18 Si Doping (Top)
400 Å GaAs	1E17 Si Doping
160 Å InGaP	not intentionly doped (i)
Delta Si Doping	4.4E12/cm2
30 Å AlGaAs	not intentionally doped (i)
130 Å InGaAs	not intentionally doped (i)
30 Å AlGaAs	not intentionally doped (i)
Delta Si Doping	1.1E12/cm2
Superlattice Buffer	
GaAs Buffer	
S.I. GaAs Substrate	

Epi Layer Structures of V3339

350 Å GaAs	5E18 Si Doping (Top)
400 Å GaAs	1E17 Si Doping
130 Å InGaP	not intentionally doped (i)
Delta Si Doping	4.4E12/cm2
30 Å AlGaAs	not intentionally doped (i)
130 Å InGaAs	not intentionally doped (i)
30 Å AlGaAs	not intentionally doped (i)
Delta Si Doping	1.1E12/cm2
Superlattice Buffer	
GaAs Buffer	
S.I. GaAs Substrate	

EXPERIMENTAL

Using a 1:8:640 chemical wet etch solution of H2SO4:H2O2:deionized water, an etch rate of 10 Å/s was expected to remove the 750Å GaAs epitaxial layer and an etch rate of ~ 0 Å/s was expected in the InGaP layer. These results would be indicative of good selectivity.

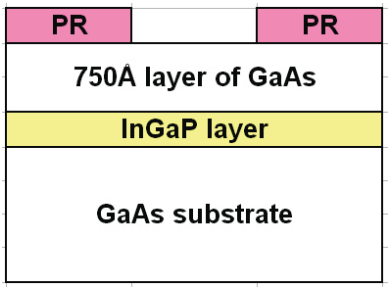


Fig. 1 is a simplified representation of the layers of the wafer. On top of the wafer is photoresist. The gap in between the photoresist has been developed in such way that the wafer is ready for chemical wet etching in that region.

Before etching the wafers, a pattern must first be imprinted on the wafer surface so that a contrast can be seen between the etched and non-etched areas. Photolithography, a process similar to film exposure, was used to imprint the pattern by using a mask to create an image on the wafers in a light-sensitive, protective layer of polymer material called photoresist. The photoresist used was Microposit S1818. The wafers were exposed using a mask aligner, which is a UV exposure system, and were tested under various exposure times until well defined features were seen on the wafer surfaces. An adequate exposure time was 75 seconds for the mask aligner used. (Light intensity can be controlled to help determine proper exposure time, but for this experiment the intensity potentiometer was not available, therefore a trial-and-error method had to be used.) After exposure, the wafers were developed in a NaOH-based solution.

The following is a description of the photolithography and development procedure:

- Cleave wafer into 1 cm x 1 cm samples using tweezers and scribe
- Clean using isopropanol, acetone and again isopropanol in a bath on a hotplate at 90°C for 5 minutes each
- Blow dry with nitrogen
- Coat samples with photoresist using spinner at 3700 rpm for 30 seconds
- Soft bake samples on hotplate for 1 minute at 115°C
- Expose samples under mask aligner for 75 seconds
- Post bake samples on hotplate for 1 minute at 115°C
- Develop samples by agitating in NaOH-based developer for 1 minute
- Rinse wafers in deionized water for 30 seconds
- Blow dry with nitrogen
- Use microscope to look for high definition of features patterned onto samples

The developed wafers were measured with a profilometer (Dektak II) to get a baseline, pre-etch, topographical profile of the photoresist for each sample. In taking this measurement, it was possible to determine the feature depth prior to etching. It was suspected that the etch solution would attack the photoresist as well as the wafer. The baseline measurement was a preparatory step to establish the initial thickness of photoresist. The wafers were then dipped into a 1:30 solution of NH4OH:deionized water and agitated for about 45 seconds, rinsed in deionized water and blown dry with nitrogen in order to remove native oxide.

The exposed wafers were then cleaved into two or three pieces, so that more data would be available for analysis. The etch solution of 1:8:640 of H2SO4:H2O2:deionized water was prepared under the hood in manageable proportions of 0.2:1.6:128 mL. Samples were individually immersed in the etch solution and gently agitated. Three etch times were used: 35, 75 and 110 seconds. The lower and upper ranges from the expected etch time of 75 seconds were used to help verify the etch rate and selectivity. After etching, the wafers were measured again using the profilometer to compare to the pre-etch results and estimate etch depth.

RESULTS AND DISCUSSION

Results were inconclusive after the first round of the etch process. It appeared that the wet etch solution did not selectively etch the wafers. It was hypothesized that the wafers could have been upside down, meaning that the thicker, bottom layer of GaAs was being etched instead of the 750Å top layer. In the second round of the etch process, care was taken to mark the bottom sides of each sample using a scribe. A control wafer was also used in the second round, which was purposefully flipped bottom side

up for etching. In the second round, a sample from each wafer type was also used.

Because the etch solution attacked the photoresist, which can be seen in the negative etch rates in Fig. 3 and in etch depths greater than 750Å in Fig. 4, the wafers had to be stripped of the PR to measure accurate etch depths. This was done by agitating the wafers in acetone for 2 minutes, rinsing with methanol for 2 minutes, and blow drying the wafers with nitrogen. The process was repeated until all of the photoresist was removed. The wafers were then measured again with the profilometer to determine the actual etch rate and depth. Reproducible etch rates were achieved as shown in Fig. 3. The etch rate for samples stripped of PR averaged 8.37Å/s with a standard deviation of 0.92Å/s, which was near the expected etch rate of 10Å/s.

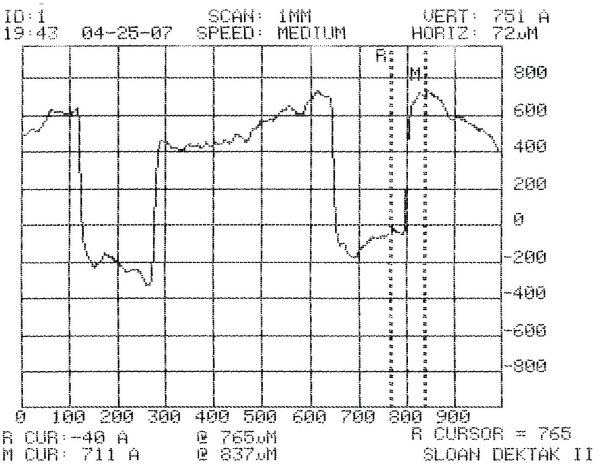


Fig. 2 is an example of the results from the profilometer, which gives a cross-sectional view of the wafer. This sample was in the etchant for 110 seconds and was stripped of photoresist. The results show that this particular sample was etched to a depth of 751Å. Because measurements were taken in angstroms (1 x 10-10 m), some experimental error is to be expected using the instruments available. There may also be slight variations in the thickness of the grown layers.

The second round of the etch process showed that the 750Å GaAs layer was selectively etched in the H2SO4: H2O2:deionized water solution with an average etch rate of 8.6 Å/s after regression analysis to find the best fit for the data. The results also concluded that the wet etch stopped at the InGaP layer since an etch time greater than that required to remove the GaAs layer still resulted in the same etch depth. In Fig. 4 the etch selectivity is demonstrated in the measurement without photoresist where the curve levels off. At this point, all of the GaAs layer was etched away leaving the underlying InGaP layer was exposed.

Fig. 3

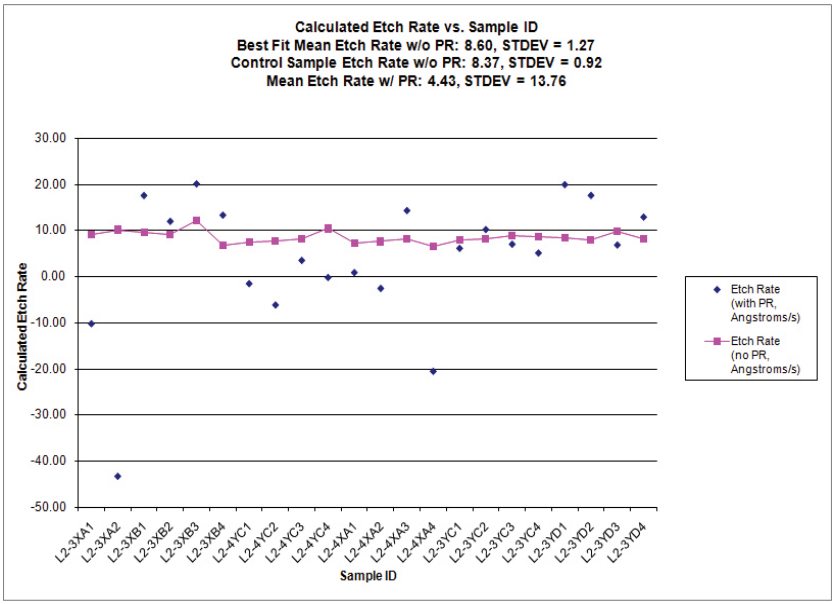
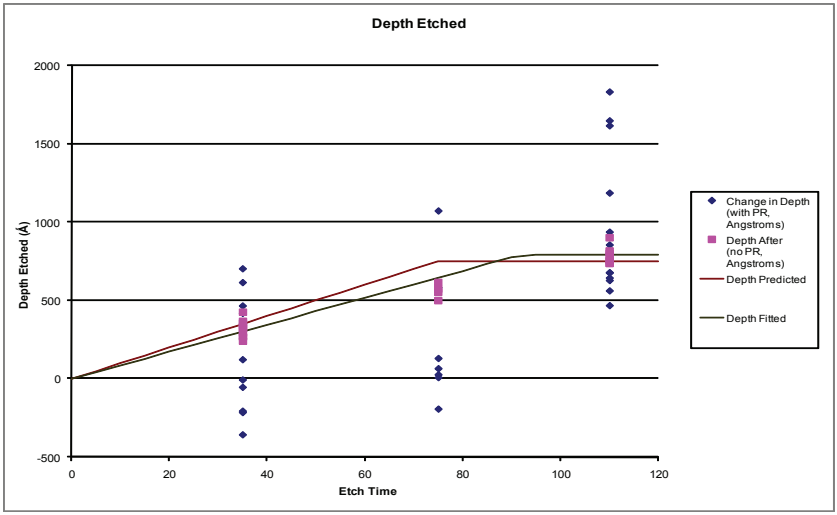

Calculated Etch Rate vs. Sample ID
Best Fit Mean Etch Rate w/o PR: 8.60, STDEV = 1.27
Control Sample Etch Rate w/o PR: 8.37, STDEV = 0.92
Mean Etch Rate w/ PR: 4.43, STDEV = 13.76
Calculated Etch Rate
30.00
20.00
10.00
0.00
-10.00
-20.00
-30.00
-40.00
-50.00
L2-3XA1
L2-3XA2
L2-3XB1
L2-3XB2
L2-3XB3
L2-3XB4
L2-4YC1
L2-4YC2
L2-4YC3
L2-4YC4
L2-4XA1
L2-4XA2
L2-4XA3
L2-4XA4
L2-3YC1
L2-3YC2
L2-3YC3
L2-3YC4
L2-3YD1
L2-3YD2
L2-3YD3
L2-3YD4
Sample ID
Etch Rate (with PR, Angstroms/s)
Etch Rate (no PR, Angstroms/s)

Fig. 4


Depth Etched
Depth Etched (Å)
2000
1500
1000
500
0
-500
0
20
40
60
80
100
120
Etch Time
Change in Depth (with PR, Angstroms)
Depth After (no PR, Angstroms)
Depth Predicted
Depth Fitted

CONCLUSIONS AND FUTURE WORK

A selective wet etch process to remove GaAs epitaxial cap layers from underlying InGaP layers has been developed using a solution of H2SO4: H2O2:deionized water at a rate of ~8.6 Å/s. In future work, this etch will be used to prepare wafers for the most difficult layer to plasma etch, InGaP, which can be etched by Reactive Ion Etching (RIE) in an Inductively Coupled Plasma (ICP). Finally, the study of InGaP plasma etch rates will lead the way for study of InGaAsSb etch rates, an important semiconductor used in applications such as mid-infrared laser diodes.

ACKNOWLEDGEMENTS

This research was made possible with the guidance of Dr. Karen Nordheden, the advising professor. Bogdan Pathak, graduate student advisor, provided limitless patience and support in training and data analysis, and Mike Santilli, postdoctoral research advisor, also provided expertise and training support in the photolithography process. Gratitude is also due to Dr. Ming-Yih Kao of TriQuint Semiconductor who provided the chemical wet etch recipe and to the University of Kansas Chemical and Petroleum Engineering Undergraduate Research Program.

END NOTES

1. Campbell, Stephen A. The Science and Engineering of Microelectronic Fabrication. New York: Oxford University Press, 2001.

2. Ghandhi, Sorab K. VLSI Fabrication Principles: Silicon and Gallium Arsenide. New York: John Wiley & Sons, Inc, 1994.