Engineering Management Field Project

Title- Auto Defect Classification (ADC) value for patterned wafer inspection systems in PLY within a high volume wafer manufacturing fabrication facility.

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Glossary of Terms

Application Specific Integrated Circuit (ASIC): Logic device that is used in electronics.

Auto Defect Classification (ADC): Method by which to you optical recognition comparison to identify or classify defect into a know type.

Blocked etch: Defect that will often short one or more lines together.

Bright Field Inspection: Inspection that normally uses bright light illumination and detection is in line to the illumination so the image background is "Bright".

Chip: A single device on a wafer is called a chip. This individual device would eventually be used in the production of a memory or processor device or other ASIC.

Dark Field Inspection: Inspection that has off angle collection so the background is dark. If a defect is detected it will scatter (light or laser) to the detector.

Defect of Interest (DOI): Defect that has high probability to cause chip (or circuit) failure.

Design of Experiments (DOE): Set of experiments with ultimate goal to reduce wafer cycle time or improve yield.

Design Rule: This is the minimum width of a printed line.

DRAM: Dynamic Random Access Memory is commonly used in all computers & gaming devices.

Etch Tool: Etch tools will "Take away" material on the wafer.

Fab: wafer manufacturing fabrication facility

Falling Lines: Lines that fall over after the etch process due to poor adhesion and chemistry below the line

Full Stack Micro Masking: Defect that occurs early in the etch process that has blocked the etch so the left over material goes down to the bottom of the trench.

Litho: Unit process area responsible for Photolithography area in fab.

Nuisance Defect: Defect that gets picks up by inspector but it does not have any or very little yield impact

Patch (image): Inspection Computer image that is used to help learn an ADC classifier.

Preventative Maintenance (PM): scheduled PM or unscheduled PM's.

Process Limited Yield (PLY): Variability or problems in process that is limiting the yield.

Quality Control (QC)

Scanning Electron Microscope (SEM): Equipment that uses electrons to hit the surface of a material and the detection is of electrons that are imaged

Statistical Process Control (SPC): Used to help monitor trends and keep the process in control

Technical Learning Vehicle (TLV): High running product layer at the leading design rule, there were is the high fill of product.

Tungsten: Metal that is often used to make interconnections between silicon and other metals.

Unit Process (UP): Group that is responsible for a specific area of manufacturing process.

Wafer: Semiconductors are manufactured and built up on a thin polished silicon device

Water Spots: Residual spots on wafer that are round and low contrast. At the Wet bench etch areas this is one of the defects of interest.

Wet Bench: Etch tool or cleaning tool that uses liquid chemistry to remove material.

Yield: % of good chips / overall chips produced or manufactured.

Introduction:

To reduce circuit chip failures in the Semiconductor Industry, getting accurate optical classification of defect source will assist in giving early indication of a potential issue that would reduce manufacturing yield. The Quality Control Defect Inspection Tool will report information of x,y location, size and other feature information but this data has limited usefulness if it does not tie directly to a classification. A critical part of the inspection is to translate the inspection defect information into a classification code. Auto Defect Classification (ADC) is the means to classify optical or laser based detection images to assist in solving the source of the failure (Brecher, 1996). ADC systems are now fully integrated into the inspection tools and utilize a virtual thumbprint created from representative examples of a classification code to classify each defect shortly after it was detected (Chou, 1997). All defects that are captured by the inspection scan will be classified once ADC is trained on example images of each class code (Peiponen, 2009).

Executive Summary: Hypothesis of key conclusions

The purpose of this investigation is to demonstrate value for Auto Defect Classification (ADC) for patterned wafer inspection systems within a high volume manufacturing fabrication in the Process Limited Yield (PLY) defect area. Process excursions in all functional Unit Process (UP) areas, examples are of etch, litho, diffusion, are monitored by PLY.

Troubleshooting of process excursions using added defect density count with a small percentage (random or largest 50 examples) of and inline Scanning Electron Microscope (SEM) data classification review does not give a clear indication of the full

wafer data. Statistical Process Control (SPC) trigging on total counts or defect density is not as powerful as making excursion decisions on classified data from ADC (Fisher, 2002).

The ADC data gives classification of the entire wafer rather than a smaller sample making signature analysis to be an additional troubleshooting tool. The inline ADC data does not have near the resolution of the SEM but can be used to help make important decisions to what is occurring in the manufacturing line. The interest is to gain a full understanding of the current capabilities and limitation of ADC and to apply the learning to enable faster reaction and visibility into process and tool excursions within a high volume manufacturing fabrication.

The Technical Learning Vehicle (TLV), high running product layer at the leading design rule, there were approximately 10,000 wafers a week with 1000 wafer die (chips) per wafer. A sustained improvement in yield of 1% across the entire manufacturing line would equate to almost 1 million dollars a month of saving. With the ability to tightly control multiple etch process tools, the resulting yield improvement was 3% across 15% of the line. With the baseline yield improvement along with ability to react quickly to process excursions, the combined improvement resulted in excessive of 5 million dollar a year of reoccurring savings.

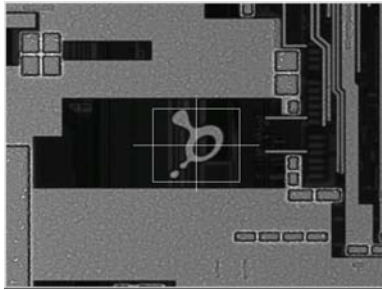

Fig 1 (Example Image of Chip)

Industry Overview

Semiconductor device manufacturing industry is a global industry creating integrated circuits for all types of electronics devices. There are three major segments of devices, Memory, Logic & ASIC (application specific integrated circuits). A majority of the industry begins with a silicon wafer and repeats a process of depositing multiple layers of material on the wafer topped with a photo sensitive top layer. Using photo-lithography to expose the wafer, exposed areas will be vulnerable or hardened to the chemical etching process. After the etch process, the remaining material (i.e. metal, di-electric etc.) will make interconnection in the circuits. After repetitive process of adding layer and etching will result in a multi-layer stack that is the semiconductor device (Shapiro, 1997). In figure 1 above is an example of metal lines on the right side of the chip that would result after the wet etch of the metal.

Most semiconductor fabrication facilities have well over one hundred process steps. Inspection steps are placed through the fabrication process of the wafer to help partition and protect the line from yield loss. For a mature process about 5-10% of the wafers will be inspected. The goal is to inspect the same wafers throughout all the inspection steps to enable proper subtraction of prior level defects.

The entire manufacturing process from bare virgin silicon just prior to final test will take just under two months. Given the nature of supply demand and oversupply of some of the devices, the industry is under constant pressure to reduce costs. In the making of semiconductor devices, process excursions may cause defects on the chip resulting in a failure that is unable to be repaired, negatively impacting yield.

The Semiconductor Manufacturing Industry is continually under cost performance pressures of improving existing yield, (Good chip/ total chip produced or manufactured). Current Optical and laser scanners will identify defect x, y location and difference intensity but understanding true yield impact a specific defect is data that is not understood until final test (Peters, 2002). Waiting until final test to understand the root cause of a failure is far too long to make process decisions to improve yield resulting in maximizing company profits. As an added feature to most Semiconductor Inspection Scanners, one can use defect examples to build an Auto Defect Classification (ADC) training set. This ADC training set is then applied to all additional scans.

The maximum opportunity for ADC to improve profits and yield through quicker reaction to process excursion is $10M per year with the assumption that ADC will allow for a one day reaction time on a total of 15 excursions a year.

Figure 2: - Yield Improvement with Excursion Detection example. Financial charts highlighting opportunity for baseline yield improvement of $10.8M yearly.

Assumptions	Without ADC	**If React within 1day to excursion**	
Dram Chip value (ASP for 1Gb DRAM in 2008)	$1.50	$1.50	
Dram Chips per wafer	1,000	1,000	
production line per week	10,000	10,000	
Production days From Gate Contact to Final Test	4 weeks	4 weeks	
Excursions	1 Excursion	1 Excursion	**Potential saving**
chips manufactured (per day)	1,428,571	1,428,571	
Line Impact (multiple products run)	15%	15%	
% wafer in product that will be impacted	25%	25%	
Ave. days in excursion	**10**	**1**	
Chip loss	535,714	53,571	
$ lost Dram	$803,571	$80,357	$723,214
Normally dealing with 2 excursion every 3 weeks, (35 excursions per year)			
Total yearly Excursion saving opportunity (est. 15 max. per year ADC could assist with			$10,848,214

For yield loss in GC module assume 10 days normally to react to excursions, as often within two weeks excursions will go away even if root cause is unknown as preventative maintenance (PM's) are normally schedule every two weeks on process tools. Excursion with 15% yield loss impact 25% of wafers..., Yield loss would be 10000 wafers per week x 1000 chips per wafer x .15 (yield loss) x 4 weeks if caught at test. But, assuming reasonable PM cycle on tools, most excursions only last for about 2 weeks until fixed by PM for a good approximation of opportunity, the calculations above is of 10 days of an excursion situation. This would calculate a loss of $800K for one excursion of duration of 10 days. If ADC were to enable a one day reaction time to an excursion with estimation of 15 excursion a year the saving would be about $10M.

The bigger and more lasting impact is making subtle yield improvements. Sustained baseline yield improved with goals toward continuous process improvement through the manufacturing product line has a lasting impact. Utilizing ADC to drive yield improvement process by an overall reduction of defect of interest (DOI) that kills the chips is the goal. Issue is controlling the process on total added counts if most all the defects have zero kill rates and no impact on yield. An improvement on 5 additional yielding die on each wafer is profound. If you can control the 5 die per wafer you are looking at 10000 (wafers per week) x 5 die x $1.5 per die x 52 weeks in a year.

Literary Research

An investigation into optical and laser based inspection it is clear that numerous industries utilize both optical and/or laser based machine vision inspection for quality control of the product that is manufactured. Industries from automotive to food processing and packaging utilize machine vision to make quality control "go" or "no-go" decisions (Anderson, 2010; Fernando, 2010). To control the manufacturing quality of automatic manufacturing of bolts, state of the art optical machine vision tools analyze the machine threads to automate quality control decisions that previously required manual inspection of an operator (Perng, 2010).

In the semiconductor industry, given the numerous outside influences of defect causes and how some defects have a much higher likelihood to impact yield where as other defects are nuisance, having a good way to automate the classification is critical. There are numerous approved patents in the semiconductor field that have new art on the way defects are accurately classified utilizing optically and laser based inspection scanners. More recently, a patent has been filed on the utilization of the multiple images of a SEM to help with ADC.

In the semiconductor industry, ADC was initially introduced to take away the offline classification variability that operators would do at offline review station. Defect x-y location is initially detected by the inspection tool. Offline ADC replaced the inaccuracies between operator classifications and proved to be very beneficial. Issue arose of setup time and redetection of the detected defects. Options for online "revisit" ADC was also used in the inspection scanners. An ADC CCD camera inside the

inspection station and a certain percentage of defects were revisited and classified after the detection of the defect. This revisit of the defect inside the Inspection Station and impacted the overall wafer throughput of inspection equipment.

In the final stages of ADC deployment, a position the industry is in now, the Semiconductor Industry utilizes the numerous features that are captured during the inspection to do the auto defect classification on the scanner captured image (called patch image). Given there is no additional overhead time to revisit the defects, inline or "on-the fly" ADC is most popular now. The creating of ADC recipe or "classifier" is done offline so not to impact uptime of the inspection stations.

Many investigations are of in-line revisit ADC as "on-the fly" ADC is the most recent release. Looking and papers that are produced, one needs to read into to analysis to understand if the ADC is a "revisit" in the chamber or the current "on-the-fly" and processing the ADC class code while the wafer is scanning.

Investigated equipment supplier websites to find numerous ADC research and presentations that were done at various industry trade conferences and engineering meeting (Steckenrider, 2009) i.e. SEMICON West, various Yield Meetings. There is an interesting investigation published at IBM on "Automatic Defect classification for Semiconductor Manufacturing" whereas evaluation of ADC was complete in 1997. This publication was of the improvement of a system that had a sample of the defect that would be revisited with another camera and redetected and classified. A more recent publication of integrating ADC into a High Volume manufacturing facility with the "one the fly" version of ADC did not surface in a literature review in various other industries.

This improvement to ADC has the ability to classify 100% of the defects detected is what this paper is focused on.

Individual successes in ADC are reported and the focus of this paper will be to deal with the introduction challenges of ADC into a high volume manufacturing facility.

Challenge

Wafer inspection tools, Bright field or Dark field, are very good at reporting the x,y location of defect. The issue is that it is difficult to understand what the root cause of the defect is with just defect location. The use of On-line real-time ADC with reliability and confidence in the data is key in having data that module owner will trust.

Given a past failed rollout of ADC at the headquarters, gaining initial support and focused resources was a challenge from the start. Gaining initial management support and setting proper expectations for success and setting the resources in place helped to ensure success. The initial issue with the acceptance of ADC as a viable reliable product a Memory Fab was there was perceived notion that ADC would not work in a high volume manufacturing environment given previous issues. This notion was due to earlier unsuccessful evaluation at the headquarters facility. The other issue is that the "ADC" name has been used for a while and is not trade marked, so any earlier rollout issues or failures of the earliest version of offline ADC helped to resonate with the most experienced users that may had issue with offline ADC or online "revisit" ADC. In digging into the issue, it was clear proper expectation of accuracy and purity of the ADC classification was not properly set.

As the project team leader for ADC in the validation phase, weekly team meeting were run and monthly status updated to senior management were created to ensure forward momentum in the schedule. By selecting team members that were enthusiastic and some that did not have previous experience with the ADC product, there was an openness to investigate and pursue the benefits of automatic defect classification. Monthly group discussions with the development facility were created to get the development facility involved in the project success and pass on lessons learned to the three sister facilities. Additionally responsibility included PLY (process limited yield) engineer responsible for 300mm Bright Field wafer inspection. The ADC project scope included both bright field and dark field inspection systems. Time to dedicate to ADC specific related activities was approximately 30%.

Project Outline

- Validation of Tools in 300mm fabrication
- Test plan
- BKM's (best know methods)
- Implementation to production.
- Develop monitoring plan to ensure ADC classification scheme remains stable
- Collection of use cases where ADC help improve reaction time and increase yield.
- Propagate Lessons learned to three Sister fabrication.

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Goals of Yield Enhancement

Ensure quick reaction to process or tool excursions that negatively impact yield. Reaction to a defect issue might consist of immediately to shut down a process tool or to help pinpoint which of the improvements in a specific design of experiment has the most profound yield impact. The reporting of overall total defect counts is limited in its effectiveness as all defects are not created equally. Reported defect size is helpful but information pertaining to aspect ratio (scratch like) or polarity (bright or dark) information will give much more value than just an x/y defect location. This brings about the true usefulness of ADC.

With all of the defects on the wafers having classification information from ADC, spatial information like scratches or a heavy clustering of a specific defect code in the center would often give clear indication of the potential defect sources. For example a high concentration at a specific edge of the wafer may indicate a specific handling robot or chamber door has contamination issues where as a center bull's eye of specific defects may indicate a spray nozzle that has issues of not atomizing the material on to the wafers. Having the classification of 100% detected by the inspection by ADC, spatial information and more importantly, used in conjunction with SPC, triggers can be set to help in the shutdown of very specific process tool to protect yield loss in the line.

Depending on the size of the defect, very often if a defect is picked early on the process, this defect will often be picked up multiple times through the process. The focus with inspection points is to get the scanner to pickup current layer defect given that with the sampling process and capacity issues, it is possible for a layer to be overloaded with adder defects.

One of the major challenges with prior level subtraction is that even with best intentions of having inspection inspections steps in place earlier in the process, when issue of capacity arises, earlier process inspection steps have high potential of being skipped out. In situations where missed prior inspections occur, previous layer defect will be considered as adders and may trigger false SPC on total adders alone. By controlling on a good current layer defect code, missed inspection steps should have less an impact on the data enabling better control. ADC can help to bin out and classify defect that are the defect of interest (DOI) and help as a nuisance filter to defect that are not of interest or have minimal known yield impact.

Accurate defect classification will give a much better indication to yield impact. ADC is a tool, when properly used will help to give a cleaner signal to the DOI. With a clean DOI signal, design of experiments (DOE's) are created to test improvements in the process to reduced or eliminate a critical yield limited DOI.

ADC can improve the abilities of "defectivity" analysis through providing the ability to react to a specific defect that is a yield detractor, by tracking and removing a cosmetic defect allowing for the true detracting defects to be measured and by providing volume data in a sampling scenario allowing for quicker analysis of process and tool changes. The analysis below of the ADC codes includes evaluations of specific defects, classification accuracy and purity, DOI signal improvement and "defectivity" improvements made. Specifically the ADC codes were applied to 3 types of defects commonly attributed to yield detractors or noise in the defectivity signal. These defects included Full stack micro-masking , Fallen lines and Water spots.

Result 1 -> Clean Signal-> Blocked Etch

Figure 3: Defect Density class code 20 vs Etch Chamber. Chamber D had higher average defect counts which triggered early chamber cleans.

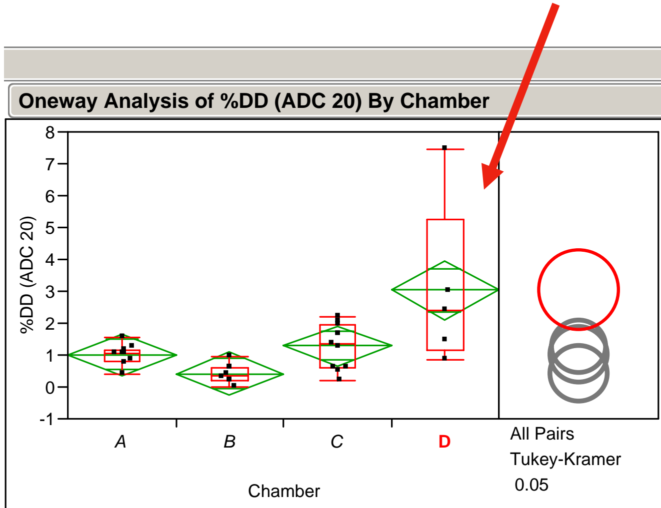
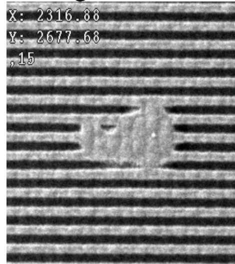


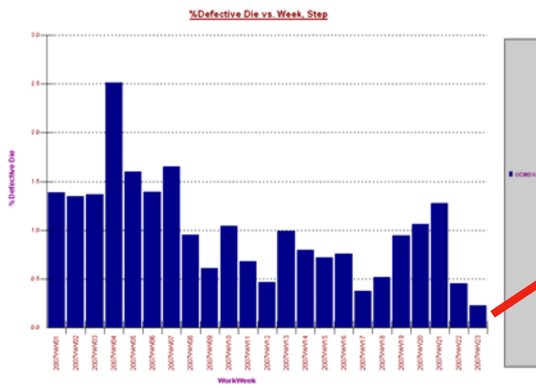
Figure 4: SEM image of Class 20 blocked etch. This defect results from contamination flaking off the chamber walls during the etch process.

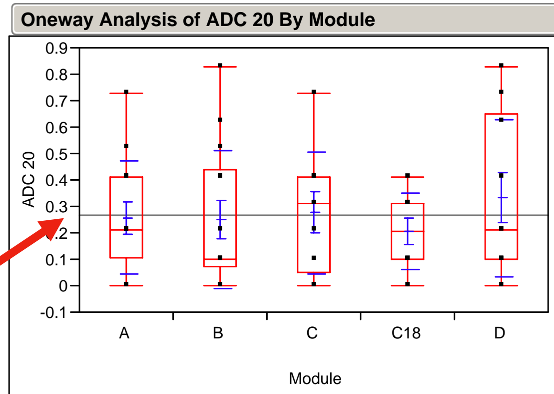


The chart (Fig 3) is a normalized defect density % on classcode 20. Along the "X" axis there are four chambers of an individual tool that is being monitored. This is a commonly know defect source that is caused by flaking off of the chamber. In this case it was clear that chamber "D" had higher than normal defect counts on the specific code 20. Getting a very clean signal to blocked etch gave the data required to justify replacing the liners at 400 RF running hours.

A good representation of ADC classcode 20 is in Figure 4. This ADC classcode 20 is best described as a blocked etch / full stack micromasking or full stack bridging. The root cause of this type of defect occurring is when a flake falls off the metal deposition chamber wall. In the patterning lithography where area are exposed to be etch, the etch wall particle flake with prevent the etching process to be successful. Given that this defect causing shorting to four of more lines, it is not able to be able to be repaired through redundancy. This defect will cause result in a defective die adversely impacting chip yield.

Figure 5: Defect Dies vs. work week Figure 6: Chambers A-D of ADC20
Monitoring chambers ADC 20 helped to find the root cause of an excursion.

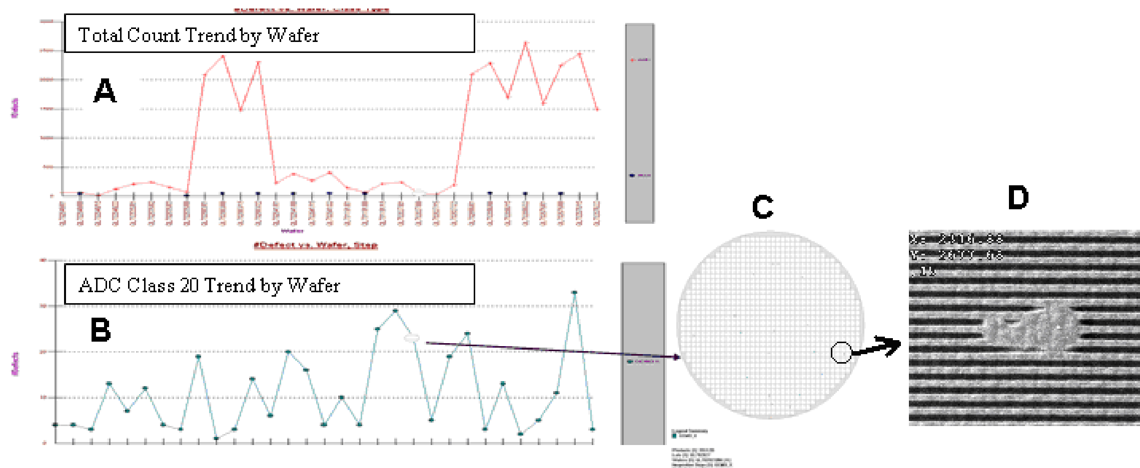




Close monitoring of defect classcode 20 helped reduce occurrences of full stack bridging and enabled valuable design of experiments between etch chambers and justify upgrade to different material for chamber liner.

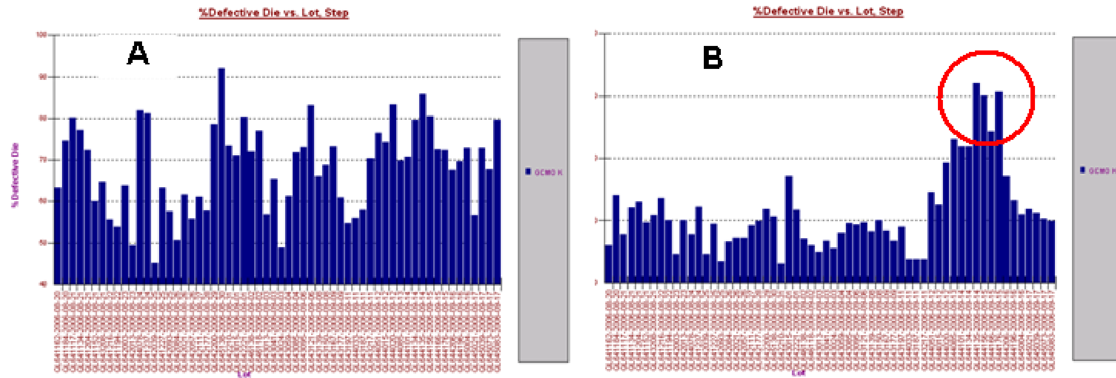
Result 1–Cont.

Figure 7:
A-> Total Count Trend by Wafer
B-> Class code 20 vs. Wafer Class Type,
C-> wafer map
D-> defect
Comparing the top chart of all defects to lower chart of ADC class coded 20 there is a clear signal to high yield impacting defect of blocked etch.



The two charts (fig 7) above is across the same data set and trending by classcode #20 above and the chart below it is of total counts. Classcode #20 has the best signal to noise to the defect of interest to monitor the health of the etch tool of blocked etch. The ADC classcode 20 chart is giving above is it clear that the classification by ADC code 20 is giving indication of tool issues that are missed by chart that displays defect totals.

Figure 8:
A-> All Defects Right – Class code 20 only
B-> ADC Code 20, red circle denotes clear excursion that was missed when displaying all defects.



In the above Figure 8, the left side graph is all defect codes is all defect and the right graph image is of classcode 20 only. In Figure 8 on the right side it can been seen that the count totals for class code 20 detects an excursion that would be missed on the same data set monitor only total counts. It is clear that that when ADC is setup to monitor a killer defect type is possible to possible to find excursions that would be previously missed.

Result 1–Cont.

Automated Charts -> Moving Median

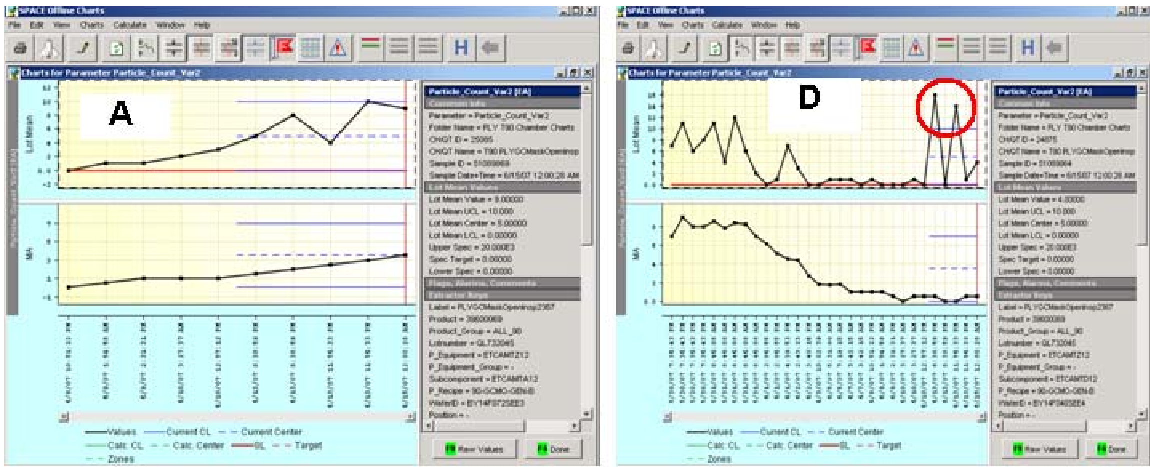
Moving Median Statistical Process Control (SPC) charts of ADC 20 have been created for each GCMO chamber to assist in deciding when to shutdown the chamber when is it out of control. There are two possible problems that occur, systematic or non-systematic. Systematic issues are time or wafer based failure events. An example is where a Preventative Maintenance event of a cleaning or replacement of expendable part is required. One of the root causes of blocked etch is when the liners on the etch chamber degrade causing the flaking off a defect on to the wafers. In a situation to

optimize production keeping the line running decisions to delay preventative maintenance events (PM's) to balance yield and cost of materials and down-time arise often to meet delivery schedule for critical customers. Using moving medians on class code 20 was successfully to gain clarity into systematic and non-systematic issues of flakes falling on the wafer. An example of a non-systematic issue is not time or event based failure. A good example is of falling lines which will be discussed in the next example in detail where as the underlying chemistry fails causing the line to weaken and fall over.

In the two charts below come off the same etch process tool that has four processing chambers. Both images have a top and bottom part of the chart. The top section is raw count of ADC code 20 and the bottom is a moving median of last seven wafers. The left side image of Figure 7 below is of a clean signal of chamber A that identifies a slow increase in moving median count that looks to be a systematic increase and does have one point failing raw count trigger limit.

The right image of Figure 9 below shows chamber D a dramatic downward trend on the raw counts at the start and what looks to be a non-systematic issue at the end of the chart where there are two out of control spikes in raw counts and the moving median has yet to have the last two out of control limits raw count limits impact the lower moving median count total.

Figure 9:
A-> Chamber A D-> Right Chamber D
imaged-> Graph shows how moving medians will highlight out of control situations.



Utilizing moving medians and continuing to drive defectively down on a know killer defect, full stack micro masking, beyond having better reaction to excursions, the baseline defectivity reduced over time.

Result 2 -> Clean Signal -> Falling Lines

An example of a critical defect of interest at metal inspections are bridging where two lines are shorted together. In this case, the bridging is called falling lines. Falling lines is best described as an issue with process chemistry where as the line stack falls over. With a wafer map of total defects, an individual would miss the pattern of falling lines which can give an indication of a specific process tool to be the issue.

Figure 10:
Four separate examples of falling lines
The images of falling lines below will result in a short of two lines.
(optical images below)

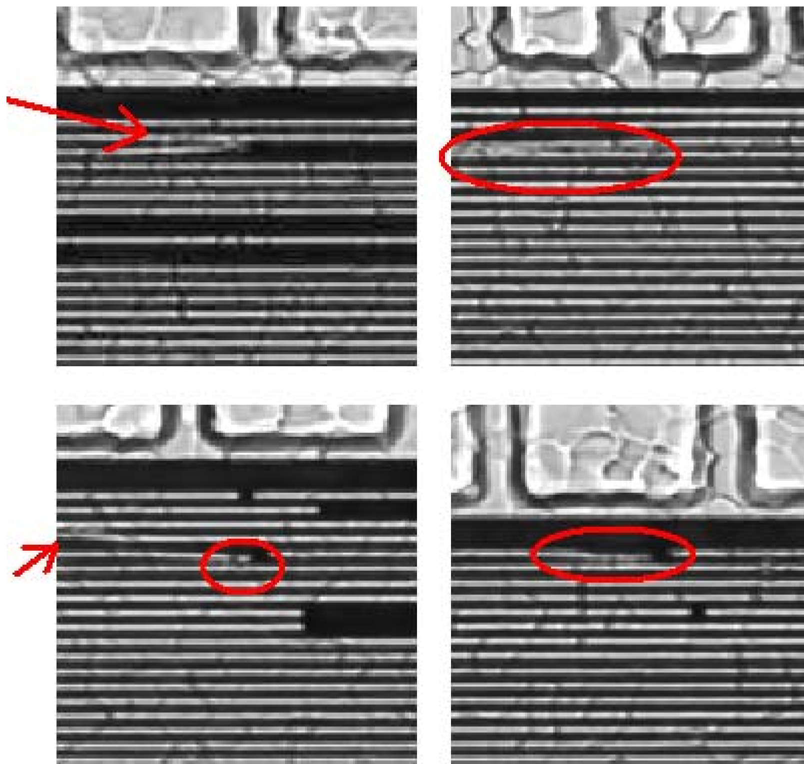
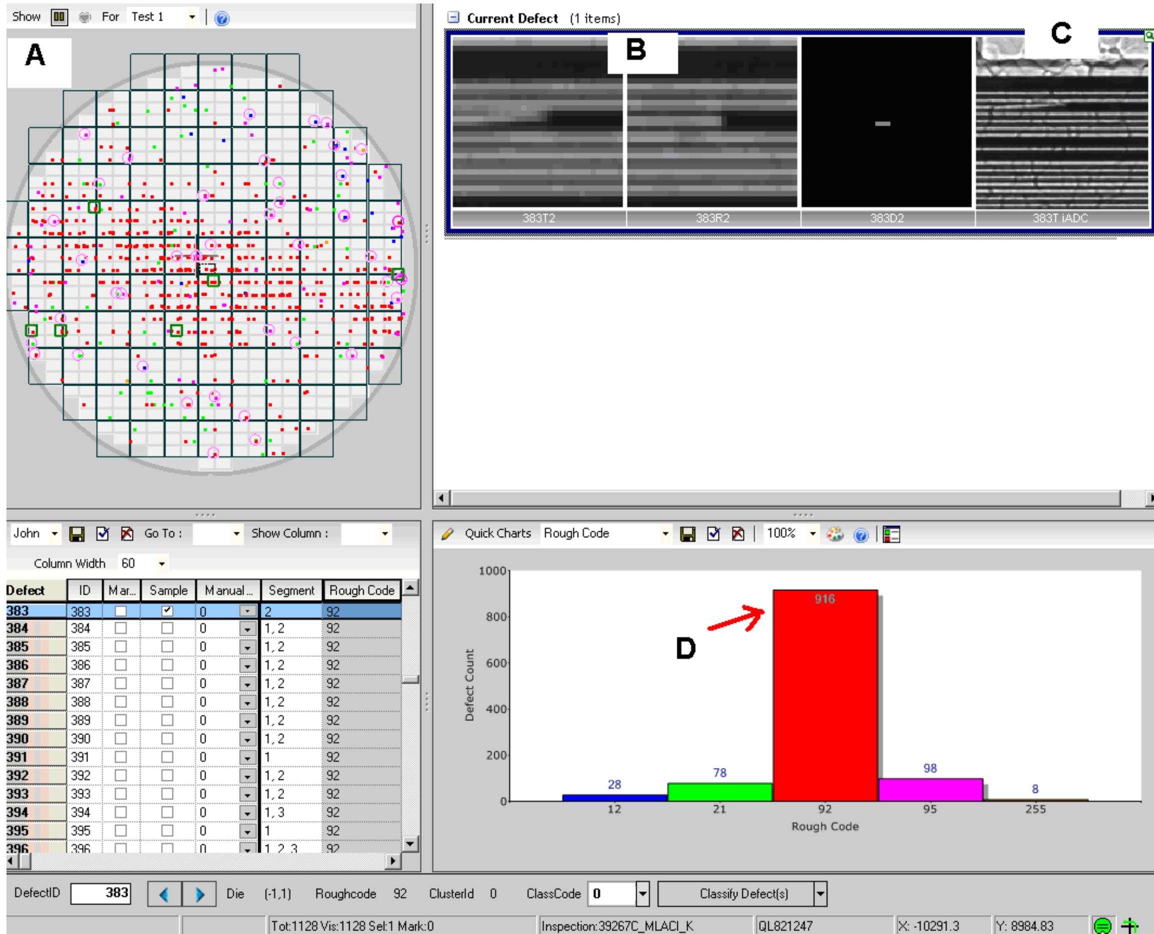


Figure 11:
A-> Wafer Map- Red on Wafer map shows spatial signature going across wafer from 3 to 9 o’clock position.
Pictures- (B) inline scanner images (C) revisit optical images
Bar graph- (D) Red bar on chart shows high levels of fallen lines classsocde 92 .



Above in figure 11 there is wafer map (A) and inspector scanner patch images (B) and an optical scanner (C) revisit image. Additionally in figure 11, there is a Bar graph of the different class codes (D). It is obvious from the graph that fallen lines is the most prevalent peak of class code 92 (D) are the predominant defect and it can also be noted on the wafer map in (A) that there is additional spatial signature information of the falling lines start at the 9:30 position and move diagonally across to about the 3:30 position.

This additional spatial signature information can be used to help troubleshoot hardware and process issues to improve yield (Gleason, 1997). With the uniqueness of process tool in the way they load wafers and apply material or remove material to the wafer surface, a signature of a specific class code will give additional information to the troubleshooting to the defect and aid in the pursuit to the root cause to mitigate the problem for occurring again.

The strong signature of falling lines was achieved without the requirement of pre-scans. In the example the falling lines defect is current level a very large concern when it come to end of the line yield. The falling line will cause shorts resulting in bad chip resulting in reduced yield. In this example ADC code 92, falling lines had a good ability to properly classify the “falling lines”; previous inspections were not required to get a good signal to the DOI that had a very high impact to yield.

Result 3 -> Clean Signal -> Water Spots

In previous examples of falling lines and micromasking, ADC was used to assist with product wafer scans to peruse baseline reduction of defects and improve reaction time to excursions. ADC was investigated to show the added value as a tool monitor. Test wafers are commonly used to check the health of a process tools after a preventative maintenance event and as a time based check to make sure that tool are functioning properly. The ability to quickly bring up a process tool after an excursion event without jeopardizing production wafers is a primary goal.

The structures on test wafers are not active chips that would be sold. These structures on the chip were created to monitor the cleaning tool commonly called a “Wet

Bench" used to remove resist layer after the etch tools completed the etch process. The goal of ADC classifier creation was to remove prior layer defect and to classify water spots only. Previous layer, Missing pattern occurs earlier in the process flow and is not of concern for this inspection step as wafers were reused numerous times and wafer spots are the defect of interest. In the example below, classcode 24 is the missing pattern is a prior level nuisance defect at this inspection stage.

The Wet Bench uses liquid chemistry to clean or etch material. To save on consumable costs, test wafers tool monitors are reused numerous times to monitor the health of the wet benches. The challenge for ADC was to accurately classify water spots and to call all other defects as nuisance. If successful in finding and classifying the water spots, test wafer can be reused numerous times. The creation of one 300mm test wafer is about $1K. The expected saving would be of $3K a month.

In the creation of this ADC classifier, the key DOI is of water spots. Residual etch materials remaining on the wafer can cause major chip damage later in the processing of the wafer. The ADC setup objective was only to classify one defect type, water spots (fig 12) and filter out all other defects (fig 13) as nuisance.

Figure 12: Water Spot Top = Revisit optical image Bottom Left = inline scanner image.

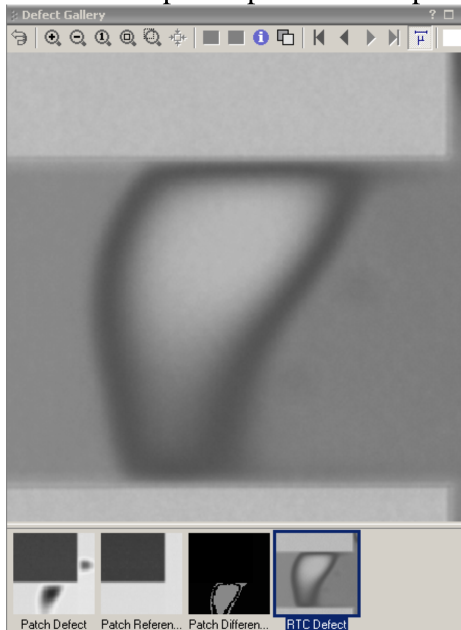
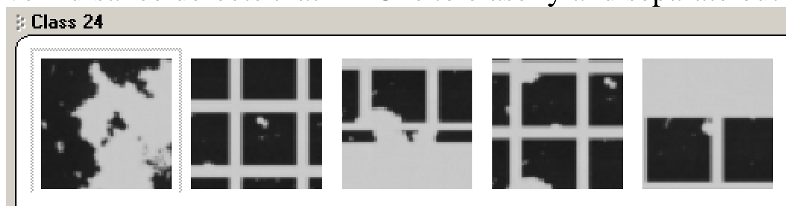


Figure 13: Nuisance Defect
Prior level nuisance defects that ADC is to classify and separate out from DOI.



The initial setup work showed that ADC was able to correctly classify water spots on the wafers and classify all other defects as nuisance. Initial results that one can monitor the health of the wet benches and an expected saving of inspection capacity as a pre-scan was not required as a post scan would see the DOI. Additionally benefit was the reuse of the test wafer expected to yield a saving of $3,000 a month.

Result 3 Cont.

In the above three examples, of Blocked Etch (ADC code 20), Falling lines (ADC code 92), Residual (ADC code 30) there is a huge statically value as ADC =100% classification & if DOI has good separation is of extreme value to mean time to detect excursion

Note: Can't expect that ADC will ever will ever be a direct match to SEM review.*

> ** Since ADC classification is done from the "Patch" images from inspectors (about 1/4 um resolution average recipe, and the resolution of the SEM is one order of magnitude better approx. 30nm.) So getting valuable data that you can trust from the inspector prior to going to the SEM that has 10times greater resolution is excellent!*

This process step and ADC classifer did not reach into final rollout into the wet bench monitoring. There was expected to be a saving of tool availability at only the post inspection was to be scanned which would result in a 50% improvement in cycle time of wafers run in this qual process. Given the proper classification and removal of prior level defects, it is expected that rollout at this process step would have had the added benefit of being able to reuse test wafers numerous time as only water spots were to be the defect of interest.

Summary

In three separate examples ADC was proven out to be of high value in a high volume wafer manufacturing.

a) Full stack micro-masking (yield detractor)

b) Fallen lines (yield detractor) and

c) Water spots (noise in defect signal).

In the Full Stack Micro-masking example the confidence in ADC made it possible to monitor individual etch chambers and additionally make decision a decision on DOE's that was an improvement to the material that was used as a liner to the etch chamber wall.

It is important to note that getting ADC classification for 100% of the defect did not impact cycle time of wafer scan time as this classification is done in parallel is able to keep up with the inspection detection. Creating a robust ADC classifier takes additional setup effort and some up front effort but is an extremely useful tool to help screen out unwanted defects and help to control the process from excursions.

In the three cases, it was shown that the ADC classification information adds value to the inspection results and helps to identify issues that would have been previously missed. With the introduction of automatic SPC Charts monitoring a ADC defect code that had a high correlation to yield impact, there was a much better control of the line. With a clear visibility and control at a process step, one would know very quickly when a tool maintenance issue arose.

Design of experiments (DOE's) that had the goal to improve a process area also took advantage of ADC as one would have quick feedback to a issue was improved upon.

With the quick feedback to DOE's, rather than waiting for end of the line chip yield data, yield improvement decisions could be made weeks improving profits.

A number of Unit Process area had a good control chart to monitor their process they had a sense on ownership to investigating problems to be fixed. ADC data proved to be very convincing to shut other process tools down in an excursion.

The ADC rollout show improved the reaction time excursion and much better signal to noise detection on specific design of experiments. Moving medians gave higher visibility and understanding to systematic and non-systematic issues in the manufacturing line. Automated charting and moving medians were setup so that lots would automatically go on hold for investigation which put the focus on solving the defectivity issues.

Once the ADC classifier was created, accuracy would be monitored with optical images along with SEM review and decisions to shut down process tools due to an excursion was done in short order. Additional proof of concept for the ADC data to set the SEM sample. Defects that are not current layer or no yield impact can be screened from the SEM review sample. Once unit process had a good ADC SPC chart to monitor tool performance, shutdowns occurred quicker and improvements to the process (DOE's) were done with quicker more favorable results.

Beyond the three examples of use cases and success of Blocked Etch, Falling Lines and the use case of Water Spots there were numerous other areas where ADC had a strong positive impact towards improving yield resulting in saving in dollars. The work that was performed with ADC on the Tungsten Deposition Step (70nm) yielded about a 3% increase in overall yield. Having the ADC tuned on and functioning allowed for 24

hour reaction and allowed an increase in time between kit changes once the root cause was resolved from about 5Khrs to 10Khrs at ~$15000 per kit change. Nitride step got an increase in yield of about 4%. The work on the Contact Barrier etch step (80 nm) increase yield about 2%.

The ability to react quicker to excursion $1.7M (see figure 14) and with the multiple improvements in etch and other unit process areas, the yearly improving yield improvement is $3.5M. With the combined baseline improvement to yield, the accumulated improvement is calculated to give a yearly baseline saving to in excessive of $5M a year.

Weekly and monthly meeting highlighted ADC success in the organization and the learning were passed to the sister facilities. The development facility reevaluated the benefit of ADC and with the well documented successes, was supportive in the utilization of ADC and ensured future inspection tools would require this feature.

Figure 14: Yield Improvement with Excursion Detection and Baseline improvement. Combined yield excursion and baseline yield improvement $5M yearly.

Assumptions

	Without ADC	**With ADC**
Dram Chip cost	$1.50	$1.50
Dram Chips per wafer	1,000	1,000
production line per week	10,000	10,000
Production days From Gate Contact to Final Test	4 weeks	4 weeks

Most excursions resolve on their own within two weeks, for calculations below assume 10 days

Excursions Yield Improvement

	1 Excursion	1 Excursion	**Ave. Cost Saving per excursion**
chips manufactured (per day)	1,428,571	1,428,571	
Line Impact (multiple products run)	15%	15%	
% wafer in product that will be impacted (most events are process tool issues)	25%	25%	
Ave. days in excursion condition before ADC	**10**	**3**	
Chip loss	$535,714	$160,714	
$ lost Dram	$803,571	$241,071	$562,500

Normally dealing 2 excursion every 3 weeks, (35 excursions per year)

Total yearly Excursion saving (estimate ADC improve reaction time to approx 3 excursions yr.) $1,687,500

Base-line Yield Improvement

production line per week (wafers)	10,000
production line per yr. (wafers)	520,000
chips per yr (dram)	520,000,000
Value of line per yr	$780,000,000
if overall 5% yield improvement entire line	$39,000,000
ADC has shown a 3% yield improvement across 15% line	$3,510,000

Conclusion

The rollout of ADC was proven to be successful to better monitor the line for process excursions and reduce the reaction time to excursions. An additional profound benefit of having ADC classification on defect with high kill probabilities resulted in an overall yield improvement across the manufacturing line. The combined yield improvement of reacting quicker to excursions and improvement to baseline yield was accumulated to give $5M a year in savings.

The utilization of moving median and ability to focus on current level defect of interest was instrumental in improving yield in numerous process areas and improve the overall health of the manufacturing line. The project lessons learned and success stories were propagated throughout the various sister facilities and helped to drive improvements at other locations.

Recommendations for future research

Much of the decision making of setting up an ADC classifier requires the Scanning Electron Microscope (SEM) to validate how good the classification is on the inspection station. The SEM is used for baseline review and to help troubleshoot excursion issues. Once there is confidence in the ADC inspection data, this can be automated to either drive the SEM Review sample with the goal to reduce the SEM baseline review.

Proof of concept was done in the ADC project rollout but did not automate smart skipping at the SEM due to the ADC Inspection review results. SEM review turned often to be the bottleneck for the production fab during the rollout of ADC.

This project did not investigate ADC on the SEM and was primarily focused strictly on ADC on the inspection stations. It would be very interesting to test out some of the new capabilities with SEM review ADC (Nakagaki, 2009). Investigation should incorporate recent new patents on SEM ADC and require all the latest improvements to image stability on the SEM.

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