Controlling Interface for Metal-Insulator-Metal Architectures with Ultrathin Dielectric Fabricated Using Atomic Layer Deposition and Sputtering

By

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Abstract

The miniaturization of future microelectronics demands the development of high quality ultrathin (few to sub-*nm*) dielectric films for application in metal-insulator-metal (MIM) architectures. Among all other approach employed for ultrathin dielectric film fabrication, atomic layer deposition (ALD) provides a unique approach for the fabrication of ultrathin TBs with several advantages including an atomic-scale control on the TB thickness, conformal coating, and low defects density. Despite extensive efforts in ALD devices, the figure-of-merit dielectric constant (ε_r) exhibits a significant monotonic decrease with the film thickness as compared to bulk single crystal value. Primarily, the control over metal-insulator (M-I) interface, specifically in ultrathin thickness range, remains a challenge due to the formation of defective oxides and interfacial layer (IL). This work demonstrates the development of high quality Al/ALD Al_2O_3/Al MIM trilayers using a unique in-house integrated *in situ* deposition (sputtering/ALD) method. These trilayers devices were characterization to understand and control the IL formation with atomic precision. To the best of our knowledge, high ε_r ~8.9 that is within 3% of the bulk value ~9.2 has been achieved for the first time on the ALD Al_2O_3 films in thickness range ~3.3-4.4 *nm*. This corresponds to an effective oxide thickness ~1.4-1.9 *nm* comparable to High-K HfO_2 of 3-4 *nm*. The low leakage current density (J) ~10^{-9} A/cm^2 is an order of magnitude lower than the best previously reported values. These results suggest that the optimal ultrathin high quality ALD Al_2O_3 provides a much lower-cost alternative for gate dielectric. Also, ALD Al_2O_3 seed layer (SL) approach was used to illustrate the critical importance of control over M-I interface to obtain dense hydroxylation and reduce incubation period, improving the dielectric properties of ultrathin ALD

MgO films. ALD MgO with SL demonstrated ε_r ~8.8-9.4 in thickness range ~3.8-4.9 *nm* comparable to bulk MgO ~9.4. In contrast, low ε_r ~3.6-4.7 was observed for ALD MgO without Al_2O_3 SL in a similar thickness range. Both the scanning tunnelling spectroscopy and ab-initio molecular dynamics studies point out that SL allows the initial dense nucleation and perfect interface resulting in a high quality dielectric with tunnel barrier height (E_b)~1.5 eV compared to 0.8 eV for MgO without SL. This result provides an approach to engineering incompatible M-I interface using a SL for obtaining high quality dielectric as required for applications in MIM tunnel junctions and CMOS. In addition, tuning thickness of Al wetting layer (t_{Al}) in capacitors consisting of Nb (25 *nm*)/Fe (20 *nm*)/ALD Al_2O_3 (2.2 *nm*)/ t_{Al}/Fe (20 *nm*)/Nb (50 *nm*) shows switching between pure dielectric behavior for t_{Al} >1 *nm* and ferroelectric/dielectric (FE/DE) bilayer at $t_{Al} \leq$ 1 *nm*. These FE/DE bilayer gate with ultrathin DE are promising for low power microelectronic devices. This helps to realize FE/DE bilayer capacitors with a total FE/DE total thickness < 3-4 *nm* that show a dynamic switching on/off of the negative capacitance under the application of an external force. This result not only provides a viable approach for generating ultrathin FE/DE bilayer capacitors but also offers a promising solution to low-power consumption microelectronics and piezoelectric sensors applications. Pinhole-free and defect-free ultrathin dielectric tunnel barriers (TBs) is a key to obtaining high tunnelling magnetoresistance (TMR) and efficient switching in magnetic tunnel junctions (MTJs). Motivated by this, this work explores fabrication and characterization of spin-valve Fe/ALD-Al_2O_3/Fe MTJs with ALD Al_2O_3 TB thickness of 0.55 *nm* using *in situ* ALD. Remarkably, high TMR values of ~77% and ~ 90% have been obtained respectively at room temperature and at 100 K, which are comparable to the best reported on MTJs

having thermal AlO_x TBs with optimized device structures. *In situ* scanning tunnelling spectroscopy characterization of the ALD Al_2O_3 TBs has revealed a higher tunnel barrier height E_b of 1.33 *eV*, in contrast to E_b~0.3-0.6 eV for their AlO_x TB counterparts, indicative of significantly lower defect concentration in the former. This first success of the MTJs with sub-*nm* thick ALD Al_2O_3 TBs demonstrates the feasibility of *in situ* ALD for fabrication of pinhole-free and low-defect ultrathin TBs for practical applications and the performance could be further improved through device optimization.

This work is dedicated to my respected parents

Mr. Bala Krishna Acharya and Mrs. Kamala Acharya

and

to my beloved wife

Mrs. Samita Sapkota Acharya and son Ivaan Acharya, welcome baby!

Declaration

I hereby declare that except where otherwise stated, the contents in this dissertation is the result of my own work and includes a part of results which is the outcomes of work done in collaboration. The results have not been submitted in whole or in part for consideration for any other degree or qualification in the University of Kansas, or any other University. This dissertation contains around 37500 words including bibliography, footnotes, figures, tables, and equations, and has less than 60 figures.

Jagaran Acharya

November 25, 2019

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TB	Tunnel barrier
TJ	Tunnel junction
MIM	Metal-insulator-metal
NVM	Non-volatile memory
M-I	Metal insulator
FinFET	Fin field effect transistor
JJ	Josephson junction
MTJ	Magnetic tunnel junction
CMOS	Complementary metal-oxide-semiconductor
GMR	Giant magnetoresistance
TMR	Tunnelling magnetoresistance
FM	Ferromagnetic materials
GGA	Gate all around
J_c / J	Critical current density/ Leakage current density
DOS	Density of states
E_f /E_b	Fermi energy/ Barrier height
ALD	Atomic layer deposition
IL /SL	Interfacial layer/Seed layer
MRAM	Magnetoresistive Random-Access Memory
FE/DE	Ferroelectric/Dielectric

Chapter 1 Introduction

Since the early 1970's, Moore's law is the driving principle behind the advancement in the semiconductor industry that predicted the density of transistors in an integrated circuit double approximately every two years [1]. Following this law, the size of transistors decreased from 10 μm to 10 *nm* over the past few decades, with 7 and 5 *nm* technology are predicted to be prominent in future electronic devices [2]. Consequently, SiO_2 gate dielectric has decreased its thickness from hundreds of *nm* to few *nm* [3]. The further miniaturization of microelectronics towards the reduced dimensions demands ultrathin dielectric (few *nm* to sub-*nm* thickness) in range of 1-2 *nm* or below [4-13]. The applications requiring such ultrathin high quality dielectrics include metal/insulator/metal (MIM) architectures [10, 12, 13] and tunnel junctions (TJs) [9, 14-18]. As technology approaches the end of Moore's law and beyond the control over metal-insulator (M-I) interface with atomic precision, low defect density, and uniformity have become critically important for future microelectronics device applications [19].

1.1 Metal-Insulator-Metal Architecture

MIM architecture is the simplest trilayer structure with insulating barriers (like Al_2O_3, MgO, HfO_2, etc.) in the few nanometers thicknesses range sandwiched between two metal electrodes. These architectures are the building blocks for many microelectronic circuits like gate dielectrics in complementary metal-oxide-semiconductor (CMOS) technology [10, 12, 13]. CMOS technologies have been the driving principle for the innovation and advancement in logic-based devices over

the past decade due to a significant reduction in the dimension of gate dielectric. Along with the reduction in the gate dimension, SiO_2 dielectric is approaching its physical limitations below 1.3 *nm* thickness due to considerably increased leakage current density (J) of 1-10 A/cm^2 that occurs primarily due to the difficulties in controlling the defects in ultrathin SiO_2 [3]. This not only prevents achievement of the required gate voltages for device operation, but also exceeds the required threshold of ~10^{-3} A/cm^2 for high-performance, low-power consumption microprocessors by several orders of magnitude [3, 20-23]. The difficulties in down-scaling the SiO_2 dielectric gates have motivated an intensive research on high-K dielectric materials [24, 25]. Considering the higher dielectric constants (ε_{Hik}) than that of SiO_2 (ε_r ~3.9), the high-K dielectric can achieve an effective oxide thickness (EOT=$t_{HiK}\cdot 3.9/\varepsilon_{Hik}$) in the range ~1-2 *nm*, with a larger thickness t_{HiK} that reduces J [26-28]. For example, in order to achieve an equivalent SiO_2 dielectric of thickness t_{SiO2}~1.5 *nm* with the specific capacitance given as ($Co=C/A=\varepsilon_o\, 3.9/\, t_{SiO2}$), the corresponding thickness of high-K material HfO_2 with ε_{Hik} ~20 is ~ 7.7 *nm* for same value of Co, which results in the lower $J \sim 10^{-5}$ A/cm^2 [22].

Using high-K dielectric material new architectures designs like fin field-effect transistors (FinFETs) have been developed that uses a conformal spacer gate as shown in Figure 1.1(a) to decrease power consumption and efficiently control switching on/off operation [26-28]. Compared to a standard planar transistor, this allows for better performance and voltage scaling as the process node decreased, by minimizing the transistor limitations like high leakage and high-power consumption [26-28]. Despite the progress made in ultrathin high-K gate dielectric of a few *nm* in

thickness, further reduction of their thickness remains challenging due to the difficulties in controlling defects, which is similar to the SiO_2 dielectric case [26, 28]. Recently, vertically aligned nanowires have been used in the development of three-dimensional (3D) gate architectures to keep up requirement of low power and high performance devices with scalability [29].

Applications requiring ultrathin high quality dielectric include the Josephson junctions (JJs) for quantum computing. When two superconducting layers are brought together within a few nanometers range, the superconductor wave functions couple together, allowing Cooper pairs, which are paired electrons to tunnel through the ultrathin barrier as in Figure 1.1(b). For quantum computing, the superposition of quantum states must have long coherence times. If the qubits couple too strongly with defects, then the entangled state will be lost, and the computation cannot be performed. While JJ qubits are entangled, their short coherence times have been problematic due to two-level fluctuations (TLFs). Most studies shows that defects in the dielectric materials particularly oxygen vacancies and interstitials in the tunnel barrier (TB), are the primary source of TLFs [30]. This decoherence in JJs is a major challenge, that results in the collapse of qubits wave function before computation completes [30]. This requires better control over the fabrication process with stoichiometric and defect free ultrathin high quality dielectric critical for improving the performance of JJs, which is challenging using current state of the art processes [31].

Another TJs application includes magnetic tunnel junctions (MTJs), which uses an ultrathin insulator sandwiched between two ferromagnetic (FM) materials that allow spin polarized electrons to tunnel through the barrier as shown in Figure 1.1(c). The most important property of

MTJs is that the spin dependent current depends on the relative orientation of the magnetization in ferromagnetic magnetic (FM) layers [31, 32]. In MTJs, defective oxides lead to the scattering and spin flip of spin polarized electrons passing through the FM layer. The oxygen vacancies and defects are unavoidable in the ultrathin dielectric films fabricated using the thermal oxidation process [31]. These vacancies and defects can effect the conductance by non-resonant scattering of electrons causing a substantial reduction of magnetoresistance (TMR). The fabrication of high quality TB with reduced oxygen vacancies and defects concentration results in the less scattering and coherent spin tunnelling resulting better TMR. The current approaches in achieving the logic functionality with MTJs include designing an integrated CMOS and MTJ circuit, where CMOS devices are used for implementing the required intermediate read and write circuitry. MTJ based logic has great potential because of the non-volatility, practically unlimited endurance, CMOS compatibility, and fast switching speed. By direct communication between spin-transfer torque (STT) in MTJs, several realizations of intrinsic logic-in-memory circuits have been demonstrated for which the MTJ devices are used simultaneously as fast access nonvolatile magnetic memory and computing elements [33-35].

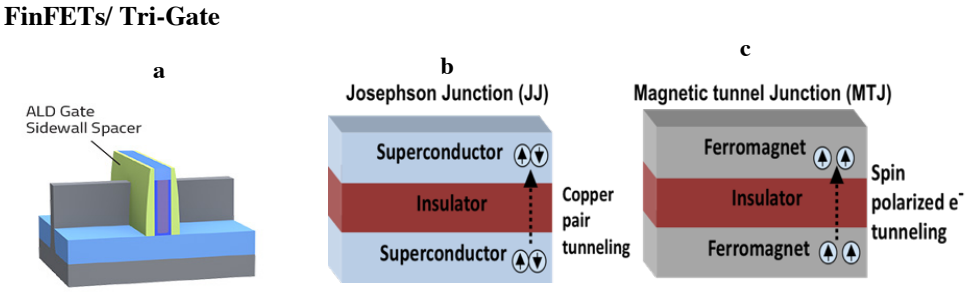

Figure 1.1 Schematic of metal-insulator-metal architecture a) conformal ultrathin ALD sidewall spacer gate dielectric in field effect transistors (FinFETs) or Tri-Gate for complementary metal-oxide-semiconductor (CMOS) technology b) Josephson Junction with ultrathin dielectric sandwich between two superconducting electrode with Copper pair tunnelling and c) Magnetic Tunnel Junctions with ultrathin dielectric sandwich between two ferromagnetic electrode with spin polarized electron tunnelling.

Navigating these trends of continuing miniaturization of devices, there is an increasing demand for the fabrication of ultrathin TB with low *J*, low defect concentration and uniform over the large wafer to increase device' performances as demanded by today's technological advancement. One critical issue with current state of the art thermal oxidation processes is the presence of defects and pinholes at ultrathin thickness, which is unavoidable [31]. Another challenge is precise control over dielectric thickness, its quality and interfaces with metals. However, the precision thickness control in sub nanometres range without pinholes and defects free uniform TB is demanded for future applications. Thus, the M-I interface needs to be controlled well to obtain high quality ultrathin dielectric for potential application in future microelectronics.

1.2 Gate Dielectric for CMOS

There are several device architectures developed to address the critical issue with the increase in leakage current with a corresponding reduction in the dimension of gate dielectric approaching its

physical limitations [20, 21]. Among these, FinFETs architecture with uniform ultrathin spacer gate dielectric has been developed to increase the contact area between the channel of the transistor and the gate. By scaling in a vertical direction, this allows faster switching times and higher *J*. However, like planar transistors, FinFETs transistors will eventually reach a point where they cannot scale further as process technology nodes shrink. To scale, the contact area between the channel and the gate needs to increase. The way to implement this is to use a gate-all-around (GAA) architecture. The GAA design allows transistors to stack vertically, rather than laterally. Three-dimensional (3D) tri-gate fin transistors have been used for 14 *nm* technology node that deliver incredible performance, power, density, and better cost per transistor. This provides manufacturing of a wide range of high performance to low power devices. This advancement in 3D architecture will continue with future complex device architecture demanding the fabrication of uniform, conformal, pinhole and defect-free ultrathin gate dielectrics to meet the requirement of low *J*.

Following the exponential dependence in technology node as predicted by Moore's Law, the cost of a single transistor on silicon chip during the last few decades has decreased more than a million-fold, as the number of devices on a single chip have also increased more than a million-fold. As the further advancement in microelectronics continues devices require a reduction in their dimensions. In CMOS technology, there is a continuing drive to shrink silicon devices that requires gate oxide layers with thickness ~1 *nm* or below [20, 21]. Future scaling has been the next important question in today's semiconductor industry, especially because numerous challenges arise from both the device physics and manufacturing capabilities perspective. The traditional

scaling based on the reduction in the physical dimensions of CMOS transistors, with simultaneous reduction of supply voltages and dissipated power, is reaching its limits. Intel introduced its advanced manufacturing process technology to help deliver the expected benefits of Moore's Law popularly known as the "Tick" cycle [36]. However, electron at this thickness produces high leakage current and device instability [20, 21]. The deposition of ultrathin uniform SiO_2 films and maintaining the insulating properties has also become increasingly difficult. High-K dielectric materials are currently being investigated to achieve higher capacitances with thicker films to obtain low leakage current, a high dielectric constant (ε_r), and high breakdown strength to achieve high capacitance densities [26, 27]. The continuous application in today's process technologies includes the next big innovation in processor microarchitecture known as the "Tock" cycle. This "Tick-Tock" model still allows to follow with the empirical Moore's Law [36]. However, this decreasing size comes at an increasing cost, so most recent technology generations do not offer much advantage in terms of cost per transistor, or cost per function, when compared to the previous nodes. Intel recently announced its focus is now shifted on "Process-Architecture-Optimization". This includes the introduction of new materials and innovative techniques for the optimization of device performance. The efficient control in the gate dielectric is the main reason for the success of CMOS technology that allows the integration of more than a billion transistors on a chip to make portable computers and smartphones viable. However, the increase in dissipation power density, especially standby power, has resulted in a trade-off between performance/speed and low-power requirements.

As Moore's law is approaching its physical limitations due to its increased energy consumption and complexity in design, the reduction in the size of transistors cannot keep up as demanded by today's technological advancement. The International Technology Roadmap for Semiconductors predicts that the semiconductor technology will reach its last generation by the year 2025 [37]. In order to address these problems, the new paradigm called "More than Moore" is commonly used in today's technology [38]. Ultimately, the devices that use charge as the fundamental element to store information will soon reach its power and capacity limitations. The new architecture and functionality with reduced device dimension demand high quality ultrathin dielectric. These results in an increase in coherent tunnelling improving the device performances as demanded by current technological advancement.

1.3 Magnetic Tunnel Junction

Spintronics is a relatively new concept that utilizes the spin degree of freedom of electrons to control the flow of electrical current expanding the power and capability of electronic devices. Spin-polarized current can be generated by exploiting the influence of spins on the transport properties of electrons in FM, which has an imbalance in density of states (DOS) for majority and minority carriers due to spin-orbit interaction [39]. With the advancement in thin film deposition techniques, such as sputtering and molecular beam epitaxy (MBE), the fabrication of multilayered structures composed of thin individual layers in the order of nanometres became feasible. These layers have thickness smaller than the mean free path of electrons that helped to realize new quantum mechanical phenomenon. Fert *et. al.* [40] and Grunberg *et. al.* [41] in 1988, first

discovered that the resistance of Fe/Cr/Fe multilayer structure changed based on the relative orientation of the two layers leading to the discovery of giant magnetoresistance (GMR). The orientation of FM layers depends on the direction of local spin polarized electrons with the majority carriers in the FM layers. Figure 1.2(a) shows anti-parallel orientation of two FM layers with majority spin carriers (i.e. red in top layer and blue in bottom layer) separated with non-magnetic layer (yellow). The majority carriers in both layers suffer large scattering from either of these layers. This results in a low spin polarized current or high resistance through the multilayer structure. However, when orientation of these layers is parallel (i.e. blue electrons) as in Figure 1.2(b), only minority carrier (i.e. red electrons) suffer scattering from both layers resulting in high majority blue spin polarized current or low resistance through the multilayer structure. This relative change in the resistance between parallel and anti-parallel orientation is known as GMR. The orientation of these layers can be changed by the application of the external magnetic field. These GMR structures were later commercialized to make magnetic sensors with an increase in the areal density of information stored on the hard disk drives.

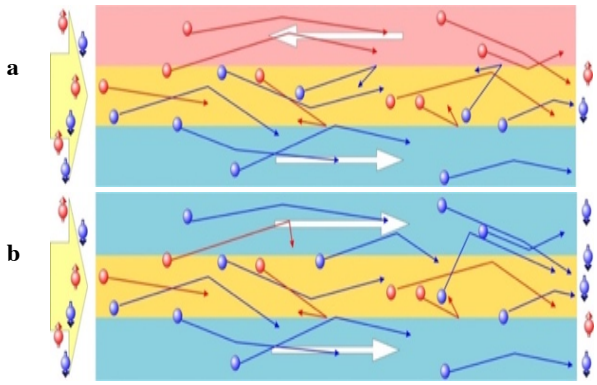

Figure 1.2 Schematic of giant magnetoresistance device structure with two FM electrodes in a) anti-parallel orientation (*i.e.* red and blue) layers separated by non-magnetic electrode (*i.e.* yellow) resulting low spin polarized current (or high resistance state) and b) parallel orientation (*i.e.* blue and blue) separated by non-magnetic electrode (*i.e.* yellow) resulting high spin polarized current (or low resistance state).

1.4 Physics of Spin Tunnelling

Replacing the non-magnetic layer (*i.e.* yellow) in GMR structure with insulating material in the thickness range of 1-2 *nm* results in the spin polarized electron tunnelling between two FM layers [32]. Figure 1.3 shows the schematic of electron wave function incident on the potential barrier with the ultrathin insulator, the evanescent states in the barrier have a finite probability of tunnelling through the insulator. Consider the bias voltage (V) applied between two metal electrodes raises fermi energy (E_f) of one metal electrode relative to other by an electron volt (eV). The number of electrons/spins tunnelling from one electrode to another is given by the product of density of states (DOS) at the given energy of in the left electrode (ρ_l(E)) and DOS at same energy in the right (ρ_r(E)) multiplied by probability of transmission matrix (T) through the barrier. The probability that states are occupied in left electrode is f(E) and in right is 1- f(E-eV) respectively,

where f(E) is the Fermi-Dirac distribution function. The total tunnelling current (I) is the difference between the left and right given by equation (1).

$$I(V) = I_{l\to r} - I_{r\to l}$$

$$= \int_{-\infty}^{+\infty} \rho_l(\mathrm{E}).\rho_r(\mathrm{E}-\mathrm{eV})\,|T|^2\, \mathrm{f}(\mathrm{E})\,[\mathrm{f}(\mathrm{E}-\mathrm{eV})-\mathrm{f}(\mathrm{E})]\mathrm{dE} \qquad (1)$$

The expression for tunnelling current can be obtained by assuming the square type potential barrier from simple undergraduate quantum mechanics, where the tunnelling probability is obtained as

$$T = \frac{16\,E_f.E_b}{\left(E_f+E_b\right)^2}\; exp^{-2d\sqrt{\frac{2m}{\hbar^2}E_b}} \qquad (2)$$

where E_f and E_b are the Fermi level of the metal electrode and the barrier height of the insulator respectively, m is the mass of electrons, $\hbar$ is the Planck's constant, and d is the thickness of the insulator.

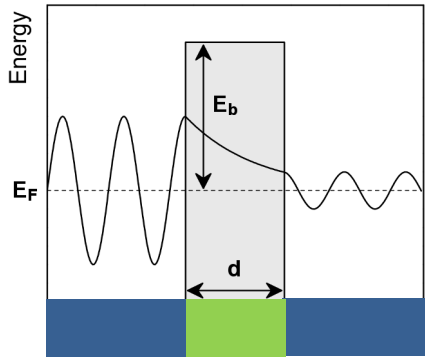

Figure 1.3 Schematic of the metal-insulator-metal structure with ultrathin 1D potential barrier with barrier height (E_b) and thickness (d) showing the basics of quantum tunnelling in which the electron wave function decays exponentially across barrier for electrons with the Fermi energy (E_f).

From equations (1) and (2) the I is proportional to$\sim exp^{-d\sqrt{E_b}}$. Thus, the wave function decays exponentially across the barrier, which demands the fabrication of ultrathin dielectric to increase the tunnelling current. However, obtaining high quality dielectric at ultrathin thickness with fewer defects and pinholes with higher E_b is challenging. The external applied voltage (V) across the barrier effectively lowers the average E_b for electron tunnelling in one electron spin and raises the average E_b for electrons tunnelling in opposite spin by eV. This leads to the increase in current with increase in V, which is the characteristic for quantum tunnelling. Thus, the tunnelling conductance in low bias voltage is obtained by equation (3).

$$G = \frac{dI}{dV} \sim \int_{-\infty}^{+\infty} \rho_l(\mathrm{E}).\rho_r(\mathrm{E}-\mathrm{eV})\,|T|^2 f(E)\,\frac{df((\mathrm{E}-\mathrm{eV}))}{dV}\,\mathrm{dE} \qquad (3)$$

1.5 Tunnelling Magnetoresistance

Tunnelling magnetoresistance (TMR) is the consequence of spin-dependent tunnelling through an ultrathin barrier in FM electrodes. In MTJs, the magnetization direction of one FM layer that is pinned known as the "fixed layer", while the other FM layer known as the free layer can change its magnetization direction under the application of external magnetic field or spin polarized current known as "free layer" as in Figure 1.4(a). MTJ is designed to have two stable magnetic states (i.e. parallel and anti-parallel) depending on the local spin polarized electrons. When the orientation of two layers are in the parallel direction, both the majority and minority carriers have available states in other FM material to tunnel through the insulator, resulting in a high current or a low resistance state known as parallel resistance (R_P) configuration as in Figure 1.4(b). However, if the orientation of the two layers are in opposite direction, the majority (minority) states available in one FM have less available states in other FM, resulting in low current or a high resistance state known as anti-parallel resistance (R_{AP}) configuration as in Figure 1.4(c). Thus, depending upon the relative orientations of magnetic layers bit "0" and "1" can be stored for R_P and R_{AP} configuration respectively. The information about a stored bit is read out using low sensing current as in Figure 1.4(d).

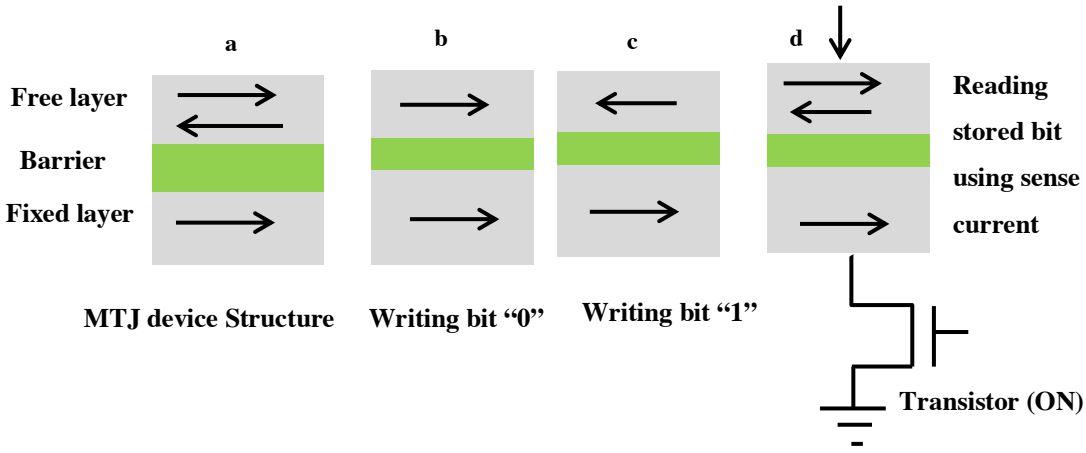

Figure 1.4 Schematic of a) MTJ structure with free layer (top), fixed layer (bottom) and tunnel barrier (middle) b) writing bit "0"(with parallel resistance R_P configuration) c) writing bit "1" (with anti-parallel resistance R_{AP} configuration) and d) reading the stored bit using sense current and compare the output with transistor.

TMR can be obtained as the difference of conductances or resistances in two resistance state as

$$\mathrm{TMR} = \frac{\mathrm{G_P} - \mathrm{G_{AP}}}{\mathrm{G_{AP}}} \times 100\ \% = \frac{\mathrm{R_{AP}} - \mathrm{R_P}}{\mathrm{R_P}} \times 100\ \%. \qquad (4)$$

where G_{AP} and G_P, and R_{AP} and R_P are conductance and resistance for anti-parallel and parallel configuration respectively. The TMR can also be explained with the concept of DOS of FM as shown in Figure 1.5(a) and (b). With parallel configuration there are more available states for the majority spin polarized electrons tunnelling through one FM electrode to the other FM resulting low resistance state R_P. However, in anti-parallel configuration there are less available states for the majority or minority spin polarized electrons tunnelling through one FM electrode to other FM resulting in the high resistance state R_{AP}. Based on the assumption for high quality MTJ that during tunnelling the spin of electron is conserved with no spin-flipping occurs, TMR can also be expressed in terms of the magnitude of polarization of FM materials using Julliere model [32]

$$TMR = \frac{2\,P_1\,P_2}{1-P_1\,P_2} \times 100\,\% \qquad (5)$$

where P_1 and P_2 are the magnitude of spin polarization of two electrode materials. The conductance in each channel is thus proportional to the tunnelling probability, which is determined by Fermi's golden rule [31]. Thus, the tunnelling probability which depends choice of FM material depends on the number of available free spin polarized electron as given by

$$P = \frac{N\uparrow(Ef)-N\downarrow(Ef)}{N\uparrow(Ef)+N\downarrow(Ef)} \qquad (6)$$

where N are the number of spin polarized electrons available for tunnelling near E_f.

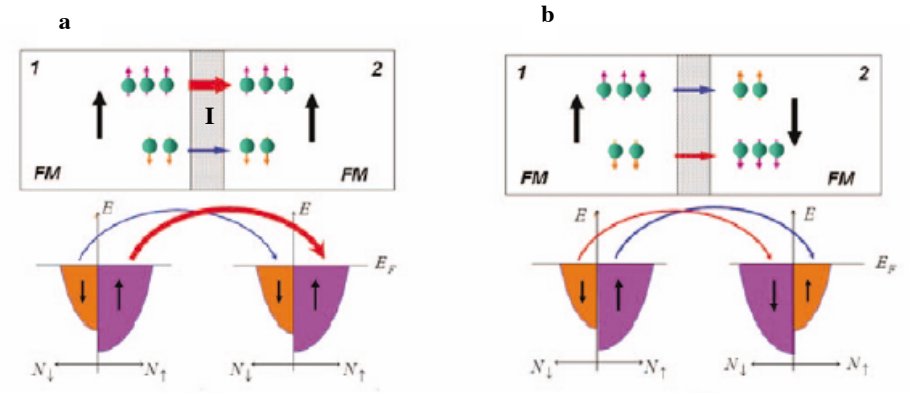

Figure 1.5 Schematic of tunnelling magnetoresistance (TMR) in MTJ structure showing spin tunnelling with a) parallel configuration with spin up as majority carriers in both FM electrodes (Bottom left figure shows density of states of corresponding to the FM electrodes in parallel configurations); and (b) anti-parallel configurations with spin up as majority carriers in FM1 and spin down as majority carriers in FM2 (Bottom right figure shows density of states of corresponding to the FM electrodes in anti-parallel configurations). This figure is adapted from reference [31].

Most of the FM like Fe, CoFe and CoFeB have in-plane magnetization with easy magnetization axes that lie in-plane (i.e. 0 or 180°), while the hard axis lies perpendicular to plane (i.e. 90°) as in Figure 1.6. There is a difference in the energy between easy and hard axes in FM material known

as magneto crystalline anisotropy. Thus, the randomization of stored bit prevented at room temperature (RT) unless the external energy is supplied to overcome this energy barrier, which is much higher than the thermal energy $K_B T \sim 25$ meV available at RT.

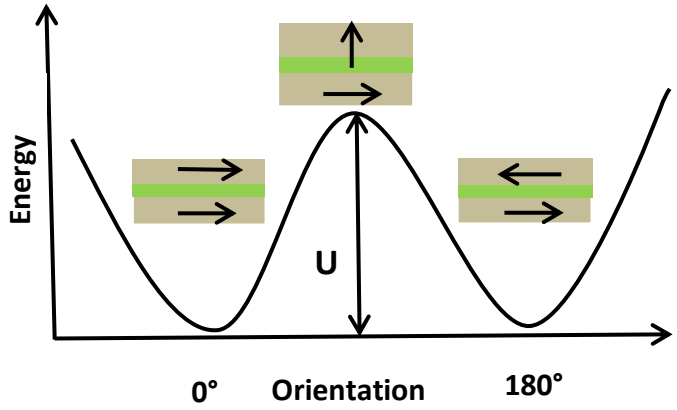

Figure 1.6 Schematic of switching energy of MRAM device structure where randomization of spin is prevented with energy barrier (U) required to overcome to switch from easy axis magnetization direction (*i.e.* 0° to 180°) to perpendicular to the plane configuration (90°) for non-volatile memory applications.

1.6 Application of MTJs

Over the past few decades, MTJ research has become an active area of research and significant progress has been made in the fabrication of devices for magnetic sensors and non-volatile magnetoresistive random-access memory (MRAM) devices, which plays a major role in a wide variety of microelectronics applications. The revolution in today's digital information storage came with the increase of storage density of hard disk drives by several orders of magnitude. This became possible only when traditional anisotropic magnetoresistance sensors were replaced with GMR and TMR sensors allowing decreases in the size of a bit. Recent research includes the

fabrication of magnetic materials with perpendicular magnetization that utilize interface perpendicular anisotropy between the CoFeB–MgO interface resulting in a large TMR [42]. MRAM based MTJs have now begun to commercialize and replace other random-access memories or embedded CMOS logic devices. Figure 1.7(a) shows a conventional MRAM device structure using magnetic field induced writing by the current passing through the bit line (BL) and write world line (WWL), where the magnetic field does not scale proportionally with current with decrease in the dimension of BL. The newly introduce spin transfer torque (STT) devices use torque exerted by a spin polarized current to the flip the magnetization direction in FM known as STT-MRAM as in Figure 1.7(b). This offers an efficient way of rewriting the memory with low power consumption and scales proportionally with current. The current STT-MRAM technology use an array of MTJs with an easy axis of magnetization oriented out of the plane of the layers to obtain high density MRAM devices [43, 44]. This offers an efficient way of reducing long start-up power consumption but provides the key advantages of high density as in dynamic-RAM, high speeds comparable to Static-RAM and non-volatility like Flash storage.

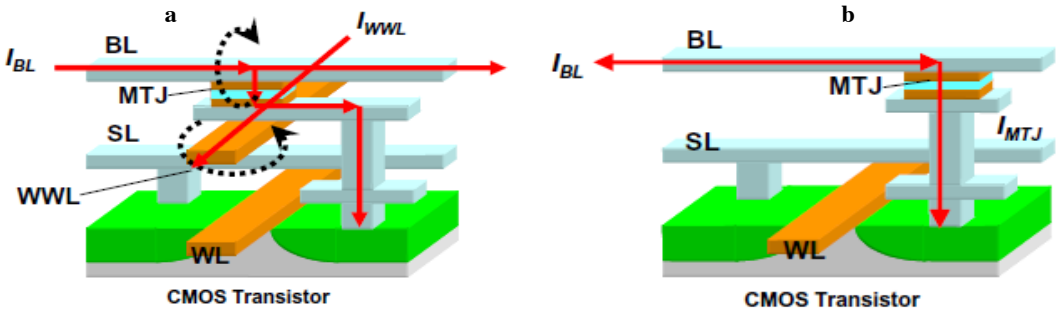

Figure 1.7 Schematic of (a) conventional MRAM device using magnetic field induced writing by the current passing through bit line (BL) and write world line (WWL) and (b) STT-MRAM device with spin transfer torque magnetization switching with write operation performed by passing the current directly through MTJs. This figure is adapted from reference [43,44].

1.7 Recent Progress in MTJs

The discovery in1975 by Julliere [32] in Co/Ge/Fe with TMR~14% at 4.2 K did not receive much attention due to its limited low temperature applications. Moodera *et al* [45] and Miyasaki *et al* [46] in 1995 observed TMR~70% at RT on MTJs made with amorphous AlO_x barrier that increased the intensive research in this area [47]. Due to the amorphous nature of the barrier FM electrodes do not have crystallographic symmetry, a variety of Bloch waves with different symmetries couple with evanescent states in AlO_x TB as in Figure 1.8(a) [48]. However, at ultrathin dielectric thickness, AlO_x suffers from defects and impurity creating a non-uniform insulator across the device that results in non-coherent spin tunnelling, where the spin of electrons is not conserve resulting in the scattering and spin flip as shown in the transmission electron microscope (TEM) image in Figure 1.9(a). However, highly crystalline TB

preserved the symmetry of the electronic states tunnelling in FM electrodes known as coherent tunnelling as in Figure 1.8(b). Figure 1.9(b) shows the corresponding TEM image with crystalline MgO barrier in CoFeB/MgO/CoFeB after post annealing at 500 °C [31]. This is the key to increasing tunnelling probability of majority and minority electronic states in FM electrodes with evanescent states in a highly crystalline MgO barrier [48]. Also, a first-principles theoretical calculation in epitaxial Fe/MgO/Fe MTJ shows the possibility of high TMR ~1000% [49] that accelerated the research and development of MTJs using MgO TBs.

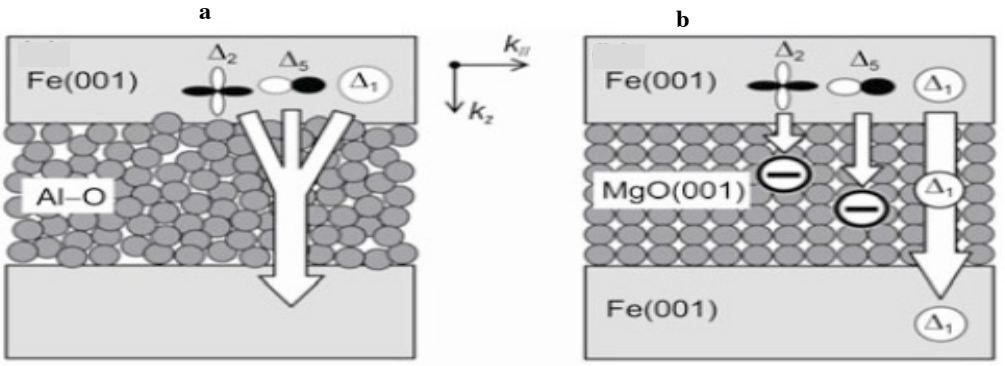

Figure 1.8 Schematic of different electronic states tunnelling through (a) amorphous AlO_x with variety of Bloch waves with different symmetries couple with evanescent states in barrier resulting non-coherent tunnelling and (b) crystalline MgO barrier that can preserve the symmetry of different electronic states tunnelling in FM electrodes resulting coherent tunnelling. This figure is adapted from reference [31].

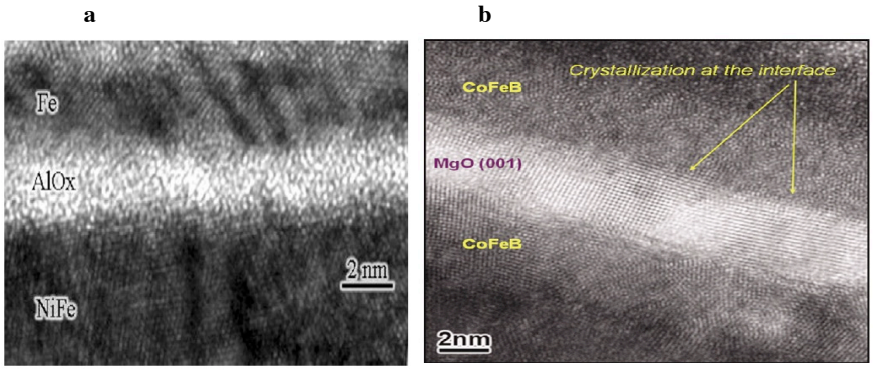

Figure 1.9 Transmission Electron Microscope (TEM) image of a) Fe/AlO_x/NiFe showing non-uniform amorphous AlO_x. This figure is adapted from reference [31] and b) CoFeB/MgO/CoFeB showing crystalline MgO barrier after post annealing at 500 °C. This figure is adapted from reference [48].

Table 1 shows the progress made in fabrication of epitaxial MTJs fabricated using the molecular beam epitaxy (MBE) process under the same condition but with different FM electrodes showing an increase in TMR by changing from Fe to Co. The high TMR in epitaxial MTJs is due to coherent spin tunnelling as discussed before. This improvement in TMR is in agreement with first-principles calculations that predict the minority electronic states in Co lies well below E_F. This is reflected during spin tunnelling at anti-parallel orientation [50]. Although, the MBE process uses layer-by-layer growth that allows atomic-scale control for the fabrication of epitaxial MTJs, this technology is expensive and is difficult to scale up for the industrial applications. Besides, large size crystalline MgO substrate is not available currently for large scale production in industry, which makes production process unreliable.

Table 1.1 Progress made in MBE fabricated MTJ.

MTJ structure	TMR in % (Year)
Fe/MgO/Fe [51]	180 (2004)
Fe/MgO/Co [52]	270 (2005)
Co/MgO/Co [4]	410 (2006)

Magnetron sputtering is an industrial proven technique and has been applied for fabrication of MTJs on SiO_2/Si substrate, which is the foundation for many electronic devices. However, SiO_2/Si is not a well suited substrate for epitaxial growth of MTJs due to its amorphous nature and large lattice mismatch with popular FM materials such as Co, Fe, and their alloys. Sputtering process deposit amorphous MTJs on SiO_2/Si substrate and post annealing is essential for improving the crystallinity. The sputtered polycrystalline CoFe and MgO based MTJ show TMR 220% [53] after annealing at 350 ℃ for 30 minutes. A slightly improved to TMR ~230% was observed after annealing at 360 ℃ for 2 hours under the magnetic field of 8KOe [54]. CoFeB is another popular FM with the highest degree of spin polarization and highest reported TMR so far. The improvement in TMR with CoFeB based MTJs is due to improved crystallinity of MgO after post annealing at high temperature ~ 500 ℃ [55]. This process is only limited for research and development with different challenges needing to be overcome to make its suitable for application.

1.8 Challenges and Alternative Approaches

1.8.1 Issues in Synthesis of Ultrathin Dielectric

The current state of art fabrication process uses thermal or plasma assisted oxidation of Al or Mg for the fabrication of AlO_x and MgO TB. This method is considerably much simpler and compatible with industrial applications. The thickness of a TB on the Al metal surface is estimated by controlling the exposure (*i.e.* pressure and time) and temperature during oxidation. Figure 1.10(a) shows a schematic for the growth mechanism for thermal AlO_x TB with defects and pinholes present at ultrathin thickness resulting in defective dielectric film. The TB growth increases exponentially with the oxygen exposure. Figure 1.10(b) shows J_c vs oxygen exposure for JJs, which clearly show two regions with two different slopes. The slope is almost constant with less scattering above 0.5 *nm* TB, which is an indication of low defects and pinholes. However, below 0.5 *nm* the slope is stepper with a sudden increase in J_c due to the presence of defects, such as oxygen vacancies and pinholes providing an additional tunnelling states resulting in an increase in leakage current. This led to the formation of a poor interface between M-I that cannot preserve the symmetry of electronic states due to coupling of the evanescent states in the TB resulting in incoherent tunnelling that significantly reduces the spin current [31].

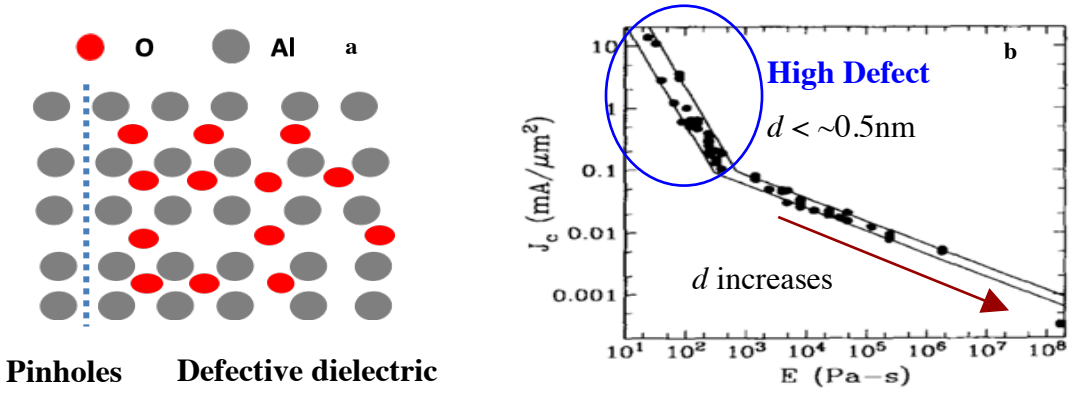

Figure 1.10 a) Schematic of growth mechanism for thermal AlO_x TB with high defects and pinholes resulting defective dielectric and b) J_c vs exposure (pressure* time) for JJs show less stepper slope for thickness > 0.5 nm and steeper slope at thickness < 0.5 nm indicative defective dielectric with low E_b. This figure is adapted from

Despite extensive effort with high TMR on MTJs with epitaxial MgO TB, they require a complex sample fabrication process and post annealing [53-55]. This post annealing has several disadvantages with recrystallization that occurs differently on different locations leading to a roughened FM/barrier interface with poor uniformity across the wafer, which makes scale-up and integration with CMOS difficult [56-60]. Figure 1.11(a) show that the high temperature annealing in range 350-500 ℃ results in the formation of grain boundaries (GBs) across TB. These GBs act like pinholes and defects increasing leakage current as in Figure 1.11(b) [61, 62], which reduces the figure-of-merit TMR. Thus, the current state of the art fabrication process remains a major challenge in the research and development of MTJs. The further reduction of TB to sub-*nm* requires an alternative method for fabrication of dielectric with atomic precision control and low defect density for future electronics.

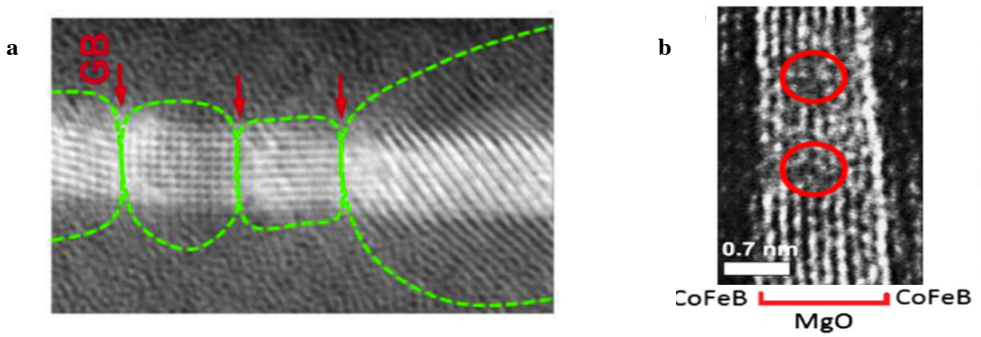

Figure 1.11 a) Formation of grain boundaries in epitaxial CoFeB/Mgo/COFeB as indicated by dashed lines where MgO grains are indicated by arrows. This figure is adapted from reference [61] and b) defects and pinholes as observed in MgO barrier due to high temperature post annealing. This figure is adapted from reference [62].

Among emerging technologies, spintronics offers the best candidates due to their engineering methods that intrinsically provide non-volatile magnetization states with zero standby power dissipation as well as potentially very high endurance making them ideal to construct memory devices. Highly functional spin-electronic devices such as spin transistors will be viable only after a better understanding of the mechanism of spin-polarized electron transport. This demands the fabrication of high quality MTJs with an ultrathin dielectric to improve the figure-of-merit for different devices. Atomic layer deposition (ALD) provides an alternative approach for the fabrication of ultrathin, uniform and leak free TBs for better device architecture and improving their performance.

1.8.2 Atomic Layer Deposition of Ultrathin Dielectric

The various deposition techniques such as magnetron sputtering, [17, 63, 64] MBE, [4, 9] and ALD [10, 13, 18, 64-66] have been the focus of recent research for different microelectronic applications. Among all, ALD is an interesting chemical vapor deposition process that relies on

well-defined chemical reactions. This reaction that occurs at the sample surface has several unique advantages [67, 68]. First, ALD is a chemical process that minimizes the formation of intermediate compounds and is important to reduce defects and impurities in the films. Second, ALD growth is self-limiting enabling atomic scale precision control of film thickness. Finally, ALD coating is highly conformal [69, 70], which is important to obtain pinhole and leak free ultrathin dielectric. Figure 1.12 shows the step-by-step growth of ALD Al_2O_3 dielectric films in the optimal case with no IL formation. First, the H_2O precursor is pulsed into the chamber to create a hydroxylated metal surface. A purge step follows after the H_2O reacts with the surface to remove excess molecules reacting with next chemical. Next, Al precursor tri-methyl aluminium (TMA) is pulsed into the chamber and purged after CH_4 is produced as a by-product. Lastly, H_2O is pulsed to produce single monolayer of Al_2O_3. Al_2O_3 thickness is controlled by varying the number of ALD cycles which consist of H_2O-purge-TMA-purge-H_2O. Each ALD cycle produces a single conformal monolayer with thickness well calibrated using ellipsometry to be 1.1-1.2 *Å*/cycle,[17, 18] which is consistent with the previous reports by other groups [68, 71, 72].

ALD offers several advantages with atomically smooth surfaces with a well-controlled chemical stoichiometric composition. ALD creates layers that is extremely conformal to match well with the wafer topography, with identical film thicknesses on device features. This high conformity is a critical capability for coating high-aspect-ratio and 3D architectures. ALD also plays a key role in self-aligned multiple patterning, which is used to form patterns smaller than those that can be produced with current lithography technology. ALD is well suited for process variability control

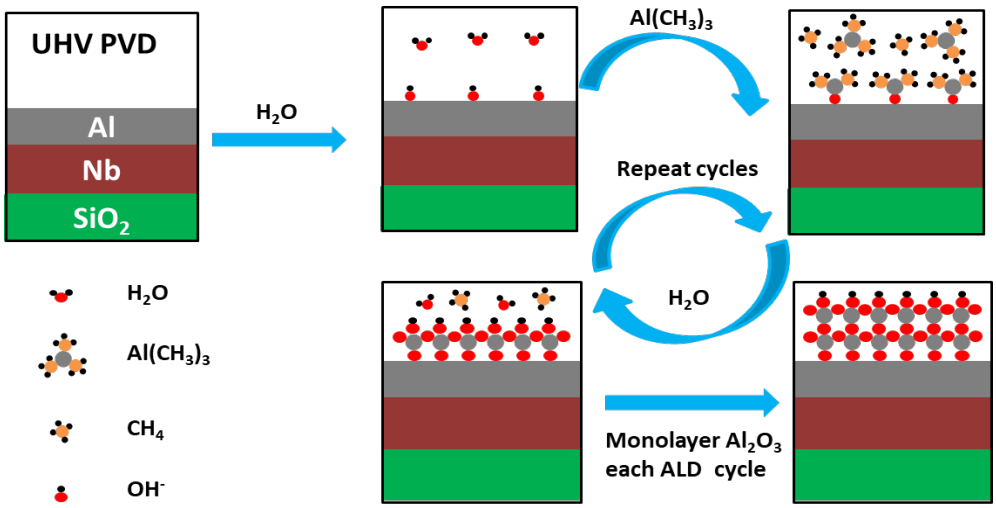

Figure 1.12 Step by step growth mechanism for ALD Al_2O_3 with optimal ALD parameters without an interfacial layer formation a) fabrication of thin film using ultra-high vacuum (UHV) using physical vapor deposition (PVD) b) exposure of H_2O c) exposure of tri-methyl aluminium (TMA) d) exposure of H_2O to complete one ALD-cycles producing monolayer of Al_2O_3 and e) each layer control by deposition of sequential exposure of chemical producing conformal, stoichiometric and low defects ALD dielectric.

and is used to form dielectric films on the sidewalls of memory holes. Metal ALD is also used for the lateral deposition that completely fills narrow, horizontal features. ALD is an excellent way of depositing thin gate sidewall spacers with extremely uniform thickness and no pinholes, which separates the control gate from the three-dimensional FinFETs structure. Its many advantages have led ALD to be used in several applications. The ALD process is capable of creating both dielectric and metal films, depending on the choice of precursors. ALD is also being explored as a means to improve overlay control, or precisely a new pattern to be aligned over an existing pattern. The use of ALD will continue to grow and play an increasingly important role in advancing semiconductor manufacturing for different applications. Proven as a key enabling technology, ALD continues to

evolve for use in challenging new structures and scaling strategies as they are integrated into next-generation devices.

1.8.2.1 *Ex-situ* ALD of Ultrathin Dielectric

Despite the exciting progress made in the fabrication of ALD dielectric thin films, such as Al_2O_3, HfO_2, ZrO_2, MgO, Al-doped ZnO,[10, 12, 13, 17, 18, 64, 68, 70, 73, 74] the dielectric properties of ultrathin insulating films in MIM structures are not optimal. Most probably due to the influence of the interfacial layer (IL) formation at the M-I interface [68, 75]. Al_2O_3 is a technologically important material due to its excellent dielectric properties, good adhesion to many surfaces, and thermal and chemical stability. These properties make Al_2O_3 attractive in the silicon microelectronics and thin film device industry as an insulator, ion barrier, and protective coating. Al_2O_3 is being considered as a high-*K* material to replace SiO_2 gate in microelectronic devices architectures such as MRAM, Dynamic Random-Access Memory (DRAM) and CMOS [26, 27]. Taking Al_2O_3 as an example, the initiation of ALD Al_2O_3 growth on metal typically requires a monolayer of hydroxyl groups formed controllably on a metal surface, which is by no means trivial. Metals are typically classified into two categories based on the nucleation for hydroxylation: noble (Au, Pt, Ir, and Ru) and reactive (Al, Nb, Fe, and Co). In the former case, the first 30-50 ALD cycles serve as the so-called incubation period since ALD growth cannot be initiated until the surface hydroxylation is complete [17, 75] . Unfortunately, this incubation period typically yields a defective M-I IL formation with the oxidation of the bottom electrode [17, 71, 76]. On the other hand, reactive metals are more sensitive to air exposure especially oxygen

exposure and other chemicals during the ALD process. A defective surface layer, which is several nanometres in thickness can form upon exposure of the reactive metal surface to air or even low vacuum [17, 64, 77]. This sensitivity means a defective IL at the M-I interface may form before the ultrathin ALD dielectric film growth. This IL can in turn cause defects in the ALD dielectric. The control over M-I interface is critical as the dielectric layer in TJs and CMOS made using *ex situ* processes have a ε_r significantly lower than the bulk single crystals values when the dielectric layer thickness is on the order of tens of nanometres or lower [11, 12, 71, 73, 74, 78-82]. Best reported results include an ε_r in the range of 7-8.5 for with ALD Al_2O_3 dielectric thickness > 40 *nm*, together with a leakage current density (J) ~ 10^{-10}-10^{-8} A/cm^2 [71, 78-81, 83, 84]. The considerable decrease in ε_r ~4 is observed as the Al_2O_3 dielectric thickness approach ultrathin thicknesses with corresponding increases in J ~10^{-7} A/cm^2 [71]. Indeed, a similar monotonic decrease of ε_r with a decrease in film thickness has been observed [11, 12, 71, 73, 82, 85]. This trend indicates that the presence of an M-I IL, which when connected in series with the dielectric film can significantly reduce ε_r and the reduction becomes more severe at smaller thicknesses. The primary challenge in the ALD growth of TBs of sub-nanometre thickness is the formation of an IL between the metal electrode and the dielectric ALD TB, typically formed when the metal surface is exposed to ambient or low vacuum in *ex situ* processes. This defective interface has a profound effect on the ALD dielectric film quality when dielectric thickness approaches the ultrathin regime.

1.8.2.2 Dielectric Properties of Ultrathin Dielectric

Table 1.2 compares ALD Al_2O_3 MIM capacitors with the thickness of dielectric in the range of few tens of *nm* to few hundreds of *nm* with their corresponding parameters like ε_r, J and breakdown field. We can observe that even for hundreds of *nm* thick dielectric film ε_r is in range ~7-7.5, which is 22.2-16.6 % lower compared to bulk single crystal ε_r ~9.2. The decrease in ε_r with decrease in the film thickness is attributed to the presence of defective IL in series with ALD Al_2O_3 dielectric. This leads to an increase in J and lower dielectric breakdown fields (E) ~ 5-8 MV/cm even for thicker dielectric film thickness.

Table 1.2 Recent progress in dielectric property of ALD Al_2O_3 dielectric MIM capacitors with thickness of dielectric in range from few tens of *nm* to few hundreds of *nm* with their corresponding parameters.

Al_2O_3 thickness(*nm*)	Growth temperature	Dielectric constant (ε_r)	Leakage current density (A/cm^2)	Breakdown field (MV/cm)	References
40	450	7	-	6-8	[86]
> 100	150	7.1	6 e-10	6-7	[87]
107	250	~7	1 e-8	7-8	[81]
101	350	~7	1 e-8	7-8	
59-115	150-300	7.5 (5)	5.3 (2)		[88]
115	177	7.5	1 e-10	5.3	[71]
57	177	7.7	2 e-10	5.3	
12	350	5.9	2 e-9	5.3	

Figure 1.13 shows the systematic study on thickness dependence of ε_r for Al_2O_3 MIM capacitor deposited on n-Si(100) and Mo-coated Si(100) [71]. There is similar monotonic decreasing trends in ε_r with a decrease in the dielectric film thickness with ε_r ~8, which is 11.1 % lower than bulk ε_r ~9.2 [71]. This significance effect of IL observed when dielectric thickness reaches ultrathin thickness is primarily due to the presence of defective oxide dominating over the ALD film resulting in an increase in leakage current which are not suitable for applications that requires high quality dielectric films.

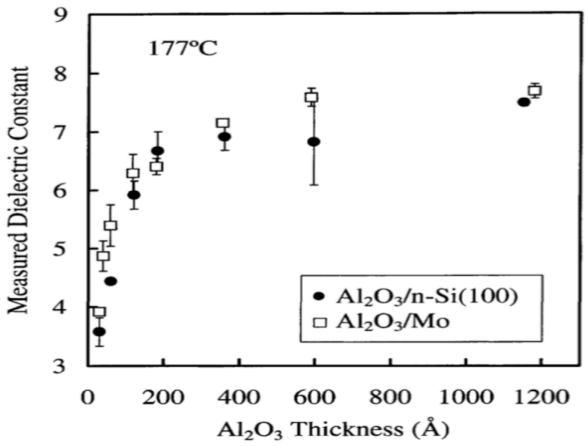

Figure 1.13 Measured dielectric constant for Al_2O_3 ALD films of different thicknesses grown at 177 °C on n-Si(1 0 0) and Mo-coated Si(1 0 0) . This figure is adapted from reference [71].

1.9 Critical Issues to Be Addressed

The *ex situ* fabrication process itself is the bottleneck for obtaining high quality dielectric due to the exposure of fresh metal surface to atmosphere leading to the formation of defective oxides IL resulting defective dielectric growth on the top. However, only *in situ* fabrication is not enough to

reduce the formation of IL to negligible. Several critical issues need to be resolved to obtain high quality dielectric growth [14, 15, 89, 90]. The pre-ALD IL formation on the metal surface is critically important which is primarily due to the formation of defective oxides resulting in defective dielectric growth. Even in the *in situ* ALD process, a prolonged exposure to vacuum (even at a high vacuum of ~10^{-7} Torr) during heating of a metal electrode for ALD TB growth can cause the formation of such an interface [25]. This interface is even more detrimental to ALD TBs for MTJs since the additional defects can impair spin current tunnelling current in MTJs [24-26]. This dissertation addresses the critical issues of controlling the M-I interface to obtain ultrathin dielectric suitable for gate dielectric in CMOS and potential MTJs application for non-volatile MRAM. Chapter 2 discuss the experimental design and details of fabrication and characterization of devices. Chapter 3 presents the optimization of dielectric properties of Al/ALD Al_2O_3/Al MIM architecture. Chapter 4 discusses the effect of ALD Al_2O_3 seed layer in controlling M-I interface for the MgO dielectric. Finally, Chapter 5 presents the on/off of negative capacitance in ultrathin ferroelectric/dielectric capacitors. Finally, chapter 6 discusses the preliminary results obtained on the fabrication and characterization of MTJs using ultrathin ALD Al_2O_3 tunnel barriers for application in non-volatile memory applications. Chapter 7 discusses about overall conclusion and future prospective for ALD fabricated MIM architecture for microelectronics and memory devices.

Chapter 2 Experimental

This chapter describes the relevant experimental procedure used throughout this dissertation. The first section introduces unique *in situ* ALD-PVD systems for the fabrication of MIM architecture. Other sections discuss the relevant details of experimental procedure related to MIM capacitors and MTJs along with their optimization procedure. Finally, the device characterization techniques with details of hardware and procedure will be discussed.

2.1 Fabrication of MIM Architecture

Figure 2.1 shows a schematic diagram of in-house integrated all *in situ* ultra-high vacuum (UHV) physical vapor deposition (PVD), ALD and STS measurement system. The load lock chamber is used for loading and unloading the samples. It is separated from the UHV chamber by a gate valve. This chamber also contains a stage for plasma treatment for surface treatments and cleaning. The PVD deposition chambers (*i.e.* MTJ and JJ) are separated by the gate valves maintained at UHV by two separate turbo pumps (Leybold) for deposition of metals like Nb, Al for JJs; and magnetic materials like Fe, CoFeB, and an antiferromagnetic IrMn for MTJs. The viscous ALD chamber is maintained at low vacuum using a mechanical pump. It's temperature is maintained by a heating tape and wrapped around with heating rope to its exterior for heating to the desired temperature. The ALD chamber is used for the deposition of ultrathin dielectrics like Al_2O_3, MgO, HfO_2 etc and is isolated from the other chambers by two gate valves to ensure a proper flow from the ALD sources. The two magnetically coupled transport rod allow *in situ* transfer of sample from one chamber to another under UHV. This unique all in situ integrated PVD-ALD transfer system

allows the fabrication of high quality ultrathin dielectrics for MIM and TJ applications. Another transfer arm allows the transfer of samples onto STS chamber (RHK) for characterization of the barrier height along with atomic force microscopy (AFM) for surface morphology respectively. Figure 2.2 shows a photograph of all *in situ* PVD-ALD-STS chambers with each chamber are labelled as indicated. The detailed description of the design and transfer procedure is presented in an earlier thesis work by *Alan Elliot* [90] and *Jamie Wilt* [89].

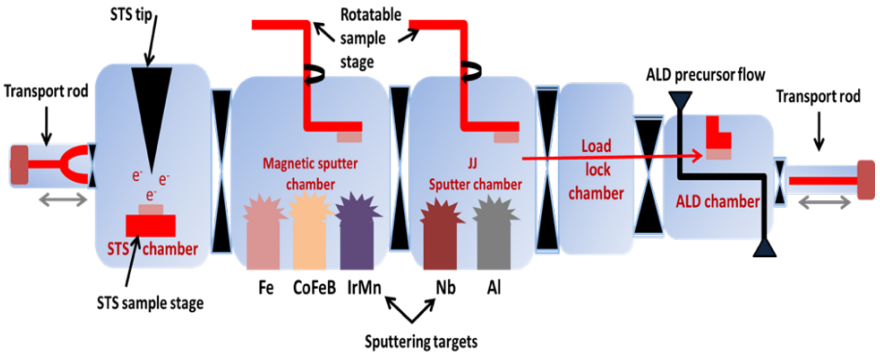

Figure 2.1 Schematic of all *in situ* in-house integrated ALD-PVD-STS UHV system with load lock, ALD chamber, Josephson junction sputter chamber, Magnetic sputter chamber and STS characterization chamber.

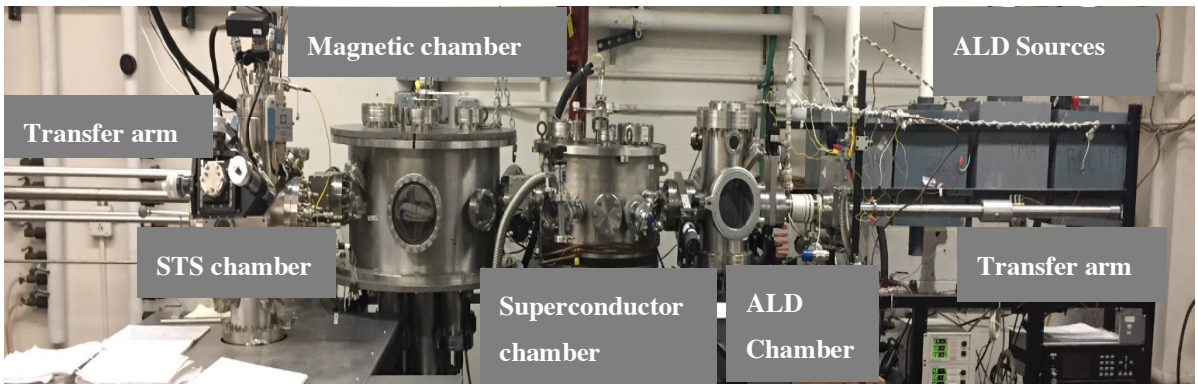

Figure 2.2 Photograph of all in situ in-house integrated ALD-PVD-STS along with each chamber label as indicated for fabrication and characterization of multi-layered MIM and TJs devices.

2.2 Fabrication of Devices

PVD method for metal deposition and ALD method for the ultrathin dielectric were used for fabrication of the capacitors and TJ devices. The *in situ* process for the fabrication of MIM capacitors and MTJ devices allows the transfer of samples and their characterization by minimizing IL formation between M-I interface. The IL is impossible to minimize with *ex situ* deposition process because the metal electrodes oxidize when exposed to air before the growth of the dielectric film. Our current design is versatile, unique and critical as *in situ* integration allows for the fabrication of ultrathin ALD dielectrics without the formation of IL or native oxides on metal electrodes for multi-functional MIM and TJ.

2.2.1 Capacitors

Figure 2.3 shows a schematic of the MIM architecture for a MIM capacitor fabricated using the shadow mask process. First of all, bilayer devices with Nb (20 *nm*)/Al (7 *nm*) were *in situ* fabricated using UHV PVD-ALD system. Nb and Al were DC magnetron sputtered onto a Si/SiO_2 substrate with a deposition rate of 1.7 and 0.5 *nm*/s respectively at base pressure better than 10^{-7} Torr using a shadow mask. After sputtering, the samples were transferred *in situ* under high vacuum to the ALD chamber and dynamically heated for a set period of time before the deposition of ALD TBs [15]. Following this dynamic heating, 40-10 cycles ALD Al_2O_3 were deposited with a 5 SCCM N_2 carrier gas for the TB deposition. The ALD growth of Al_2O_3 occurs with alternating pulses of H_2O and TMA via a ligand exchange at the heated sample surface. The two precursors steps are separated by a purge of an inert carrier gas N_2 [68], to ensure the formation of a single

monolayer of amorphous Al_2O_3 with a deposition rate of ~1.1 Å/per cycle [17, 18]. Then, the top electrode was deposited using another shadow mask to define different capacitor areas with 200x200, 200x300 and 200x400 μm^2 [16]. The inset shows the cross-section of MIM architecture deposited to obtain optimal performances of MIM capacitors. The control of the thickness of the Al wetting layer is found to be critically important in tuning the properties of ALD Al_2O_3 with and without IL especially in the case of material sensitive for the oxidation like Fe. Using an Al wetting layer in the Fe/Al/ALD Al_2O_3 (2.2 *nm*)/Fe capacitors, we show a transition from a DE only capacitor for Al thicknesses greater than 1.0 *nm* to an ferroelectric/dielectric (FE/DE) bilayer capacitor at smaller Al thickness to promote the formation of ultrathin FeO_x IL of thickness below 2 *nm* at the Fe and ALD Al_2O_3 interface. This trend can be attributed to the formation of a native oxide IL at the Fe/ALD Al_2O_3 interface when the Al wetting layer is very thin or absent. This method provides an easy way to fabricate different bilayer stacks by tuning the thickness of Al wetting layer thickness in a multi-layered structure.

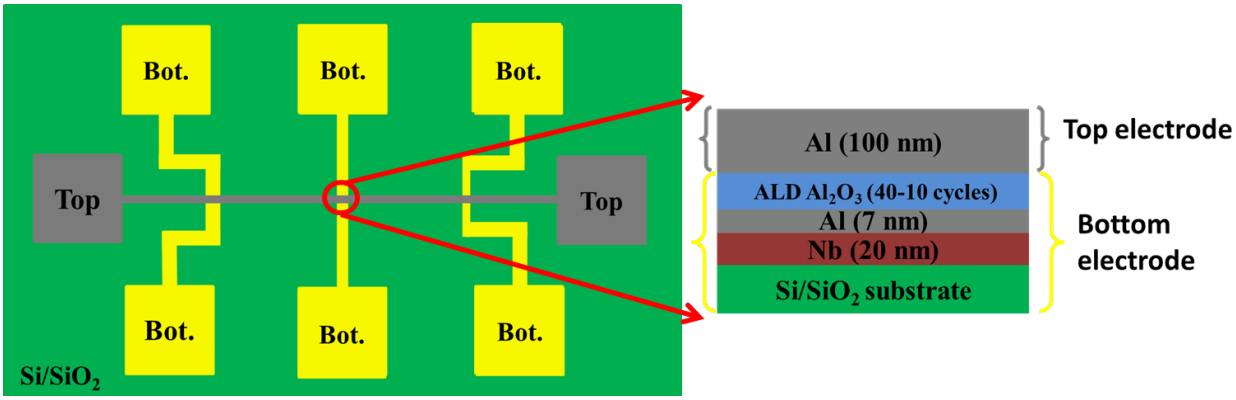

Figure 2.3 (Left) Schematic diagram (viewed from above) of the bottom electrode (yellow) with a shadow mask used to define the 400, 300 and 200 μm wide bridges and the top electrode (brown) with a 200 μm wide bridge to define the corresponding MIM capacitors.

2.2.2 Magnetic Tunnel Junctions

Thin magnetic films like Fe and CoFeB were deposited using DC magnetron sputtering onto a Si/SiO_2 substrate at base pressure less than 10^{-7} Torr. Several test runs were performed to optimize the properties of the magnetic thin film. The optimal condition was obtained at Ar pressure ~4 mTorr, a power of 200 W and, the distance between sputtering gun and sample fixed at 6 cm, with a deposition rate of 1.0 nm/s. Then, a simple spin-valve structure was used for the fabrication of MTJs based on the magnetic hysteresis (M-H) loop measurement. The thickness of the FM layers is key for obtaining different coercive field allowing the observation of both anti-parallel (R_{AP}) and parallel (R_P) configuration, which can be achieved using an external magnetic field. Based on the M-H loop of the Fe thin film, the thicknesses of the fixed and free layers were chosen as 50 and 5 *nm* respectively. The multi layered structure consisting of Nb, Fe and Al layers with the Al wetting layer from 7-1 *nm*. After sputtering, these samples were *in situ* transferred under high vacuum to the ALD chamber [15] for deposition of 5-10 cycles of ALD Al_2O_3. Figure 2.4(a) shows the MTJs structure with the Al wetting layer as Nb (50 *nm*)/Fe (50 *nm*)/Al (1 *nm*)/ALD Al_2O_3 / Fe (5 *nm*)/Nb (50 *nm*). After several optimizations, the Nb layer was used as a seed layer and capping layer for preventing the oxidation of Fe, since Fe oxidizes aggressively in the presence of an oxygen atmosphere. In the extreme limit, MTJs device with no wetting layer *i.e* without the Al wetting layer is obtained as Nb (50 *nm*)/Fe (50 *nm*)/ALD Al_2O_3 / Fe (5 *nm*)/Nb (50 *nm*) as shown in Figure 2.4(b). Thus, MTJs devices with and without the Al wetting layer were fabricated using *in situ* UHV PVD-ALD system.

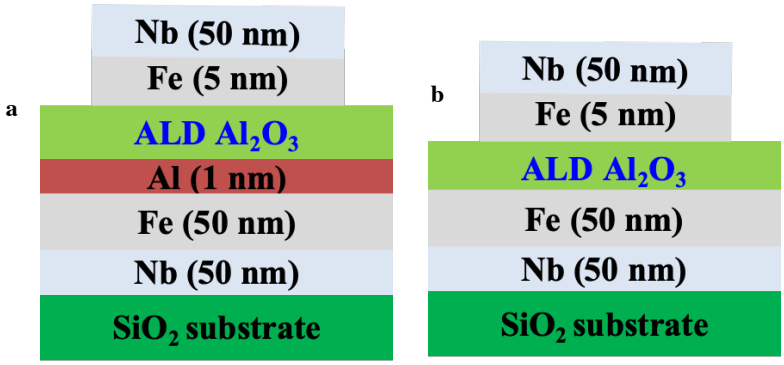

Figure 2.4 Schematic for magnetic tunnel junction device structure a) Nb (50 nm)/Fe (50 nm)/Al (1 nm)/ALD Al_2O_3 / Fe (5 nm)/Nb (50 nm) with Al wetting layer and b) Nb (50 nm)/Fe (50 nm)/ALD Al_2O_3 / Fe (5 nm)/Nb (50 nm) without Al wetting layer.

Figure 2.5(a) shows a multilayered MTJ device without the Al wetting layer deposited using PVD-ALD system. This was processed into the MTJ devices structure, which is patterned into several devices using a standard photolithography (PL) process and the process flow shown in Figure 2.5. The main wiring of the MTJ was defined using the PL process (Figure 2.5b). An ion milling is used to etch the entire multilayer stack (Figure 2.5c). The PL photoresist mask is then removed and electron beam lithography (EBL) is used to define the MTJ mesa (Figure 2.5d) followed by an ion milling for mesa structure (Figure 2.5e). Then, the MTJ mesa is isolated using SiO_2 evaporation, which is then lifted off (Figure 2.5f). A second EBL is used to define the top wiring for the MTJ and followed up with plasma cleaning for a clean surface before the Nb sputter and lift off to complete the device structure (Figure 2.5g-i).

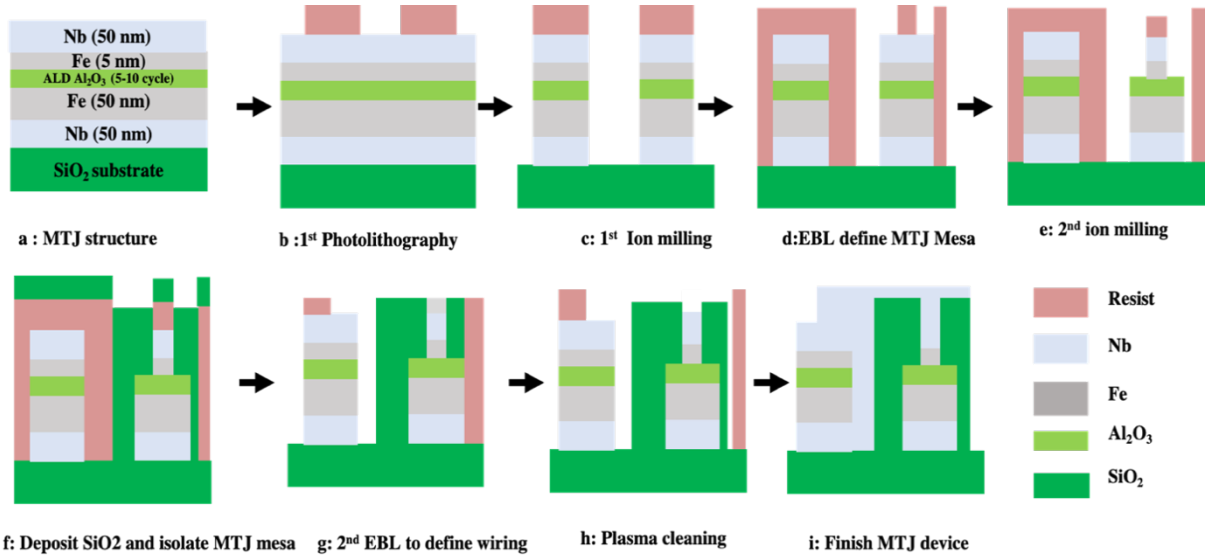

Figure 2.5 Schematic flow chart of Magnetic tunnel junction fabrication with different steps of fabrication process.

The micrographs and profilometry of the devices during each process flow are critical steps for optimization and better performance of the finished devices. Figure 2.6(a) shows a micrograph of the main wiring after the 1st ion milling resulting in the total step height measurement ~160 *nm*. Figure 2.6(b) shows 3D-profilometry after SiO_2 evaporation showing all devices have EBL resist removed a with step height of SiO_2 ~300 *nm* as shown in Figure 2.6(c). The final device after the 2nd EBL, the 2nd ion milling and top Nb electrode deposition is shown in Figure 2.6(d), which is finished and device ready for four probe I-V and TMR measurement after wire bonding with the contact pads.

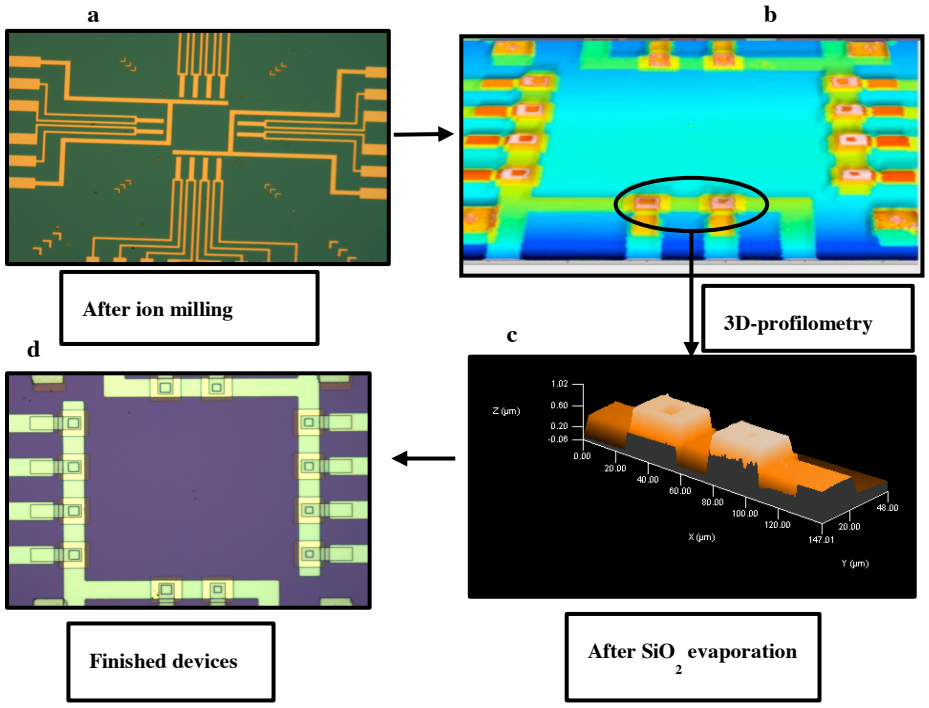

Figure 2.6 Real micrograph of devices after different steps of fabrication process a) micrograph of main wiring after 1st ion milling b) 3D-profilometry after sio2 evaporation c) Step height measurement with Sio2 evaporation and d) Micrograph of finished devices.

Figure 2.7(a) shows the photolithography process used to define the wiring of the MTJ circuit using a photomask. Each MTJ has a pair of smaller pads associated with I+ and V+ terminals and the larger pads serve as I- and V- shared among 6 junctions. The trilayers have dimensions of 2.5 x 2.5 cm, enough to fit six patterns were spin-coated with S1813 photoresist (Shipley) at 4000 rpm for a resist thickness of 1.75 µm. The resist was baked at 90 °C for six minutes before exposure to a 500 W UV lamp for 90 sec. The samples were then developed in a 1:3 solution of M351 microposit developer and water for 100 sec, and then rinsed in deionized water and blown dry with N2. Each device in the photomask was designed for a four-probe measurement of 12 junctions of

size 10, 7 and 5 μm to check the uniformity of devices. Figure 2.7(b) shows a photograph of a homemade probe designed to minimize the noise and wire bonding of the MTJ chip to the sample stage stage. Figure 2.7(c) shows the schematic of the physical property measurement system (PPMS) stage, wiring connector and sample stage ready for the for TMR measurement. The MTJs samples were current biased with the function generator (Agilent 33120 A) and temperature and magnetic field were set using automated PPMS (Quantum Design Evercool II system).

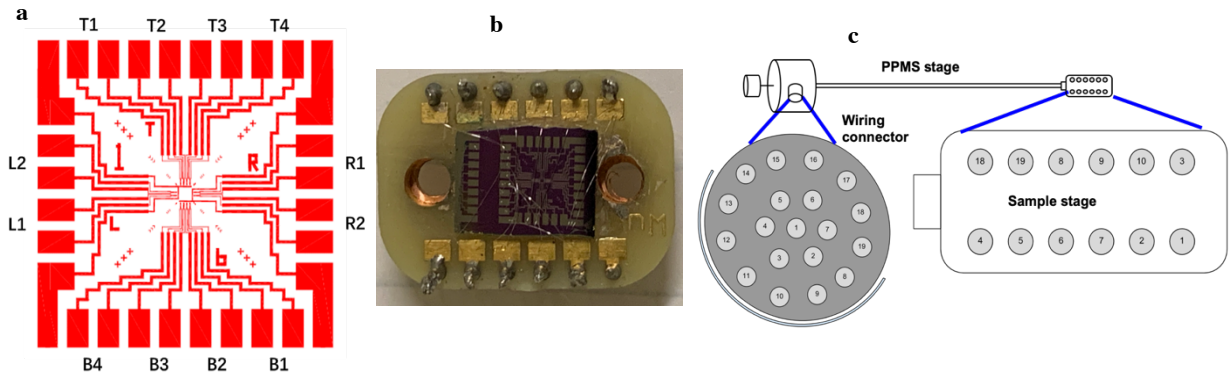

Figure 2.7 a) Schematic of photomask used to define MTJ circuit with each MTJ has pair of electrode and ground electrode shared among 6 MTJs for four probe measurement b) photograph of MTJ chip wire bonded to sample stage and c) Schematic showing PPMS stage, sample stage and wiring connector for TMR measurement.

The patterned sample using PL was attached to the sample stage using Ag paste after drying for about 15 min with a lamp. After that, the chamber was pumped with a turbo molecular pump to base pressure of below $5x10^{-6}$ Torr to avoid any contamination and chemicals. The key advantage of ion milling is anisotropy and non-selectivity, which was used to etch through the multi-layered structure. The optimal condition for ion milling was obtained at the ion beam voltage of 400 V with a corresponding beam current of 40 mA. Liquid N_2 cooling was used to prevent the

overheating of samples during ion milling. The milling rate for metals and insulator were well calibrated in a dummy sample of Nb, Fe, and Al_2O_3 with 11, 10 and 0.5 *nm* per minute respectively. To confirm etching of multi-layered structure, the samples were over milled ~5-7 % and multiple checks with optical image and profiler were performed during different stages of sample fabrication to make sure there were no shorts present. The first ion milling is easy to perform, after etching the underlying SiO_2 was revealed as in Figure 2.5(c). For etching through top metals during Figure 2.5(e) show 2nd ion milling the milling rate must be well controlled. The heating time was found to be crucial because overheating of EBL resist during ion milling makes resist harder and difficult to remove after SiO_2 evaporation. After several tests and optimization, liquid N_2 cooling was found to be efficient in preventing the overheating of EBL resist. The ion milling was then used to define lateral dimensions ranging from 5 – 10 μm as in Figure 2.5(d) called the MTJ mesa. The high performance positive electron beam resist (ZEP520A Zeon Chemicals) was spin coated onto the samples at 1000 rpm for a thickness of ~ 1 μm. The resist was then exposed to an electron beam and developed to reveal the pattern used as a mask for 2nd ion milling to define the MTJ mesa Figure 2.5(g). After the definition of the mesa, SiO_2 was evaporated onto the sample mounted to a water-cooled stage at operating pressures ~10^{-6} Torr. This was done to electrically insulate the MTJ mesa. The deposition rate ~ 5 *nm*/sec was monitored *in situ* with a quartz crystal monitor. To ensure a consistent deposition rate and high film quality, fresh SiO_2 was ground into a powder before each deposition and placed into the evaporator's crucible. After the evaporation was complete, the sample was brought to RT gradually over the course of 30 minutes, after which it was removed from the evaporation chamber. Lift off was then performed on the sample to

remove excess SiO_2 using the same EBL mask and diethylacetamide (ZDMAC), which strips ZEP520A for about an hour. Finally, the sample was suspended in solution and ultrasonicated for 60 seconds.

After the insulation of MTJ mesa, the top must be electrically connected to the wiring leads defined by photolithography using a second round of EBL to define the area of the top wiring, shown in Figure 2.5(g). During the device processing steps, the top Nb film was exposed to air and chemicals, producing native NbO_x on the surface. This was removed using a plasma cleaning procedure performed using an RF power supply in a load lock chamber before the deposition of the top Nb electrode as in Figure 2.5(h). The previously used optimized plasma cleaning condition for JJs with 80W RF plasma power ignited at 30 mTorr Ar, with the sample placed at 2 cm away and cleaned for 2 minutes from the top electrode. Then, sample was transferred into the sputtering chamber for the deposition of 300 *nm* and the device was finally finished after lift-off. However, this condition resulted in non-uniform resistance area (RA) across the junction. This may have been because the NbO_x was still left on the surface. To optimize the plasma cleaning process the method of sheet resistance ($R_{\square}$) was used. The resistance for each resistor in the MTJ circuit defined using photomask and top contact shown in Figure 2.14 is calculated using the equation as

$$R = \rho\, L/A = \rho/t * \sum \frac{L_i}{W_i} = R_{\square} * \sum \frac{L_i}{W_i}, \qquad (7)$$

where $\sum \frac{L_i}{W_i}$ is the sum of ratio of $\frac{L_i}{W_i}$, L_i *and* W_i are lengths and widths of resistors in series for each different path, $R_{\square}$ is sheet resistance.

The optimization of distance from stage to plate was done by fixing the power at 80W RF. The optimal distance was found to be 18.20 mm. Different powers 120 W and 80 W with different times, 2, 4 and 6 minutes were tested for the optimization. To confirm that plasma cleaning was optimal the measurement of contact resistance (R_C) was done for the Nb electrode using EBL to define the contact between top and bottom Nb electrode. R_C for 12 devices measured on a chip using different plasma cleaning condition were compared. Based on the comparison of$R_{\square}$, all devices with 120 W power for 2 minutes plasma cleaning at 30 mTorr Ar show uniform $R_{\square}$ in range 2.33-2.09 Ω/square within 15% variation showing best results. Thus, only 2 minutes of plasma cleaning at a higher power of 120 W was sufficient to remove NbO_x on the top of the Nb film. The sample was then *in situ* transferred to the JJ chamber for deposition of the top 300 *nm* of the Nb electrode that connects the bottom contact pads to the top of the junction allowing current to pass through the junction of 25-100 μm^2 cross sectional area Figure 2.12 (i).

2.3 Characterization

2.3.1 Vibrating Sample Magnetometer

The Vibrating Sample Magnetometer (VSM) utilizes the principle that, if the magnetic field or flux that is enclosed by a coil changes, a voltage will arise across the terminals of that coil. The magnetic sample is placed in the middle of a set of pickup coils and vibrates at a frequency of 75 Hz in the vicinity of a set of the pickup coils creating a change in flux. This flux is proportional to the magnetic moment which is measured in emu and displayed as a function of the magnetic field (H). An electromagnet surrounds the sample and pickup coils, which is used for varying the field

to which the sample is exposed so that the magnetization (M) in emu/cc can be measured as a function of the H. The VSM's operating software, EasyVSM can extract many different magnetic parameters to characterize a wide variety of magnetic samples of both high and low coercivity. Figure 2.8 shows the M-H hysteresis loop measurement performed using VSM on a Fe (50 *nm*) thin film structure showing high saturation magnetization confirming excellent magnetic property.

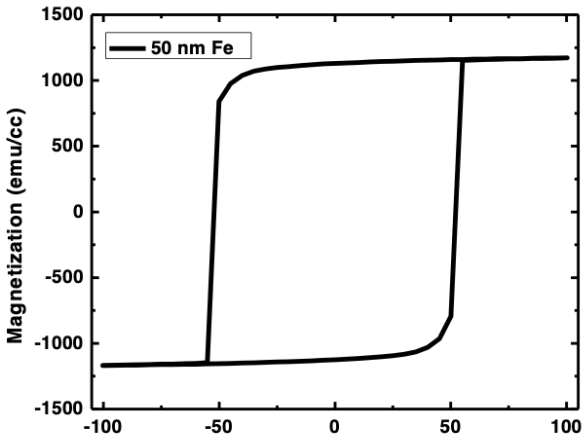

Figure 2.8 Magnetization (in emu/cc) vs magnetic field (in Oe) (M-H) hysteresis loop for Fe (50 nm) characterized using vibrating sample magnetometer

2.3.2 Atomic Force Microscopy

Figure 2.9(a) shows a schematic of an atomic force microscope (AFM) consist of a sharp tip (<1 *nm*) mounted onto a silicon or silicon-Nitride cantilever. A laser reflects off the top surface of the cantilever and onto a quad-photodiode. Piezoelectric elements scan the tip across the sample surface. As the tip deflects off surface features, the laser position onto the quad-photodiode changes slightly. By measuring the photocurrent in the photodiodes, angstrom level precision in the tip position can be achieved using both contact and tapping or non-contact modes as shown in Figure 2.9(b). However, thermal noise inherent in this flexible cantilever induces vibrations that

reduce the maximum resolution of surface features. The main drawback of AFM as compared to other instruments is that it's slow scanning speed. To increase imaging speed and improve resolution, a feedback loop is used to allow the cantilever to quickly confirm to surface features. The control over surface roughness is critical for the fabrication of ultrathin and uniform ALD TB for MTJs application. AFM, WiTec Alpha 300 in contact mode and RHK-HV *in situ* non-contact AFM were used to characterize topography of the samples and surface roughness was calculated using root-mean square average of roughness within in the scan area.

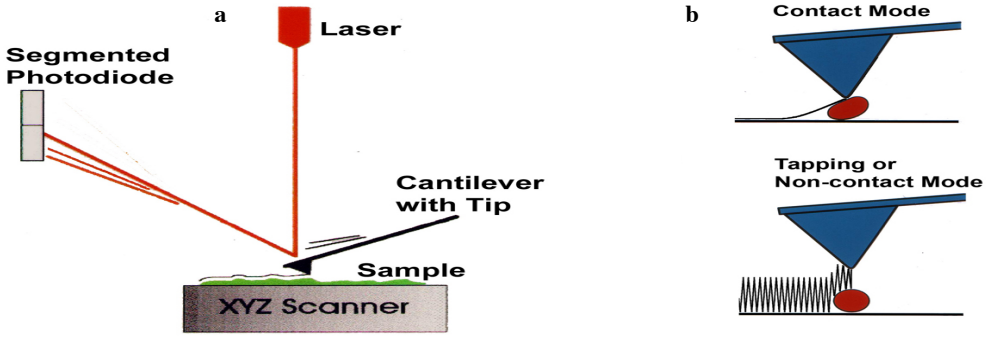

Figure 2.9 a) Schematic of atomic force microscopy (AFM) for surface morphology study b) contact and tapping or non-contact AFM modes

2.3.3 *Ex-situ* C-V Measurement

The dielectric properties of MIM structures with ultrathin ALD Al_2O_3 in thickness range 4.4-1.1 *nm* were characterized using a B1500A Semiconductor Device Analyzer, which supports single pass capacitance-voltage (CV) and leakage current-voltage (IV) measurements within the same mainframe using a new, single-slot multifrequency capacitance measurement unit (MFCMU) and two Source/Measure Units (SMUs). However, performing both IV and CV measurements on a

single probe station is not easy. SMU-based IV use triaxial connectors, while CMU-based CV measurements use Bayonet Neill–Concelman connectors. The capacitance is measured by superimposing small ac signal on an applied dc gate voltage. The ac signal is necessary for the capacitance measurement while the dc voltage determines the bias condition. The measured capacitance is a function of applied dc voltage. During CV and IV measurement the tungsten probe scratches through the top few nanometres of the ALD Al_2O_3 layer to make an ohmic contact with the bottom electrode. Thus, the measurement can be performed between top and bottom electrodes to define $Al/Al_2O_3/Al$ trilayer capacitors with a defined capacitor area.

The working principle of the B1500A's MFCMU is based on the auto balancing bridge using four terminal pair extension test cable. The CV meter consists of (1) AC signal source (V_x) with the DC bias source in the high terminal, (2) current (I_x) flowing through the DUT, and (3) low terminal vector current meter. The high current terminal applies the AC measurement signal and the DC bias voltage to the DUT, and the high potential terminal senses the actual AC signal applied to the DUT. The low current terminal sinks the DUT current through the reference resistor (R_r) and keeps the low terminal potential as close as possible to zero volts (called as virtual ground). This is done using a negative feedback loop consisting of the high gain amplifier with (V_r) in the low current terminal and the feedback resistor R_r. The current flowing through the DUT (I_x) is obtained as V_r/R_r, and the DUT impedance (Z_x) is obtained as $Z_x = V_x / I_x = R_r (V_x/V_r)$. Based on the information about impedance and current through DUT the response of electrical component is calculated. The total capacitance is given by expression $C = \frac{\Delta Q}{\Delta V} = I_X . \frac{\Delta T}{\Delta V}$ where $\frac{\Delta V}{\Delta T}$ is the scan rate, ΔQ is the total

charges, and I_X is the current through the DUT. Thus, open, shut and phase compensation must always be performed before making the measurement. Phase compensation improves the bridge balancing stability at high frequencies and minimizes the phase shift effects due to frequency and cable length.

2.3.4 Four Probe I-V Measurement

IV measurements were taken at RT using a four-probe measurement configuration for initial check in quality control and analysis of uniformity of devices. The 25 μm diameter tungsten probes were connected to four channels of a semiconductor device analyzer (Agilent B1500A). This homemade chamber is equipped with linear motion controls with micrometer precision that allows probes to move from pad to pad inside to measure the junction resistance. The MTJs were current biased from 0 – 100 μA, and the voltage developed was measured. From the slope of I-V, the RT resistances were calculated. For junctions of different sizes, the product of the resistance and the area should be constant across the wafer, and the resistance itself should be inversely proportional to the area of the junction.

2.3.5 TMR Measurement in PPMS System

The TMR measurement on MTJ samples was done using PPMS which can vary temperature from RT to 4 K and H from 0 up to 9 T. MTJ samples were glued with silver paste in a Cu sample stage and dried in air for about 30 minutes. After that, each top and bottom pad were wire bonded using an Al wire bonder. Finally, MTJs with a four probe I-V measurement performed at RT were loaded in PPMS for TMR measurement. Figure 2.10 shows a plot of TMR in % obtained using equation

vs magnetic field in Oe for both R_P and R_{AP} configurations. An initial, H of 1500 Oe is applied where the orientation of both free and fixed layer magnetization is parallel as indicated by R_{P1} (inset 1). Then, H is switched to negative value until the free layer magnetization is switched resulting in R_{AP1} (inset 2). The negative magnetic field is increased until both layers of magnetizations are parallel as indicated by R_{P2} (inset 3). Finally, H is switched to positive value and increased until the free layer magnetization is switched as indicated by R_{AP2} (inset 4). The applied magnetic field is further increased to get magnetization of both layers parallel as indicated by R_{P1} original (inset 5). The efficient switching of free layers for these MTJ devices was possible by the application of an external applied H.

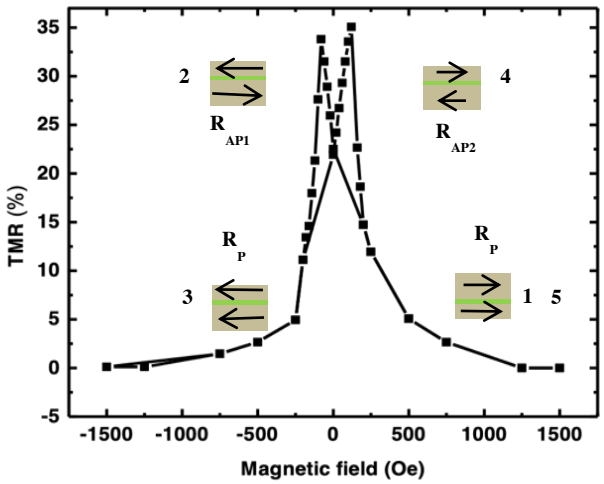

Figure 2.10 TMR measurement procedure for magnetic tunnel junctions using physical property measurement system

2.3.6 *In situ* STS Characterization

For the STS studies Al/Al_2O_3 bilayers (without top Al electrode) in thickness range 0.11-1.10 *nm* were transferred *in situ* by Jamie Wilt *et al* [89] for characterization of TB height. The STS chamber was maintained at a pressure of about 2×10^{-10} Torr. A mechanically cleaved Pt-Ir tip was used for all STS studies at RT. The constant height I-V and dI/dV spectroscopy were taken simultaneously using a lock-in amplifier with a voltage modulation of 100 mV at 1 KHz. The TB height was used to estimate the barrier height by the intersection of the conduction band minimum (CBM) and valence band maximum (VBM) using similar two bisquare-method linear fits to ln(*dI/dV*) [91]. One line fits the band gap regime, and the other the CBM and VBM. This ln(*dI/dV*) linear fit method was chosen over I-V or *(dI/dV)/(I/V)* fit methods for its insensitivity to high noise in the STS spectra [8, 92]. To examine the dielectric breakdown of the Al_2O_3 TB, the STS tip was held fixed at each scanned location and the bias was sequentially ramped up and down 20 times. Detailed studies on the dielectric properties of $Al/Al_2O_3/Al$ MIM structure will be discussed in the next chapter.

Chapter 3 Probing Effect of Interface on Dielectric Properties of Ultrathin $Al/Al_2O_3/Al$ Trilayers

Following empirical Moore's law, miniaturization of microelectronic devices has been the main driving force behind the advancement in semiconductor industry and justifies an increasing demand for more densely integrated devices [2, 19, 93, 94]. One of the direct consequences of this demands the need for a continuous reduction of the gate dielectric thickness. Unfortunately, for SiO_2 gates approaching ultrathin thickness range of 2-4 *nm*, have considerably increased *J* to 1-10 A/cm^2 [3, 24]. This occurs primarily due to the difficulties in controlling the defects in ultrathin SiO_2 [3]. This not only prevents the achievement of the required gate voltages for device operation but also exceeds the required threshold of $\sim 10^{-3}$ A/cm^2 for high-performance, low-power consumption microprocessors by several orders of magnitude. The difficulties in down-scaling the SiO_2 dielectric gates have motivated an intensive research on high-*K* dielectric materials [24, 25]. With considerably higher dielectric constants (ε_{Hik}) considerably higher than that of SiO_2 ($\varepsilon_r \sim 3.9$), the high-K dielectric can reduce the *J* by using a larger thickness t_{HiK} [26-28].

Though Al_2O_3 is not a high-*K* material, it is being considered as technologically important material due to its excellent dielectric properties, good adhesion to many surfaces, and thermal and chemical stability to replace SiO_2 in microelectronic devices architectures such as MRAM, Dynamic Random-Access Memory (DRAM) and CMOS [26, 27]. These properties make Al_2O_3 attractive in the silicon microelectronics and thin film device industry as an insulator, ion barrier, and protective coating. However, in most previous studies with Al_2O_3 dielectric layer MIM devices made using

ex situ processes have significantly lower ε_r than the bulk single crystals values even when the dielectric layer thickness is on the order of tens of nanometres [11, 12, 71, 73, 74, 78-82]. This trend indicates the presence of a M-I IL, which when connected in series with the dielectric film can significantly reduce ε_r and this reduction becomes more severe at smaller thicknesses. Indeed, a monotonic decrease of ε_r with decreasing dielectric film thickness has been observed when the dielectric film thickness falls into the ultrathin regime [11, 12, 71, 73, 82, 85]. The best-reported ε_r is in the range of 7.0-8.5 for ALD Al_2O_3 films with thickness exceeding 40 *nm*, together with a significant J in the range of 10^{-10}-10^{-8} A/cm^2 [71, 78-81, 83, 84]. The ε_r decreases monotonically with further decrease in ALD Al_2O_3 film thickness [71, 82, 85]. Groner *et al* reported ε_r ~7.7 for a 60 *nm* thick ALD Al_2O_3 film, which decreases to ~5.9 and 4 at 12 *nm* and 3 *nm* ALD Al_2O_3 film thicknesses respectively [71]. J increases to a high value ~10^{-7} A/cm^2 as the Al_2O_3 dielectric thickness approach ultrathin thickness range approximately 6.5 *nm* [83] and 3 *nm* [71]. A similar trend has also been observed in high-K dielectric films. For example, ε_r in the range of 8-20 were found for ultrathin HfO_2 films of thicknesses range 1-4.5 *nm*, which is considerably lower than the bulk value of 25 [11, 12, 73]. Overall, the IL can strongly degrade the dielectric properties of the MIM structure preventing the high quality insulator from being achieved in ultrathin film thickness range.

To address this critical issue, this chapter explores the effect of controlling M-I interface during pre-ALD exposure of the metal surface [14, 15] to minimize the formation of IL and its impact on the quality of ultrathin ALD Al_2O_3 dielectric thicknesses 1.1 – 4.4 *nm* (or 10 -40 cycles) on an Al

electrode fabricated using *in situ* integrated sputtering/ALD system [18]. A defective IL can even form during the pre-ALD sample transfer even under HV. Such layers have a profound effect on the dielectric properties of the Al_2O_3 with a significantly reduced ε_r of 0.5-3.3 as compared to the bulk ε_r~9.2. Remarkably, by controlling the pre-ALD exposure to reduce the IL to a negligible level by reducing the heating time to ≤15 min, a high ε_r up to 8.9 was obtained on the ALD Al_2O_3 films of thickness of 3.6-4.8 *nm*. This corresponds to an effective oxide thickness (EOT=$t_{HiK}\cdot 3.9/\varepsilon_{Hik}$) ~1.5-2.1 *nm*. These EOTs are comparable to the EOTs of a high-K dielectric such as 3-4.5 *nm* thick HfO_2 [12]. This is the first time that close to bulk ε_r value was obtained in Al_2O_3 films of thickness <5 *nm* [16] and suggests that the optimal ultrathin ALD Al_2O_3 may provide a low-cost alternative gate dielectric for CMOS.

3.1 Controlling Metal-Insulator Interface

The *in situ* deposition process with optimal growth parameters like ALD temperature, precursor pulse time and purge time is not sufficient for obtaining high quality dielectric. Several issues need to be resolved for the growth of high quality ultrathin dielectric films. First, pre-ALD IL formation, which is primarily the formation of defective oxides on metals surface resulting defective dielectric growth on the top. Secondly, hydroxylation on the metal surface with a defective interface plays an important role in the growth of ALD dielectric, which need to be systematically optimized.

Although, the defective IL formation is primarily formed due to *ex situ* exposure of the metal surface to atmosphere. However, only *in situ* fabrication is not enough to reduce the formation of

IL to negligible. Figure 3.1(a) shows systematic optimization of pre-ALD exposure of metal surfaces by heating at different powers (154, 220 and 304 W) and heating time (75 and 15 min) using STS by *Jamie Wilt et al.* [89]. This study suggests that exposure of fresh metals surface to heat and low vacuum can result in a significantly different top surface. The extended exposure of metals surface at 154 W for 75 min results in the formation of defective IL with low-quality dielectric grown on top referred as "non-optimal condition" (Figure 3.1(b)). This defective IL is due to exposure of metal to O_2 or chemical in chamber resulting defects like oxygen vacancies and interstitials with low E_b comparable to thermal AlO_x ~0.6 eV. However, reduction in exposure time to 15 min at higher power 304 W, known as "optimal condition" (Figure 3.2(c)) can preserve metallicity of the bottom metal surface. When sub-angstrom thick Al_2O_3 dielectric material grown on top show high quality with E_b ~1.4 eV, which more than double as compared to thermal AlO_x.

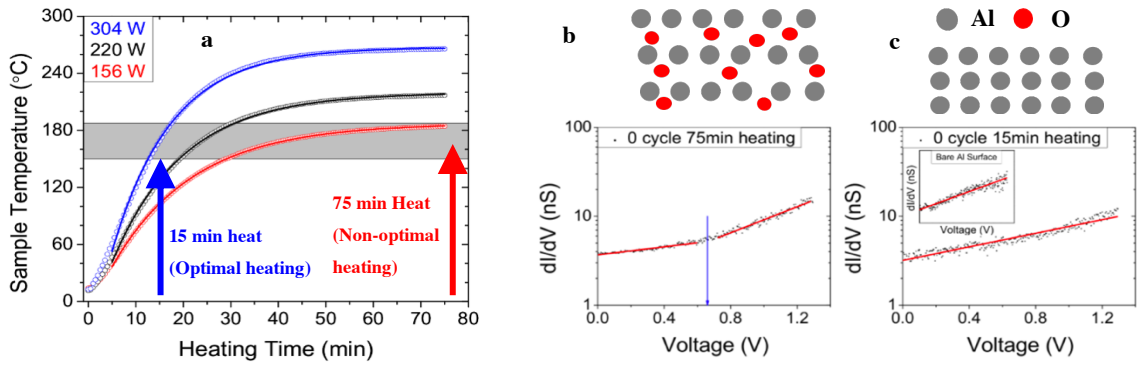

Figure 3.1 a) Measured sample temperature as a function of exposure time in an ALD reaction chamber which has been preheated at the given wattages. The solid lines are fits to the data STS b) *dI/dV* spectra are plotted for an Al sample after 75 min heating in the ALD chamber and (c) after 15 min of heating. The arrows (blue) depict the TB height, calculated as the intersection of the fit lines (red). Diagrams (top) illustrate the expected surface as seen by the STM tip. The insert in (c) is the *dI/dV* spectrum of a sample that was directly transferred to the STM chamber after Al sputtering. This figure is adapted from reference [89].

To control ALD Al_2O_3 nucleation during the first ALD cycles, the Al wetting layer was exposed to a pre-ALD H_2O pulse to create adsorbed hydroxyl molecules on the metal surface. Figure 3.2 shows an *ab-initio* molecular dynamics (AIMD) simulations were performed to study the kinetics for hydroxylation on a 2x2 supercell of face-centered cubic Al (111) under constant equilibrium volume and temperature by *Jamie Wilt et al.* [89]. The results show that when only one H_2O molecule is present on the Al surface (i.e. without any other H_2O in proximity), the dissociation into -OH is thermodynamically unfavorable Figure 3.2(a) (I and II). However, when multiple H_2O molecules are nearby, dissociation occurs after just a few ps Figure 3.2(a) (III and IV). The mechanism is a proton transfer between nearby H_2O, which creates an intermediate compound that dissociates to form -OH group. The areal density of the H_2O pulse is crucial to facilitate an efficient hydroxylation reaction, which can form a uniform monolayer of -OH on the Al surface. These results agree well with the STS study on 1 cycles ALD Al_2O_3 showing an increase in surface coverage from ~54% at 1 s pulse duration to ~93% at 2 s duration as in Figure 3.2(b). Thus, experimentally observed time frames suggest that long initial H_2O pulses ~2s, are required for H_2O molecules to adsorbed to the Al surface and reach a high enough areal molecular density for an efficient dissociation into hydroxylation. Interestingly, longer than 2s H_2O pulses led to a reduced ALD Al_2O_3 surface coverage due to steric hindrance as supported by the simulations.

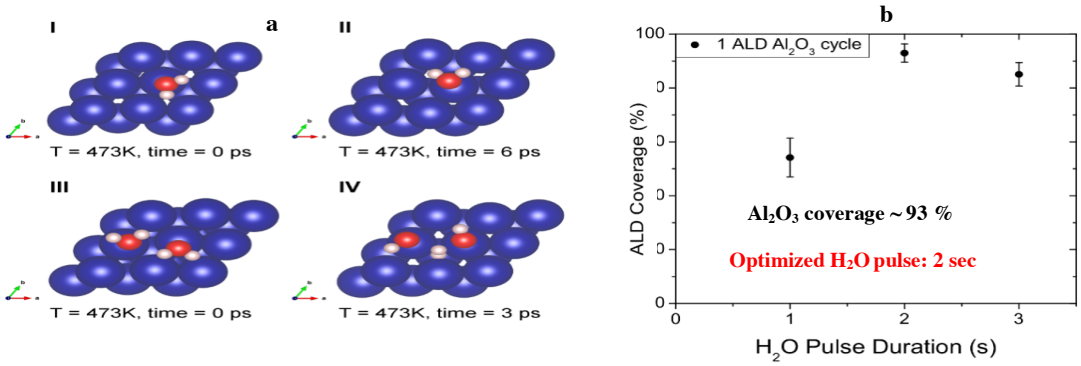

Figure 3.2 (a) AIMD simulations are shown for H_2O adsorption onto an Al (111) surface. When only one is present on the Al surface, dissociation is thermodynamically unfavorable (I, II). However, when are in close proximity, dissociation into -OH and is nearly instantaneous (III, IV). (b) The percentage of the Al surface which had a barrier height consistent with ALD Al_2O_3 after one ALD Al_2O_3 cycle is shown verses a variable initial H_2O pulse duration from. This figure is adapted from reference [89].

After the optimization of dynamic heating conditions for pre-ALD IL formation and exposure time of Al metal surface for H_2O pulse, the devices were tested for uniform and high quality ultrathin ALD Al_2O_3 barrier using MIM device structure, which are important components for today's microelectronics device applications. First, the comparison of dielectric properties between optimal and non-optimal conditions with 4.4 *nm* ALD Al_2O_3 MIM devices will be discussed. Figure 3.3(a) shows the capacitance as the function of the applied electric field ($E=V/d$). Here d is the thickness of the ALD Al_2O_3 dielectric film and V is the applied voltage. E was restricted to ~2 MV/cm for all samples to avoid dielectric breakdown. Figure 3.3(a) represents the comparison of $Al/Al_2O_3/Al$ trilayer capacitors with a cross-sectional area 0.08 mm^2. The observe capacitance for optimal devices is ~3 times higher as compared to non-optimal devices due to the presence of negligible IL between Al/Al_2O_3 interface leading to the perfect dielectric film growth. However, non-optimal condition shows the presence of IL which is defective is in series with the pure

dielectric film, which indeed reduces the total capacitance with a corresponding increase in the leakage current. As the defective dielectric acts like a pinhole or defects with the presence of conducting channel for the flow of current in dielectric film. Our observation is consistent with the increase in leakage current by more than 3 order of magnitude higher for non-optimal conditions as in Figure 3.3 b). Indeed, the optimal ALD condition results in the growth of high quality dielectric resulting better interface between Al/Al_2O_3 and negligible IL formation.

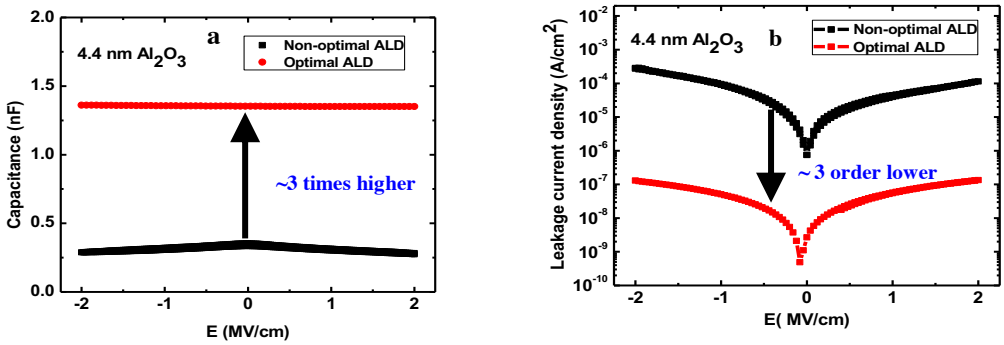

Figure 3.3 Comparison of a) capacitance and b) leakage current for 4.4 nm $Al/Al_2O_3/Al$ MIM device fabricated with optimal (red) and non-optimal (black) condition with maximum applied electric field 2 MV/cm.

Based on the above transport measurement on two different dielectric films, the proposed growth mechanism for non-optimal and optimal ALD Al_2O_3 dielectric growth is shown in Figure 3.4. Figure 3.4(a) shows the schematic for the non-optimal case of the formation of IL leading to the growth of defective Al_2O_3 with defects and pinholes. Thus, Al_2O_3 dielectric is in series with IL leading to an increase in the leakage current. However, at optimal conditions with well controlled ALD parameters IL formation is reduced to negligible resulting in perfect high quality dielectric as in Figure 3.4(b).

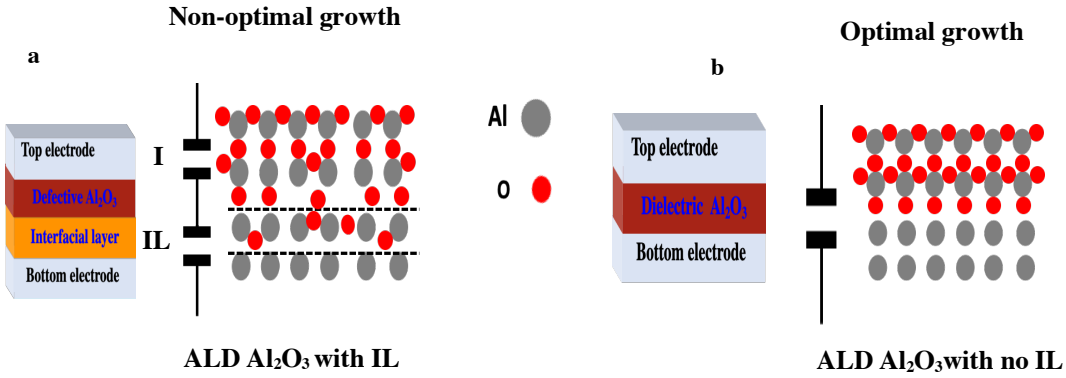

Figure 3.4 Schematic showing the comparison non-optimal with the formation of interfacial layer in series with defective dielectric and optimal growth of ALD Al_2O_3 on metal surface resulting high quality dielectric.

3.2 Properties of Optimal ALD Al_2O_3 Ultrathin Dielectric Films

For further discussion properties of MIM devices fabricated with optimal ALD condition will be presented unless otherwise indicated. Figure 3.5(a) shows the measured capacitance for Al/Al_2O_3/Al trilayer capacitors with 10-40 ALD Al_2O_3 cycles, or 1.1-4.4 *nm* in thickness with area 0.08 mm^2 as a function of *E*. At larger thicknesses in the range 1.65-4.4 *nm*, the capacitance is independent of the *E* before dielectric breakdown. This constant capacitance indicates that high quality Al_2O_3 dielectric growth was achieved. At the smallest thickness of 1.1 *nm*, the capacitance has a moderate *E* dependence. Specifically, capacitance decreases with increasing *E*, which suggests an increase in the leakage current due to electron tunnelling [95]. It can be observed that the capacitance vs. thickness is not proportional to *1/d,* as expected in the case of ideal capacitors. Thus, at smaller thickness below 2 *nm* MIM devices do not behave like ideal capacitors as given

by the equation $c = \varepsilon_o \varepsilon_r A/d$, where ε_o is the permittivity of free space and A is the area of the capacitor, which is due to the effect of quantum tunnelling.

To further understand the performance of devices across the sample, the variation of specific capacitance (C_o) = $C/A = \varepsilon_o \varepsilon_r/d$, with junction area of 0.08, 0.06 and 0.04 mm^2 MIM trilayer samples for ALD Al_2O_3 thickness in the range 1.1- 4.4 *nm* with a negligible IL is shown in Figure 3.5(b). The C_o is expected to be a constant for ideal capacitors. A 10% variation of the specific capacitance was observed for 4.4 (black), 3.3 (red) and 2.2 *nm* (blue) thick Al_2O_3 chips. This variation is comparable to the capacitor area variation of the shadow mask. This result suggests that the ALD Al_2O_3 films are highly uniform in this thickness range. However, a higher variation of ~20-30% was observed on the 1.65 (dark cyan) and 1.1 (magenta) *nm* ALD Al_2O_3 chips, which is not surprising since the effect of defects and pinholes will be amplified at such a small thickness.

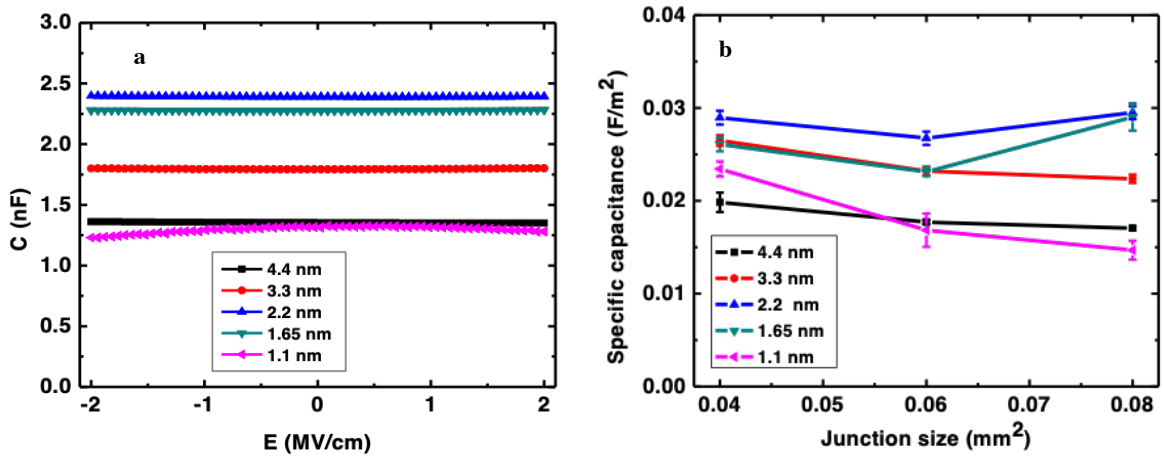

Figure 3.5 Variation of a) capacitance and b) specific capacitance with junctions areas for MIM Al/ALD Al_2O_3 (4.4-1.1 nm)/Al MIM capacitors fabricated using optimal ALD conditions.

The mechanisms behind this decreasing trend in capacitance and large variation in C_o was used to understand the properties of non-ideal capacitor behavior. ε_r was calculated from the measured C values using the equation $\varepsilon_r = Cd/A\varepsilon_0$. Figure 3.6 compares the calculated ε_r of the ALD Al_2O_3 films made with the optimal (black data)[14] (in the thickness range 1.1-4.4 *nm*) and non-optimal (red data) [15] (at two different thicknesses of 1.1 *nm* and 4.4 *nm*) ALD conditions. ε_r values for the former are significantly higher than in the latter, suggesting that the dielectric properties of ultrathin ALD Al_2O_3 films strongly depends on the presence of the IL. With optimal ALD conditions the IL is negligible and ε_r ~ 8.9 for 3.3–4.4 *nm* thick ALD Al_2O_3 was observed, corresponding to an EOT~1.4-1.9 *nm*, respectively. These EOTs are comparable to the EOTs of a high-K dielectric such as 3.0-4.5 *nm* thick HfO_2 [11, 12] and this suggests that the optimal ultrathin ALD Al_2O_3 may provide a low-cost alternative gate dielectric for CMOS.

Furthermore, ε_r 8.9 for 3.3-4.4 *nm* thick ALD Al_2O_3 films is only about 3.3% lower than the bulk Al_2O_3 value of ~9.2 [82] and more than double than the best previously reported value ε_r ~4.0 for 3 *nm* thick ALD Al_2O_3 [71]. In contrast, with non-optimal ALD conditions at which an IL is present, ε_r is considerably lower with a value in the range of 2.5-3.3 for 4.4 *nm* thick ALD Al_2O_3 as shown in Figure 3.6. The difference in ε_r illustrates the significant effect that an M-I IL has on the dielectric property of thin dielectric films. Specifically, a defective IL is in series with the ALD Al_2O_3 layer. This IL degrades the dielectric properties of the composite IL/ALD Al_2O_3 film. In addition to introducing a poor-quality IL capacitor, the ALD Al_2O_3 film grown on top of an IL is also defective, which can further decrease the ε_r. Even at a substantially larger thickness of ~60

nm, the ε_r was reported to be just 7.6 for *ex situ* deposited ALD Al_2O_3 film on n-type Si and Mo coated Si-substrate [71]. An IL ~1.1 *nm* was reported to form on n-type Si substrate and a similar IL is suspected to form on Mo-coated Si-substrate [71]. Since the IL is difficult to avoid in *ex situ* fabricated MIM trilayers, it is reasonable to expect lower ε_r in the samples with more significant IL growth. The $\varepsilon_r \sim 7.2$ is obtained for 2.2 *nm* ALD Al_2O_3 film without IL which corresponds to EOT~1.2 *nm* comparable to the EOT of a 4.5 *nm* of HfO_2 high-K dielectric film [73]. However, based on EOT comparison the actual physical thickness of 2.2 *nm* ALD Al_2O_3 is much lower than high-K material. This result demonstrates the feasibility of incorporating ultrathin ALD Al_2O_3 with high-K material as a gate dielectric in CMOS. A significant decrease in ε_r in the range of 0.4-0.9 was observed for the 2.2 *nm* ALD Al_2O_3 film with non-optimal ALD conditions when an IL was present. The decrease in ε_r with the film thickness have been observed for the high-K dielectric HfO_2 [11, 12, 73] with thicknesses in the range of 1-4.5 *nm* and also for ZrO_2 films in a comparable thickness range of 4-6.5 *nm*. This result illustrates the critical importance to elimination the IL to obtain high quality ultrathin dielectric films. ε_r significantly reduced for the ALD Al_2O_3 thin films with poor dielectric films fabricated either *in situ* with the non-optimized conditions or ex situ due to the presence of IL. When the IL is negligible, ε_r remains constant for the ALD Al_2O_3 films with 3.3 and 4.4 *nm* thickness.

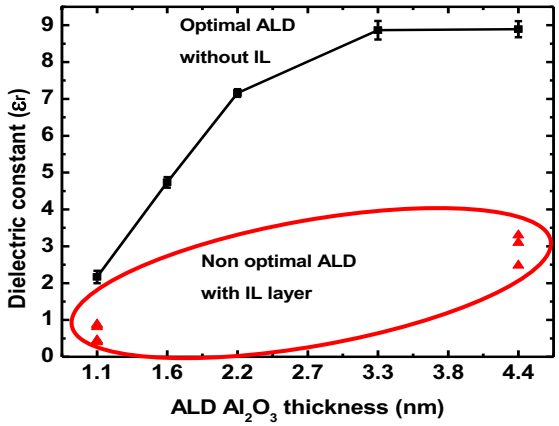

Figure 3.6 Variation dielectric constant with thickness of ALD Al_2O_3 (1.1-4.4 nm) capacitors fabricated using optimal (black) indicating close to bulk $\varepsilon_r \sim 8.9$ at 3.3-4.4 nm and non-optimal (red) indicating) $\varepsilon_r \sim 2.5$-3.3 at 4.4 nm ALD parameters.

3.3 Estimates of Thickness of Interfacial Layer

When the thickness of the dielectric film is further reduced below 3 *nm*, a monotonic decrease of ε_r with the dielectric film thickness is observed especially in the thickness range of 1.1-2.2 *nm* as in Figure 3.6. There are two possibilities for decreasing trend in ε_r: 1) increase in quantum tunnelling that increases the leakage current subsequently decreasing capacitance and 2) presence of an IL in series with capacitance. To rule out the possibility that a thin IL with a substantial thickness for the data point as shown with star for pure dielectric capacitor could play a more significant role in this thickness range, a fitting of the measured capacitance (C_T) as function of the dielectric thickness was carried out with an assumption that an IL capacitor (C_{IL}) is connected in series with an ideal capacitor for ALD Al_2O_3 films (C_{ALD}) described by the equation (8).

$$\frac{1}{C_T} = \frac{1}{C_{ALD}} + \frac{1}{C_{IL}} \qquad (8)$$

The specific measured capacitance can then be calculated using equation (9).

$$\frac{C_T}{A} = \frac{\varepsilon_o}{\left(\frac{T_{IL}}{\varepsilon_{IL}} + \frac{T_{ALD}}{\varepsilon_{ALD}}\right)} \qquad (9)$$

where T_{IL} and T_{ALD} are thicknesses of the IL and ALD Al_2O_3 films in *nm*, and ε_{IL} and ε_{ALD} are the dielectric constants for the IL and ALD Al_2O_3 dielectric films, respectively. T_{IL} (in nm) and ε_{IL} are unknown parameters and several values of their ratio $\frac{T_{IL}}{\varepsilon_{IL}}$ from 0.01 to 0.3 were used in the fitting as in Figure 3.7. The ratio $\frac{T_{IL}}{\varepsilon_{IL}} = 0.01$ curve (black) provides the best fit to the C_o of the 4.4, 3.3 and 2.2 *nm* thick ALD Al_2O_3 films (star data point shown with red circle). Assuming $\varepsilon_{IL} = 1$ or 2 for the defective IL, the IL thickness would be $T_{IL} = 0.1$ Å and 0.2 Å respectively. This means that the IL is indeed negligible and the decrease in the measured C_o for ALD Al_2O_3 films in thickness range 1.1-2.2 *nm* is primarily due to the electron tunnelling. In this case, the circuit could be modelled as a resistor connected in parallel with the Al/ALD Al_2O_3/Al capacitor schematically shown in the inset of Figure 3.7. Our results show that 30 Ω resistor when connected in parallel with a 3.7 nF capacitor (comparable to the capacitance of 1.65 *nm* ALD Al_2O_3 film) results in a decrease in capacitance to 2 nF, which is 40% lower than a pure dielectric capacitor. This result suggests that the decrease in the measured specific capacitance of the 1.1-2.2 *nm* thick ALD Al_2O_3 dielectrics (star data point shown with green circle) is due to tunnelling of electrons. To confirm

this argument, we have carried out an ac impedance measurement on the MIM samples which can give the information about the dominant components in the circuit.

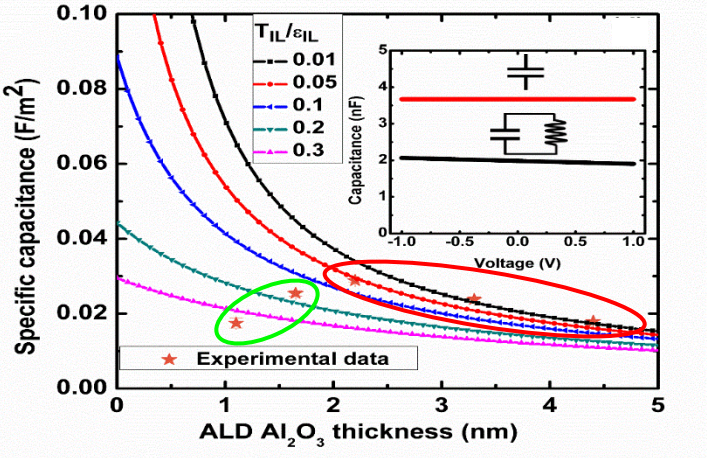

Figure 3.7 Comparison experimentally obtained specific capacitance data for ALD Al2O3 dielectric with the modelling based in the assumption that interfacial layer capacitance capacitor is connected in series with an ideal capacitor for ALD Al2O3 films. The inset shows an experimental verification of modelling showing the decrease in the measured capacitance for a standard 3.7 nF capacitor when connected in parallel with a 30 Ω resistor.

3.4 AC Impedance Measurement

The ac impedance spectroscopy measurement for MIM trilayers was performed using small time varying perturbation of 10 mV at a constant base potential. The difference between the input and output signal along with their phase angle gives more information about the dominant components within the circuit like a resistor or a capacitor over the different frequency range [96, 97]. The graphical representation using three different component, real and imaginary components of impedance (Z) i.e. real Z and imaginary (im) Z, and phase angle variation (ϕ) are widely used to represent impedance measurement data [96, 97]. To confirm that the electron tunnelling is responsible for the monotonic decreasing trend in ε_r for 1.1-2.2 *nm* thick ALD Al_2O_3 dielectrics

rather than IL formation, which is equivalent to a resistor connected in parallel with the Al/ALD Al_2O_3/Al capacitor *i.e.* R‖C behavior. Figure 3.8 summarizes the impedance results for 4.4 *nm* (40 cycle) and 1.65 *nm* (15 cycle) ALD Al_2O_3 film. In the former the circuit is expected to consist of only a capacitor, while in the latter, a combined circuit of a R‖C behavior is anticipated considering the electron tunnelling (as form inset for Figure 3.7). Figure 3.8(a) shows the nature of Nyquist plot obtained using real Z against imaginary Z represent capacitive behavior for 4.4 *nm* ALD Al_2O_3 film and R‖C behavior for 1.65 *nm* ALD Al_2O_3 film[96] in agreement with our experimental results and modelling. Quantitatively, the values of capacitance at 1 KHz for the 4.4 *nm* and 1.65 *nm* samples are 1.4 and 2.3 nF respectively, which are in good agreement with that obtained from the C-V measurement in Figure 3.8. The resistance of 52 ohm for the 1.65 *nm* sample is consistent with that used in the inset in Figure 3.7. The phase angle variation with frequency as in Figure 3.8(b) confirms that 4.4 *nm* ALD Al_2O_3 film shows pure capacitive behavior with phase lag by 90°. However, 1.65 *nm* ALD Al_2O_3 shows expected R‖C behavior with capacitive behavior with phase lag by 90° at a higher frequency and resistive without any phase variation i.e. 0° at lower frequency confirming the above observation of quantum tunnelling at thickness below 2 *nm*.

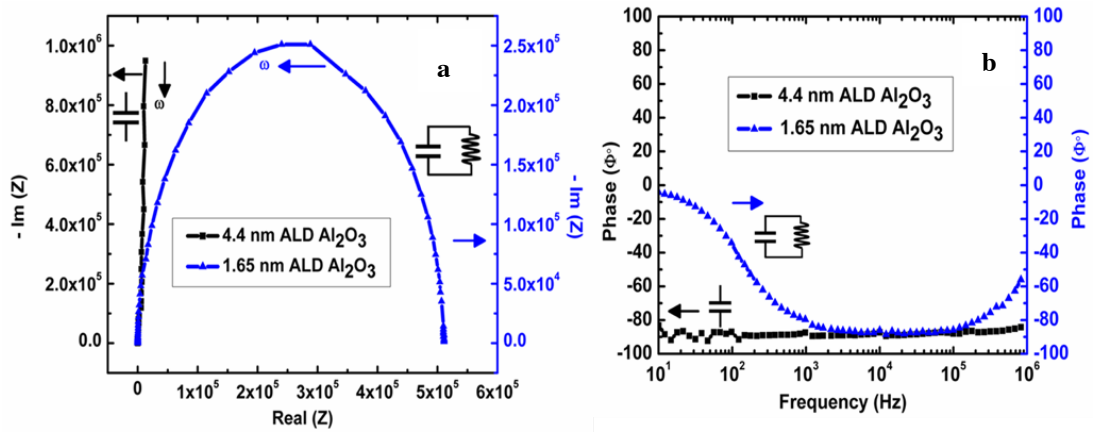

Figure 3.8 AC impedance measurement a) A Nyquist plot and b) a phase variation with frequency measured on 40 cycle (4.4nm, black)) and 15 cycle (1.65 nm, blue) ALD Al2O3 MIM capacitors.

3.5 Leakage Current and Breakdown Characteristic of Dielectric

The understanding of the growth mechanism and leakage characteristic is critically important for device application especially for ultrathin dielectric films. The properties of three ALD Al_2O_3 dielectric films thicknesses 4.4, 2.2 and 1.1 *nm* were studied as shown in Figure 3.9. The 4.4 *nm* (black) thick ALD Al_2O_3 film with a negligible IL has a low J~10^{-9}A/cm^2 at zero bias, which increases to ~10^{-7}A/cm^2 with an increase in E to 2 MV/cm. This value of J at zero bias is two orders lower for ALD Al_2O_3 films even at 6.5 *nm* [83] and comparable to 12 *nm* [71] for ex-situ, which is an indicator of the higher quality of *in situ* fabricated TBs with a negligible IL. For 2.2 *nm* thick ALD Al_2O_3 film (red) J ~10^{-6}A/cm^2 at zero bias and increases to 10^{-4} A/cm^2 with the corresponding increase in E to 2 MV/cm. A similar increasing trend in J is observed for 1.1 *nm* thick Al_2O_3 films (black) with J~10^{-3} A/cm^2 at zero bias, which significantly increases to ~1 A/cm^2 at 2 MV/cm. This increase in J is due to quantum tunnelling of electrons that start to dominate at

dielectric thickness below 2 *nm* as expected for ultrathin dielectric films [71, 95]. Thus, with a decrease in the thickness of ALD Al_2O_3 dielectric films makes MIM capacitors more susceptible to higher leakage current even at smaller *E*. The similar trend is observed for SiO_2 or for even high-K material when pushed to ultrathin thickness below 2 *nm*. This trend is not related to the quality of TB as explained with observe decrease in ε_r but associated with an increase in quantum tunnelling as in Figure 3.6. Due to the higher quality of TB through reduction of the IL and *in situ* ALD fabrication, we can push the limit of our C-V measurement to ultrathin ALD Al_2O_3 thickness, which is not only an extension of previous work done by many research groups [71, 83, 84] but also finds an important application in CMOS and MIMTJs.

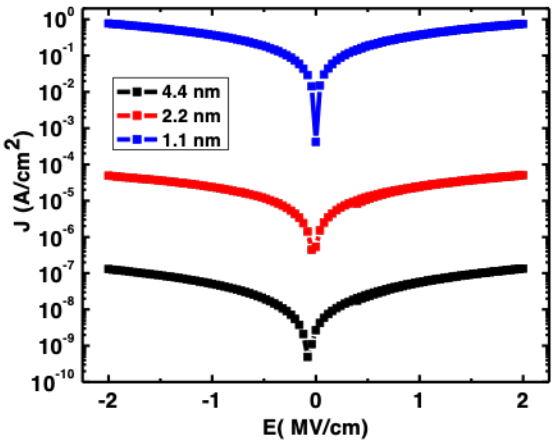

Figure 3.9 Leakage current density vs. electric field (*J-E*) for MIM capacitors fabricated using optimal ALD condition for 4.4, 2.2 and 1.1 nm ALD Al_2O_3 dielectric film.

The characteristics of TBs under intense electric field (>10 MV/cm) provides an additional insight into the quality, nature and significance of the IL often known as dielectric breakdown. There are mainly two main type of breakdown characteristics for ultrathin dielectric. First, soft breakdown

that occurs in gradual manner as disorder within the TB increases through defect migration eventually leading to the significant increase in *J*. This soft breakdown characteristic is observed in the TB with defective IL with high defects or pinholes leading to the growth of defective dielectric film on the top. Interestingly after soft breakdown, the removal of *E* in the dielectric film can recover its insulating property. This is an important parameter to evaluate the strength of the ALD Al_2O_3 dielectric film. The breakdown dielectric behavior is studied using figure 3.10 with *J* vs. *E* by increasing *E* until the dielectric film shows a sudden increase in *J*. The 4.4 *nm* thick ALD Al_2O_3 (black) show *J* ~10^{-7} A/cm^2 with *E*~2 MV/cm which significantly increases to ~10^{-5} A/cm^2 (blue) due to the corresponding increase in the leakage current when *E* approaches 5 MV/cm, this is known as soft dielectric breakdown [98, 99] .

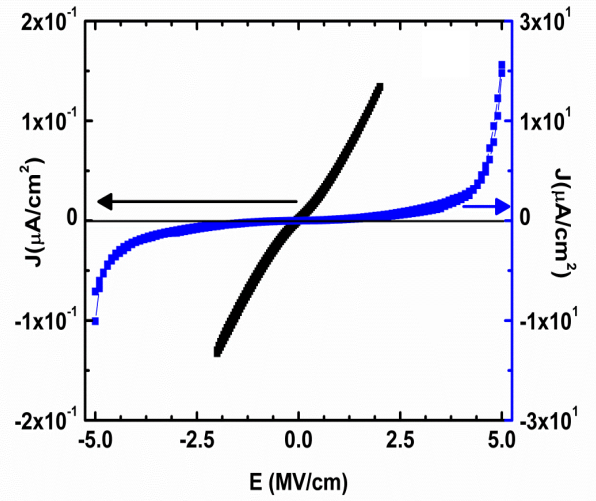

Figure 3.10 Leakage current density vs. electric field for 4.4 nm Al_2O_3 before (black) and after (blue) soft dielectric breakdown where dielectric can recover its original I-V after removal of external field.

Next, hard breakdown occurs with the sudden breaking of Al_2O_3 bonds in dielectric film leading to the sudden increase in the leakage current. After this traumatic breakdown event, the insulator becomes metallic with a large spike in leakage current and result in a linear I-V after breakdown. Figures 3.11(a) and (b) show a hard-dielectric breakdown electric field (E_{HBR}), which makes the dielectric film lose its insulating property and become conductive. The 4.4 *nm* thick ALD Al_2O_3 film (black) shows E_{HBR} ~6.2 MV/cm comparable to ~7-8 MV/cm reported for a thicker film ~100 *nm* [71, 83] indicating the better quality of ultrathin dielectric ALD Al_2O_3 films fabricated using our *in situ* sputtering and ALD system [18]. The enhancement in E_{HBR} ~10 MV/cm is observed when the film thickness is reduced to 2.2 *nm* (blue). The E_{HBR} further increases to ~32 MV/cm for 1.1 *nm* ALD Al_2O_3 film, which is consistent with the enhancement of E_{HBR} ~30 MV/cm observed for 1.2 *nm* ALD Al_2O_3 film [95, 100]. The significant increase in E_{HBR} is related to an increase in leakage current due to the quantum tunnelling of electrons through the ultrathin dielectric that prevents ALD Al_2O_3 films from a hard-dielectric breakdown at low E [95, 100]. With an increased contribution of tunnelling current to the total current, which reduces the number of ballistic collisions and therefore heating within the insulator. Thus, these observed high E_{HBR} values in ultrathin ALD Al_2O_3 films show the potential for reducing the thickness of gate dielectrics used in CMOS.

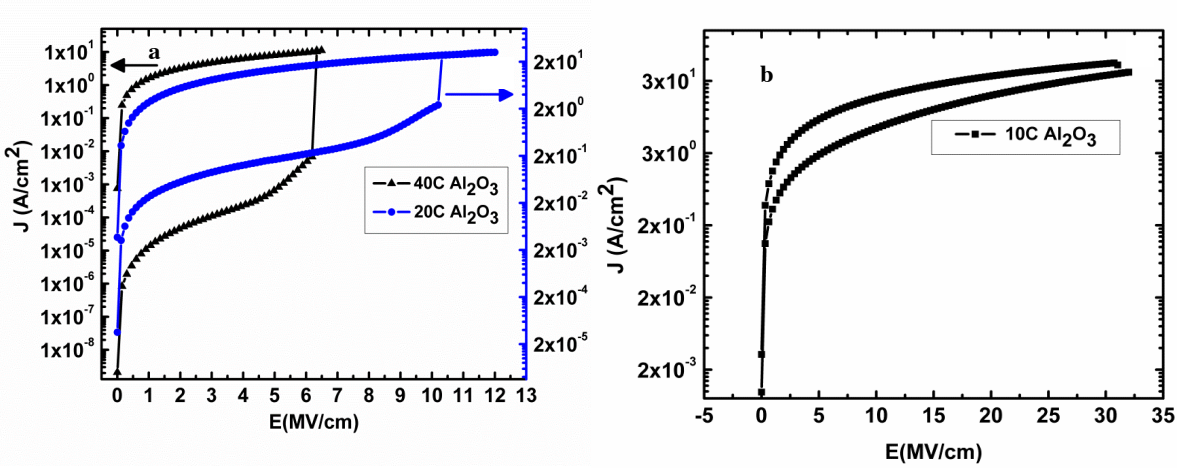

Figure 3.11 Leakage current density vs. electric field after hard dielectric breakdown for (a) 4.4 (black) and 2.2(blue) nm ALD Al_2O_3 and (b) 1.1nm ALD Al_2O_3 cycles.

3.6 *In situ* STS Characterization of ALD Al_2O_3 Films

Taking advantage of the unique all *in situ* fabrication and characterization system, the further studied the quality of dielectric using *in situ* STS method by Jamie Wilt *et al.* [89]. *Ex situ* tunnel junction and capacitance measurements are limited to insulators, which are greater than 1*nm* in thickness due to the requirement of low leakage current [10, 18, 71, 95, 100]. *In situ* STS is not limited by such a constraint, in fact, a high leakage current is required for STS to measure insulators, thus limiting the maximum measurable insulator thickness, which is around 2-3 *nm* for high-k dielectric [101]. Therefore, STS can quantify the ultrathin insulators based on E_b in tandem with the *ex situ* measurements. By varying the bias voltage applied between the sample and an atomically-sharp metallic tip and recording the tunnelling current along with its derivative, STS can probe the local density of states of the insulator [102]. To make electrical contact for the bias voltage, a molybdenum washer was mechanically clamped to the Si/Au substrate as shown in

Figure 3.12(a). The M-I structure was then grown on top and the sample transferred to the STS chamber *in situ* under high vacuum to avoid additional alumina growth.

The STS study on ALD Al_2O_3 TB in thickness range 0.1-1 *nm* or 1-20 cycles on Al has shown that E_b, defined as the CBM, is constant with Al_2O_3 thickness in the range of 1-10 ALD cycles with a value of about 1.5 eV [15]. This E_b constancy with thickness is an indicator that the quality of our ALD Al_2O_3 TB does not change with thickness. The IL formed primarily due to exposure of Al to trace O_2 and/or H_2O during the pre-ALD heating step was systematically reduced by controlling the heating parameters to obtain an increase in ALD Al_2O_3 E_b from about 1.0 eV to about 1.5 eV (with a negligible IL) along with a transition from soft-type to hard-type dielectric breakdown [14, 15]. Therefore, the ALD Al_2O_3 band gap, which is another good indicator for the quality of the insulator, must be constant as well. A representative STS *dI/dV* spectrum is shown in Figure 3.12(b)**.** The band gap is defined as the difference between the CBM and the VBM. On this log (*dI/dV*) scale the Valence and conduction bands should be roughly linear [91]. The band gap region of the STS *dI/dV* curve is nearly flat, indicating a low leakage current through the insulator [63]. We fit linear lines (bisquare method) to the valence band and the conduction band. The VBM and CBM were calculated to be about -1.0 eV and 1.6 eV respectively and were defined as the linear fit line's intersection with the nearly flat band gap region. We found that the ALD Al_2O_3 band gap was 2.63 eV +/- 0.30 eV. This band gap value is comparable to the ultrathin (1.3 *nm*) α-Al_2O_3 band gap of 2– 4 eV [63, 103]. Together with the C-V measurements, this excellent band gap indicates that high quality ultrathin ALD Al_2O_3 growth has been achieved when the IL is minimized.

To expand upon the dielectric breakdown characteristics observed in Figure 3.9, the STS bias voltage was repeatedly ramped up and down with the tip height fixed over one location until dielectric breakdown. I-V and corresponding dI/dV spectra are shown in Figure 3.12(c) and (d) respectively for 10 cycle ALD Al_2O_3 films with a minimized IL**.** Our ultrathin ALD Al_2O_3 TB broke down in a hard-type breakdown behavior where the tunnelling current suddenly increased by a factor of ~1000. This breakdown event occurred near the end of the 13^{th} spectra and can be seen in the corresponding IV curve (Figure 3.13(c)). Subsequent spectra had tunnelling current which was above the saturation current of the STM (~100 nA). This type of breakdown behavior is consistent with epitaxial Al_2O_3, indicating that no significant defective IL is present in our ALD Al_2O_3 TBs [104].

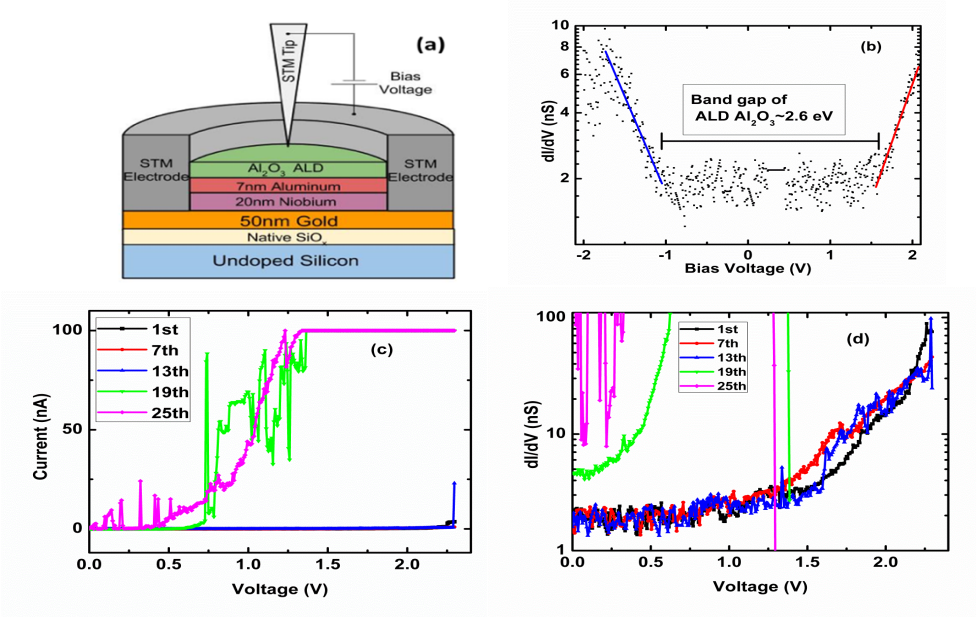

Figure 3.12 *In Situ* Scanning tunnelling spectroscopy for the ALD Al_2O_3 tunnel barrier (a) A schematic for the sample mounting scheme (b) A representative of *dI/dV* spectra with blue and red lines are bisquare method linear fits to the valence band and the conduction band respectively (c) The breakdown characteristics with *I-V* and (d) corresponding *dI/dV* spectra where the bias voltage was sequentially ramped up and down with a fixed tip-sample distance.

3.7 Chapter 3 Conclusion

In summary, we have investigated the effect of control over M-I interface on the dielectric properties of *in situ* fabricated Al/Al_2O_3/Al trilayers with ultrathin (1.1 *nm*-4.4 *nm*) ALD Al_2O_3 dielectric films. Several important observations have been made. First, an IL can still form at the Al/Al_2O_3 interface in high vacuum at a non-optimal ALD growth condition and it has a profound effect on the dielectric properties of the ALD Al_2O_3 dielectric films. Specifically, the IL at the Al/Al_2O_3 interface is defective like thermal AlO_x with higher pinholes and defects on ALD Al_2O_3 is defective, resulting in a low ε_r of ~3.3 for the 4.4 *nm* thick ALD Al_2O_3 films and soft-type

dielectric breakdown ascribed to the mobile defects in the IL/ALD Al_2O_3. On the other hand, the IL can be systematically controlled by preventing pre-ALD exposure of trace amounts of H_2O, oxygen and other chemical species in vacuum. For the 3.3-4.4 *nm* thick ALD Al_2O_3 dielectric films with a negligible IL, we obtained high ε_r ~8.9 approaching that of the bulk Al_2O_3 ~9.2 corresponding to EOT ~1.4-1.9 *nm* respectively and low J ~10^{-9} A/cm^2 at zero bias. This high quality dielectric property is further confirmed by the hard-type dielectric breakdown with E_{HBR} ~32 MV/cm on the 1.1 *nm* thick ALD Al_2O_3. These results illustrate the critical importance in controlling the M-I interface to obtain high quality dielectric films. It also provides the feasibility to reduce the thickness of gate dielectrics for CMOS and MIMTJs, which are important to a large variety of microelectronic applications.

Chapter 4 Effect of Al_2O_3 Seed-Layer on Properties of Ultrathin MgO Films Fabricated using *In Situ* Atomic Layer Deposition

Magnesium oxide (MgO), which is a wide band gap material of 7.80 eV with ε_r ~9.80 and high stability, is an interesting dielectric material for MIM, TJs and other devices [105-109]. Specifically, MgO is the best TB material for magnetic tunnel junctions to allow coherent tunnelling of spin current, which leads to significantly higher tunnelling magnetoresistance up to 200 % [9] in contrast to 70% in MTJs with Al_2O_3 as the TB [47]. MgO has been deposited using CVD [110], pulsed laser deposition [111], homogeneous precipitation, sol-gel processes [108, 109] and ALD [107]. This has motivated research on growth of ultrathin ALD MgO. A systematic study on the dielectric properties of ALD MgO for MIM devices is lacking, which is possibly due to the difficulties to obtain leak-free ultrathin ALD MgO films. However, the study of ALD MgO in the thickness range of 4.6-11 *nm* on Si for metal oxide semiconductor capacitor show close to single crystal bulk MgO [112].

Earlier studies on MgO dielectric suggest presence of more defects and pinholes as compared to Al_2O_3 characterized using STS and structural analysis [113-115]. To prevent the formation of an IL between the M-I interface a recent approach employs an Mg interlayer or graphene [116-118]. Despite this effort, the oxidation of the electrodes is still a potential cause for the formation of IL, resulting in defective dielectric films [118, 119]· It is therefore imperative to address the issue with

the IL formation in development of high quality ALD ultrathin dielectric films. As discussed in chapter 3, we have developed a dynamic heating process to reduce the exposure of the metal surface (in high vacuum) before deposition of ALD Al_2O_3 ultrathin films on Al and Fe using an *in situ* UHV sputtering/ALD process [18]. The M-I IL layer can effectively suppressed in both *in situ* STS studies of the 0.10-1.10 *nm* thickness ALD Al_2O_3 layer and *ex situ* studies of the MIM devices [16]. It is particularly worth mentioning that an ε_r within 3% of the Al_2O_3 single-crystal bulk value has been demonstrated in 3.30-4.40 *nm* thick ALD Al_2O_3 films by reducing the Al/ALD Al_2O_3 IL effect to a negligible level [14-16]. Unfortunately, direct growth of ultrathin ALD MgO films on Al or Fe using the similar *in situ* sputtering/ALD processes failed to generate high quality dielectric films, which is attributed to different nucleation mechanisms of ALD MgO and ALD Al_2O_3 on metals [113, 114, 119]. This problem represents a general problem in the growth of ALD-dielectric on metals with an incompatible M-I interface that prevents uniform nucleation of an atomically thin ALD dielectric film.

The incubation process in ALD of dielectric films is primarily generating oxides on the surface of metals to assist a more efficient ligand exchange between precursors on the sample surface. This means the many of the initial ALD cycles are used for the incubation of native oxides on the metal surface for nucleation of ALD MgO [118-120]. Unfortunately, the native oxides are typically defective as shown in a recent study by our group [14, 15]. ALD dielectric films grown on native oxides can have much degraded electronic and dielectric properties [16, 71, 82, 118-121]. In this chapter, we explore a novel approach of "incubating" a metal surface by *in situ* growth of a sub-*nm* thick ALD Al_2O_3 seed layer (SL) that is high quality and hence will have a negligible negative

impact on the ALD MgO growing on top as compared to the native oxide IL. We show a 0.55 *nm* thick ALD Al_2O_3 SL enables high quality ALD MgO ultrathin (<5 *nm*) film growth. Remarkably, an ε_r up to 8.82-9.38 was achieved in ultrathin ALD MgO dielectric films of thicknesses ~ 3.30-4.95 *nm*, which is in contrast with the leaky ALD MgO counterpart of significantly lower ε_r ~3.55-4.60 without the SL. These results are supported with higher E_b~1.50 eV for MgO/SL and dense nucleation with 100% coverage. However, E_b is reduced to 0.80 eV for ALD MgO without SL and ALD coverage reduced to less than 80%. An *ab-initio* molecular dynamics simulation suggests that the SL layer allows for more regularly distributed Al and OH ligands leading to the growth of denser and high quality ALD MgO dielectric as compared to the case on Al films, which is by its nature not self-terminating and is anticipated to have a relatively rougher terrain for subsequent growth of dielectric films. Thus, the SL approach may be applied to engineering the M-I interface for growth of high quality ALD-dielectric ultrathin films on metals that would be otherwise incompatible [122].

4.1 Controlling Interfacial Layer Formation for ALD MgO

There have been difficulties in the direct growth of ALD MgO ultrathin (<5 *nm*) films on metals due to the low volatility of the Mg precursor which results in non-uniform nucleation. Typically, it requires an incubation stage, which means first tens or even more of ALD cycles are used to promote the formation of native oxides on the metal surface for nucleation of ALD MgO [118-120]. The native oxides are typically defective as shown in our recent study. ALD dielectric films grown on native oxides have much degraded electronic and dielectric properties. The direct

comparison between ALD Al_2O_3 and native AlO_x on the Al surface indicates that the former has a significantly reduced defect concentration [14]. In STS study on AlO_x < 0.6 *nm* thickness was found leaky with zero to very small E_b~ 0.6 eV. We have found that the direct growth ALD of MgO ultrathin films on Al and Fe is difficult. However, MIM structures are leaky even when the MgO film thickness is 4.4 *nm*. This is a contrast to high quality ALD Al_2O_3 ultrathin films of thickness as small as 0.1 *nm* on Al and Fe [14, 15]. To resolve this issue in ALD growth of MgO on metals, a SL approach was developed to bypass the difficulty of ALD MgO growth directly on metals. The ALD Al_2O_3 SL differs fundamentally from native oxides on metal surfaces. Based on the nucleation mechanism, Figure 4.1 shows schematic for both optimal and non-optimal growth of MgO dielectric. Figure 4.1(a) shows a schematic of optimal MgO growth that results in the perfect interface between M-I interface resulting in the growth of high quality MgO film. The dielectric contribution of sub-*nm* SL is negligible as compared to thick MgO films. The primary influence of SL is for the dense nucleation leading to the growth of a perfect MgO dielectric film. However, Figure 4.1(b) shows the schematic for difficultly in nucleation for MgO with fist few incubation cycles for the formation of dense hydroxylation that results in the formation of IL which lead to defective MgO leading to low quality dielectric film.

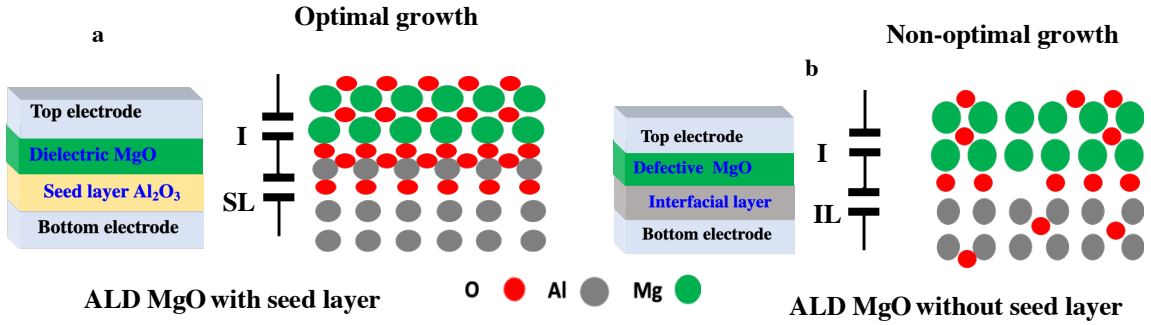

Figure 4.1 Growth mechanism for a) ALD MgO with ALD Al_2O_3 (dielectric with dense -OH nucleation) with seed layer Al_2O_3 showing perfect dielectric growth b) ALD MgO without seed layer (dielectric with less -OH nucleation and possibility of pinholes for ALD MgO without Al_2O_3 seed layer forming interfacial layer resulting defective dielectric showing perfect dielectric growth.

4.2 Ab initio Molecular Dynamics Simulations

To shed light on the effect of the SL, reactive MD Simulations were carried out by our collaborator Ridwan Sakidja to compare the ALD MgO growth on two surfaces with different configurations of OH groups distribution: OH groups distribute in a regular pattern on top of Al (111) surface, which represents the case of MgO/SL as shown schematically in Figures 4.1(a); and OH groups distribute disorderly on Al (111) wetting layer, which represents the case of MgO/WoSL as shown in Figures 4.1(b). The simulation results suggest that the OH pattern and density on the sample surface have a direct impact on the number of Mg-O bonds in subsequent Mg precursor pulse as in agreement with the proposed growth mechanism as in Figure 4.1. Figures 4.2(a) and (b) corresponds to the side view of atomic trajectories for "orderly placed" OH deposition after 0 and 25,000 fs respectively. In this case, we barely see any occurrence of water vapor release implying the retention of OH molecules through the OH-OH lateral bonding formation of oxide cluster on

the surface, presumably creating a denser dielectric film. Figure 4.1 (a) shows a schematic of the proposed growth of MgO directly on Al (111) surface, resulting in not self-terminating -OH and consequently a defective IL in series with MgO dielectric. To support the argument, Figures 4.2(c) and (d) depicts the side view trajectories with "randomly-placed" OH groups on the Al (111) surface after 0 and 25,000 fs respectively. Instead of forming a continuous OH layer as a result of the reaction between the adsorbed water molecules, some are deprotonated, releasing hydrogen and leaving oxygen on the Al surface. This leads to a low surface density and coverage of adsorbed OH on the Al surface, hence defective ALD MgO in subsequent ALD growth. Therefore, the SL allows for dense and ordered OH ligands to assist ALD MgO dielectric growth.

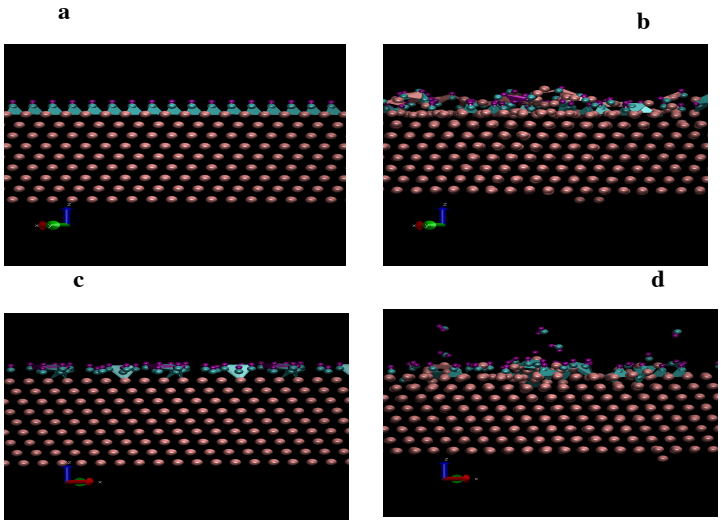

Figure 4.2 a) and b) Side view of the atomic trajectories for the case of 'orderly placed" (representing -OH on the Al(111) surface after 0 and 25,000 fs respectively; c) and d) Side view of the atomic trajectories for the case of 'disorderly placed" (representing -OH on the Al(111) wetting layer after 0 and 25,000 fs respectively.

4.3 Optimization of Thickness of ALD Al_2O_3 Seed Layer

As the simulation results suggest that the hydroxyl monolayer formed on the Al surface may be partly destroyed through deprotonation upon ligand exchange with $MgCP_2$, resulting in the release of oxygen and hence the formation of native AlO_x on the Al surface. Also, we found that the residual hydroxyl groups left on the sample surface due to incomplete ligand exchange with $MgCP_2$ may contribute to the surface charges. We should also mention that we have investigated the surface roughness of the ALD samples on flat and rough surfaces and found all ALD films are very smooth since the ALD coating is conformal and self-limiting. Based on the results from previous works by our group and others, we initiated the idea of using an ALD Al_2O_3 SL to facilitate the ALD MgO growth with the following hypotheses: 1) the hydroxyl groups on the oxide surfaces, such as the native oxides formed during the incubation mentioned above and the ALD Al_2O_3 SLwould be much more efficient in the ligand exchange with $MgCP_2$; and 2) replacing the native oxides formed in the incubation with the ALD Al_2O_3 SL would minimize degradation of the electronic and dielectric properties of the ALD MgO.

Figure 4.3 show the transport measurement on the MIM devices with variation of the SL thicknesses in the range of 0.22-0.55 *nm* (or 2-5 ALD Al_2O_3 cycles) to fabricate the capacitors of total 30 cycles (25 cycles + 5 SL, 26 cycles + 4 SL, and 26 cycles + 3 SL). The SL plays a significant role in initial nucleation and dense hydroxylation for subsequent ALD MgO. When there is no SL, deprotonated releasing hydrogen from water may leave oxygen on the Al surface, resulting in the formation of native oxides and incomplete coverage of the hydroxyl groups on the

sample surface. We observe that with a decrease in thickness of the SL the dielectric properties of MgO film decreases possibly due to non-uniform nucleation for MgO as discussed in Figure 4.2. For example, MgO with 5 cycles Al_2O_3 SL show ε_r close to bulk value with E_b ~1.50 eV and almost 100% coverage. A further decrease in SL thickness ε_r decreases and reduced to ~22-30 % for 3 cycles Al_2O_3 SL with a reduction in ALD coverage. Unfortunately, the dielectric study for SL thickness below 0.33 *nm* (or 3 cycles) is unreliable with high leakage due to non-uniform nucleation resulting defects and pinholes. This agrees well with the *in situ* STS result of incomplete coverage of MgO dielectric with 0.22 *nm* (or 2 cycles) SLor MgO directly on Al. Based on these studies, the 0.55 *nm* (or 5 cycle) ALD Al_2O_3 SL is optimal and results in the best dielectric properties of the ALD MgO.

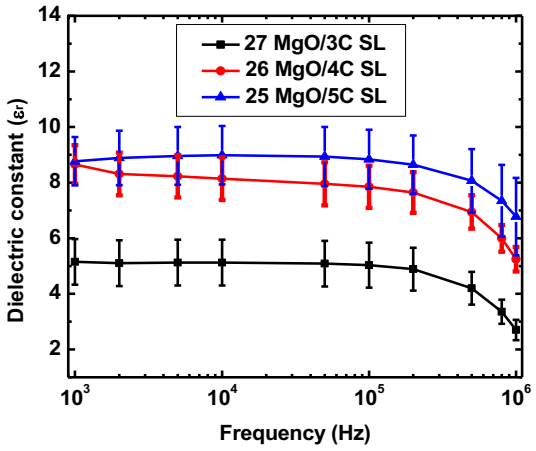

Figure 4.3 Dielectric constant variation with frequency for total thickness of 3.3 nm MgO/SL with variation of seed layer thickness 0.33-0.55 nm (or 3-5 ALD cycles).

4.4 Dielectric Properties of MgO With and Without Seed Layer

The confirmation of the growth of MgO was done using FTIR spectra taken on ALD MgO 2.2 *nm* (or 20 cycles) films deposited at the optimal conditions with substrate temperature 200 °C and source heated to 100 °C. The appearance of absorption peaks at 495, 640, 750 and 960 cm^{-1} are indexed to MgO [121, 123]. The dielectric properties of MgO with SL in thickness range 2.75-4.4 *nm* or 25-40 cycles were compared to those of 4.4 *nm* MgO without SL have been deposited.

Figure 4.4(a) shows variation of C_0 with frequency in the range from 1 KHz-1 MHz measured on MIM capacitors with different "I" layers of ALD MgO of thicknesses of 2.20, 2.75, 3.30 and 3.85 *nm* on the SL (colored curves). Also, a device with 4.4 *nm* thick ALD MgO without a SL is also included for comparison (black). The C_0 is defined from $C_0 = C/A = \varepsilon_0\varepsilon_r/d$ for different MIM devices and the dielectric thickness (d) regards the total thickness of the SL and the ALD MgO thickness. The error bars were calculated using the three devices fabricated on the same sample with different capacitor areas of 400x100, 300x100 and 200x100 μm^2, respectively. The MIM devices with the ALD MgO/SL show an almost constant C_0 in the frequency range from 1-100 KHz (within 4-6% variation). With a further increase in the frequency, C_0 decreases due to dielectric loss [124, 125]. In addition, an almost constant C_0 was observed on the composite devices with the ALD MgO/SL in the thickness range of 3.30-4.95 *nm*. At a smaller ALD MgO/SL thickness 2.75 *nm*, C_0 decreases considerably by 35-50 % possibly due to effect of electron tunnelling which will be discussed later. In contrast, the MIM devices with the ALD MgO/WoSL show an overall lower C_0 by a factor >2 and more significant frequency dependence possibly due to defects initiated at the defective M-I

interface [126]. Figure 4.4(b) shows the variation of ε_r with frequency calculated using $\varepsilon_r = C_0 t/\varepsilon_0$ from the data in Figure 4.4(a). The ε_r shows a similar frequency dependence to that of C_0, which is almost constant in the frequency range of 1-100 KHz with a small decrease of 4-5%. Further increasing frequencies, ε_r shows a larger decrease and this decrease is significantly larger on samples with lower ALD cycles. This larger variation of both C_0 and ε_r at higher frequencies can be explained by a capacitive response and dielectric loss of the MIM capacitor with fast charging and discharging since at large frequency all charges or dipoles cannot respond with fast polarity switching [124, 125]. Our results indicate that these ALD MgO capacitors are well suited for application in the frequency range up to 100 KHz but are less suitable for application which requires higher frequency application in MHz or GHz. It should be noted that the independent measurement of ε_r for the 0.55 *nm* ALD Al_2O_3 SL cannot be accomplished using the MIM structure since electron tunnelling become possible as the thickness of the ALD Al_2O_3 is comparable or below 2 *nm* and increases exponentially with decreasing ALD Al_2O_3 thickness reported earlier [16]. Considering the comparable single-crystal bulk dielectric constants of the Al_2O_3 (~9.2) and MgO (~9.8) and negligible electron tunnelling would occur at the dielectric thickness in exceeding 2 *nm*, the ε_r of the composite ALD MgO/SL film was calculated using the total thickness of the ALD MgO and the ALD Al_2O_3 SL.

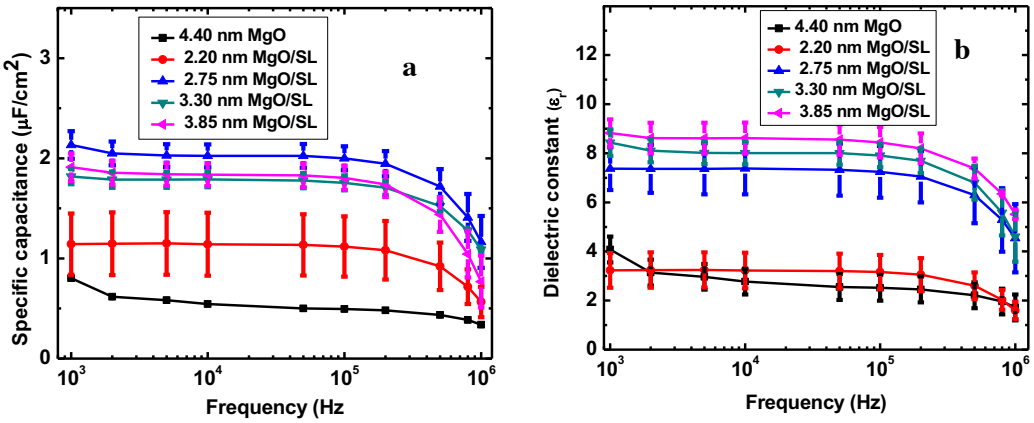

Figure 4.4 Variation of a) Specific capacitance and b) dielectric constant with frequency for Al/MgO(2.20-3.85 nm)/SL (0.55 nm)/Al and Al/MgO (4.40) nm /Al MIM capacitor using previous shadow mask method.

Figure 4.5(a) shows the variation of ε_r with the ALD cycle number for ALD MgO/SL at 1, 10, and 100 KHz. In the frequency range of 1-100 KHz, the ε_r values are comparable within 4-6 % of variation, and they increase monotonically with the cycle number (or thickness) of the ALD MgO. At 30-45 C (or thicknesses of 3.30-4.95 *nm* including the SL), ε_r values of ~8.82-9.38 have been obtained on the ALD MgO/SL. To the best of our knowledge, this is the first time such a high ε_r approaching to the single-crystal MgO's value is obtained in ultrathin ALD MgO films. The effective oxide thickness, or EOT=$t_{HiK}\cdot 3.90/\varepsilon_{Hik}$ used for evaluating high-K dielectric materials where t_{HiK} and ε_{Hik} are the thickness and ε_r of the high-K dielectric materials, for the ALD MgO/SL is estimated to be ~1.45-2.05 *nm*. This suggests that the EOT of the ultrathin ALD MgO/SL films are around 1.1-0.95 *nm* that is comparable to that for high-K HfO_2 of 3-4.5 *nm* in thickness and ε_{Hik} in the range of 10-18.5 [11, 12, 127].

Figure 4.5(b) shows a direct comparison of the ε_r values of the ALD Al_2O_3, ALD MgO/SL and ALD MgO ultrathin films, illustrating a similar monotonic increasing trend with increasing ALD cycle numbers. At the optimal fabrication condition reducing IL to negligible thickness, ε_r remains constant around 8.90-9.00 for 3.30-4.40 *nm* thick ALD Al_2O_3 films, which is comparable to the value for the Al_2O_3 single crystal[82] and is more than double of the best (ε_r~4.0) previously reported on 3.00 *nm* thick Al_2O_3 films [71]. The reduced ε_r values at smaller thickness are ascribed to the electron tunnelling through the ALD Al_2O_3 as reported in our previous work [16]. A similar thickness dependent trend on ALD MgO/SL with ε_r values ~8.82- 9.38 for 3.30-4.95 *nm* and reduced ε_r values at smaller thicknesses have been observed. Also, the ε_r values measured on two ALD MgO samples of 4.40 *nm* (cyan) are also included for the comparison. However, 4.40 *nm* ALD MgO show significantly lower ε_r ~3.55-4.60 is indicative of the formation of defective dielectric IL between the M-I interface with a possibility of non-uniform nucleation, which agrees with our detailed discussion later with STS. This argument agrees with previously reported results that MgO dielectric is expected to have more defects and pinholes compared to Al_2O_3 [113, 114], suggesting the possibility of a different growth mechanism for MgO. A similar trend is shown in the ε_r of the ALD MgO/SL samples (blue) indicating that the defect concentration has been significantly reduced with the adoption of the SL.

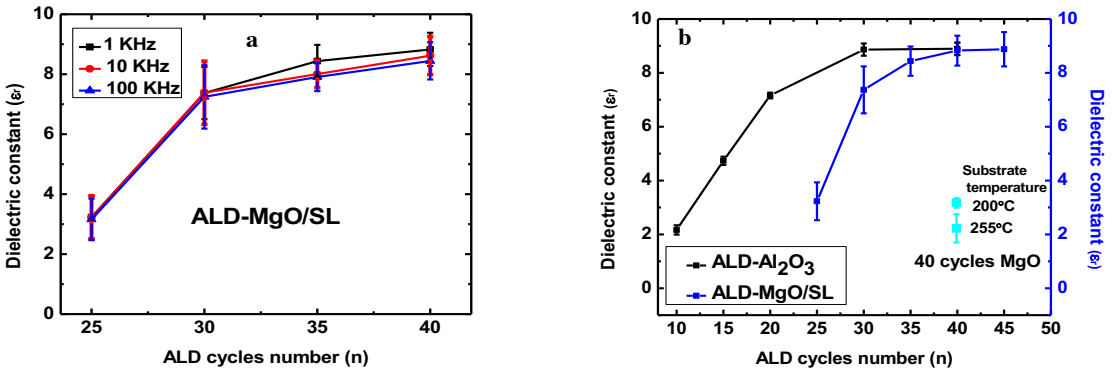

Figure 4.5 Variation of a) dielectric constant for ALD MgO/SL with ALD cycles number at different frequencies (1, 10 and 100 KHz) and b) Comparison of ALD Al2O3 dielectric (black) reported in a previous paper1 with ALD MgO with SL (ALD MgO/SL) (blue) and ALD MgO wo-SL) (cyan) deposited at substrate temperature 200 and 255 °C.

It should be mentioned that the ALD MgO and ALD Al_2O_3 films deposited at low temperatures of ~200-220 °C are amorphous [68], which means that TEM diffraction can be obtained on them and their interfaces with the metal electrode with an atomic resolution. To address this challenge, we recently implemented an ultrahigh vacuum scanning tunnelling spectroscopy (STS) to *in situ* study of the morphology and the electronic structure of the ultrathin ALD dielectric films with the thickness in the range of 0.1-1.0 *nm*. To complement the *in situ* STS measurement, devices of tunnel junctions and MIM trilayers (like the ones reported in this work) have also been fabricated to characterize the ALD dielectric films using electric transport measurement by Ryan *et al* [122]. The agreement between the *in situ* STS and transport measurements on these devices can be found in our previous works.

In an attempt to further understand the role of Al_2O_3 SL, Figure 4.6(a) shows schematic of an *in situ* STS analysis carried out on TBs with a combination of 10 ALD cycles (10 C) of: Al_2O_3 (10

C), Al_2O_3 (5 C) + MgO (5 C), and MgO (10 C). The 5C Al_2O_3/5C MgO and 10 C Al_2O_3 were found to have nearly identical E_b ~1.50 eV as in Figure 4.6(b) representing TBs with excellent quality on both samples. This is in drastic contrast to the 10 C MgO grown directly on the Al wetting layer resulting in a poor E_b ~0.80 eV. These results illustrate the importance of SL to obtain high quality MgO dielectric. This difference may be observed by viewing Figures 4.6(c) and 4.6(d) which illustrate the difference in *dI/dV* spectra between the higher quality Al_2O_3/MgO and lower quality MgO barriers. The lower E_b is due to defects present in the TB, these defects became more obvious while probing the surface since approximately 20% of the spectra were conductive or defective and the rest showed relatively low E_b. Furthermore, at other locations on the surface, there was too much noise for the scanning tip to even settle to take *dI/dV* spectra. During ALD MgO growth without a SL, a complete layer of MgO is not grown, and what is grown is of lower quality due to defects.

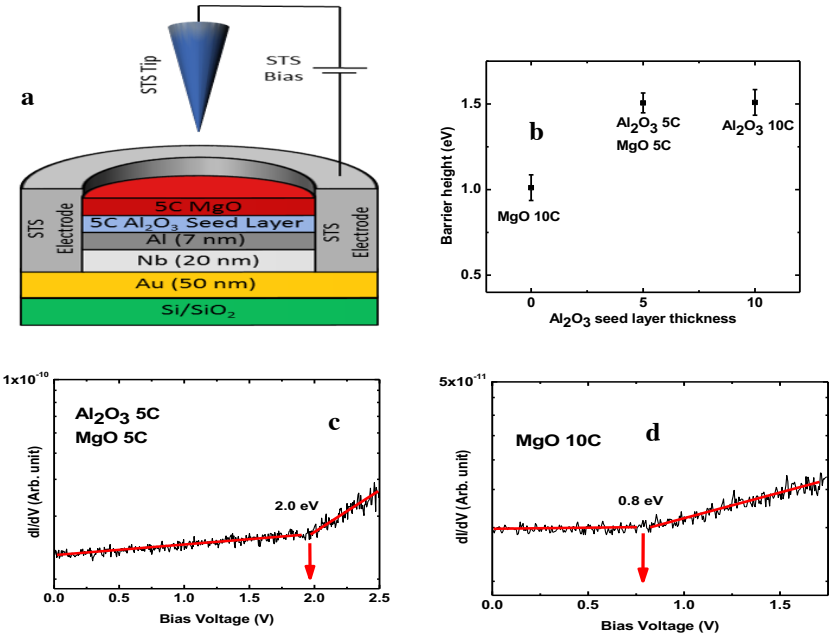

Figure 4.6 a) Diagram of *in situ* deposited seed layer and TB for STS analysis b) Comparison of barrier heights for TBs of total thickness 10 C using different amounts of Al_2O_3 in their compositions. c) representative *dI/dV* spectrum taken on a 5 C Al_2O_3/5 C MgO TB and d) a representative *dI/dV* spectrum taken on a 10 C MgO TB.

4.5 Effect of Interface on Leakage Current

The proposed ALD MgO nucleation mechanism enabled by the SL is supported by a comparison of *J* measured on MIM capacitors with an "I" layer of 4.40 *nm* thick ALD Al_2O_3, ALD MgO/SL and ALD MgO/WoSL respectively (Figure 4.7). This result indicates that the $J \sim 10^{-7}$ A/cm^2 for the 4.40 *nm* ALD Al_2O_3 sample is the lowest among the three samples. The higher *J* values in the two ALD MgO samples may be ascribed to the higher defect concentrations in these samples as compared to that of ALD Al_2O_3. However, the implementation of a SL can effectively reduce the leakage by more than one order of magnitude than in the ALD MgO/WoSL. The ALD MgO growth on metals show a large incubation period is necessary for complete hydroxylation that

promotes the formation of native oxides on the metal surface [118-120]. We have attempted *in situ* ALD MgO growth on Al and Fe. But found the MIM structures are leaky even when the MgO film thickness is 4.4 *nm*. This is in contrast to high quality ALD Al_2O_3 ultrathin films of thickness as small as 0.1 *nm* on Al and Fe [14, 15]. To resolve this issue in ALD growth of MgO on metals, this work develops a seed-layer approach to bypass the difficulty of ALD MgO directly on metals. The ALD Al_2O_3 SL differs fundamentally from native oxides on metal surfaces. As we have shown in our previous work on the direct comparison between ALD Al_2O_3 and native AlO_x on Al surface [14] the former has a significantly reduced defect concentration.

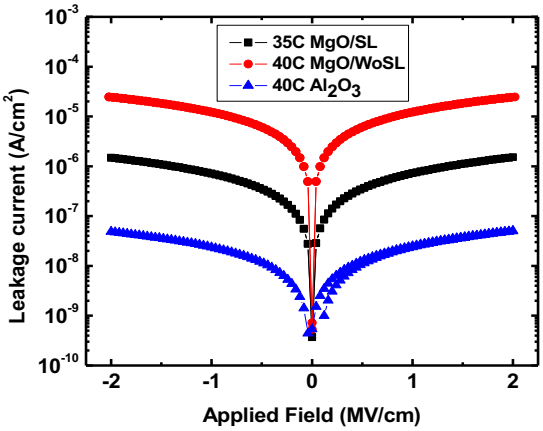

Figure 4.7 Comparison of leakage current for total 4.40 nm ultrathin ALD dielectric film with ALD Al_2O_3, ALD MgO/SL and ALD MgO/WoSL for MIM capacitor using log plot.

4.6 Chapter 4 Conclusion

In summary, an ALD Al_2O_3 SL of 0.55 *nm* in thickness has been employed to grow MIM devices with ultrathin ALD MgO dielectric films in thickness 2.20-4.40 *nm*. The goal is to address critical

the issue in the nucleation of ALD MgO directly on metals that are incompatible to form a sharp M-I interface. Our results indicate that the SL can convert such an incompatible metal surface to compatible by regulating the surface OH density/pattern, and hence facilitating high quality ALD MgO growth. The ALD MgO/SL films at 3.30-4.95 *nm* thickness exhibit ε_r ~8.82-9.40, approaching the ε_r ~9.80 of the single-crystal MgO. STS demonstrates the ALD MgO/SL with E_b~1.50 eV with almost 100% coverage. Also, our MD simulations indicate that ALD MgO/SL layer allows regularly distributed Al and OH ligands leading to the growth of denser and high quality MgO dielectric. In contrast, ALD MgO of comparable thickness is defective with low ε_r of 3.55-4.66 along with non-uniform nucleation on the Al surface with a significant portion of the Al surface remaining conductive as confirmed using the *in situ* STS. The reactive MD simulations on MgO growth directly on Al provides insights showing not self-terminating surface with rougher terrain for subsequent growth of a defective dielectric film. These results illustrate that the SL approach is promising to engineer otherwise incompatible M-I interface to enable *in situ* growth of MIM trilayers of ultrathin leak-free dielectric with low defect concentration required in a large variety of microelectronic and memory applications.

Chapter 5 Switching On/Off Negative Capacitance in Ultrathin Ferroelectric/Dielectric Capacitors

To keep up with Moore's Law, miniaturization of microelectronic devices demands the thickness of gate dielectric approaching ultrathin range in 1-2 *nm* thickness. Despite the significant progress made in ultrathin high-K gate dielectric of a few *nm* in thickness, further reduction of their thickness remains challenging due to the difficulties in controlling defects, which is similar to the SiO_2 dielectric case [26, 28]. A promising resolution of this issue is to stack a ferroelectric (FE) layer with the dielectric (DE) layer to make a FE/DE bilayer stack [128-136]. FE materials can have significantly higher ε_r values by a few orders of magnitude. More than that of SiO_2 or many other DE materials [137-139]. Using the FE gate alone remains difficult due to the hysteretic current-voltage characteristics and unstable negative capacitance as shown, for example, on the FE $Hf_{0.5}Zr_{0.5}O_2$ (HZO). These issues could be minimized in the FE/DE bilayer stacks on which the polarization switching at a low applied voltage leads to an efficient control of gate switching on/off, hence low-power operation taking advantages of the negative capacitance in the FE layer [128-136]. In a recent study of the HZO/Al_2O_3 FE/DE bilayers with fixed FE layer thickness of 20 *nm*, Si *et al* discovered that the DE layer thickness must be ≤ 4 *nm* in order to observe FE polarization switching [140]. When the DE thickness exceeds 4 *nm*, they observed that the HZO/Al_2O_3 FE/DE stack behaves like a regular DE layer with no polarization switching and

transient negative capacitance[140]. This observation revealed the importance of the FE/DE interface on controlling the polarization switching in PE layer through a balance of the gate voltages across the FE and DE layers in the FE/DE bilayer stack [140, 141]. Another related study on FE $PbTiO_3$ nanodot capacitors with their radii of 2, 5 and 10 *nm* [142]. An interesting correlation between the nanodot radius and thickness was revealed from the observation of the static negative capacitance when the nanodots have comparable lateral and vertical dimensions [142].

In this chapter, a new approach for the fabrication of ultrathin FeO_x/Al_2O_3 FE/DE bilayer capacitors with total FE/DE stack thickness in range 3-4 *nm* using *in situ* ALD. FeO_x thin films exhibit a multiferroic behavior at RT [143-146]. The FE properties of the FeOx have been investigated for potential future technological applications such as fast-writing, power-saving, and non-destructive data storage [144-146]. High quality, ultrathin dielectric ALD Al_2O_3 of thickness as low as ~ 2.2 *nm* has been recently demonstrated in Al/ALD Al_2O_3/Al capacitors with high ε_r ~ 8.0 that is close to the Al_2O_3 bulk crystal value of ε_r~9.2 [16]. Using an Al wetting layer in the Fe/Al/ALD Al_2O_3 (2.2 *nm*)/Fe capacitors, we show a transition from a DE only capacitor at Al thickness in exceeding 1.0 *nm* to an FE/DE bilayer capacitor at smaller Al thickness to promote the formation of a sub-nanometer thick FeO_x at the Fe and ALD Al_2O_3 interface. This allows the observation of a transition from positive capacitance on DE only capacitors to negative capacitance on FE/DE bilayer capacitors. Furthermore, we show that switching on/off of the negative

capacitance can be achieved using the piezoelectric effect of the FE layer in the ultrathin FE/DE bilayer capacitors via application of external mechanical deformation.

5.1 Device Structure and Growth Mechanism

Figures 5.1(a) and (b) illustrate the schematic of the ultrathin capacitors of Nb (25 *nm*)/Fe (20 *nm*)/ALD Al_2O_3 (2.2 *nm*)/Al (7*nm* or 0 *nm*)/Fe (20 *nm*)/Nb (50 *nm*) structure with and without a 7 *nm* thick Al wetting layer respectively. With the 7 *nm* thick Al wetting layer, the bottom Fe electrode is protected from oxidation[17] and the interface between Al/Al_2O_3 has been found to have a negligible AlO_x interface at the optimal ALD growth condition as illustrated schematically in Figure 5.1(c) [14, 15]. When the Al wetting layer is removed, reduced E_b for ALD Al_2O_3 was observed, suggesting an IL may form at the Fe/Al_2O_3 interface, most likely through the formation of FeO_x as shown in Figure 5.1(d) [147]. Comparing to Al, Fe is a stronger oxygen getter, which means that FeO_x is more likely to form than AlO_x at a given dielectric growth condition. An Al wetting layer of thickness in greater than 1.0 *nm* seems adequate to prevent oxidation of Fe as illustrated with comparable to the optimal E_b ~1.55-1.66 eV of the ALD Al_2O_3 [147]. At smaller Al wetting layer thicknesses, the E_b shows monotonic decrease to 1.40 eV at ~ 1 *nm*-thick Al wetting layer on Fe and 1.30 eV when the Al wetting layer is completely removed. This trend can be attributed to the formation of a native FeO_x oxide IL at the Fe/ALD Al_2O_3 interface when the Al wetting layer is very thin or absent [14]. This means instead of forming a simple Al/Al_2O_3/Al DE capacitor (Figure 5.1(c)), a FE FeO_x capacitor is added to the Fe/FeO_x/ALD Al_2O_3/Fe

capacitors that can be viewed as two capacitors in series: a sub-*nm* thick FE FeO_x capacitor and a 2.2 *nm* thick DE ALD Al_2O_3 capacitor as depicted in Figures 5.1(b) and (d). It should be noted that small thicknesses of both FE and DE layers are critical to the observation of the negative capacitance in the obtained FeO_x/ALD Al_2O_3 FE/DE bilayer capacitors [140, 142, 148].

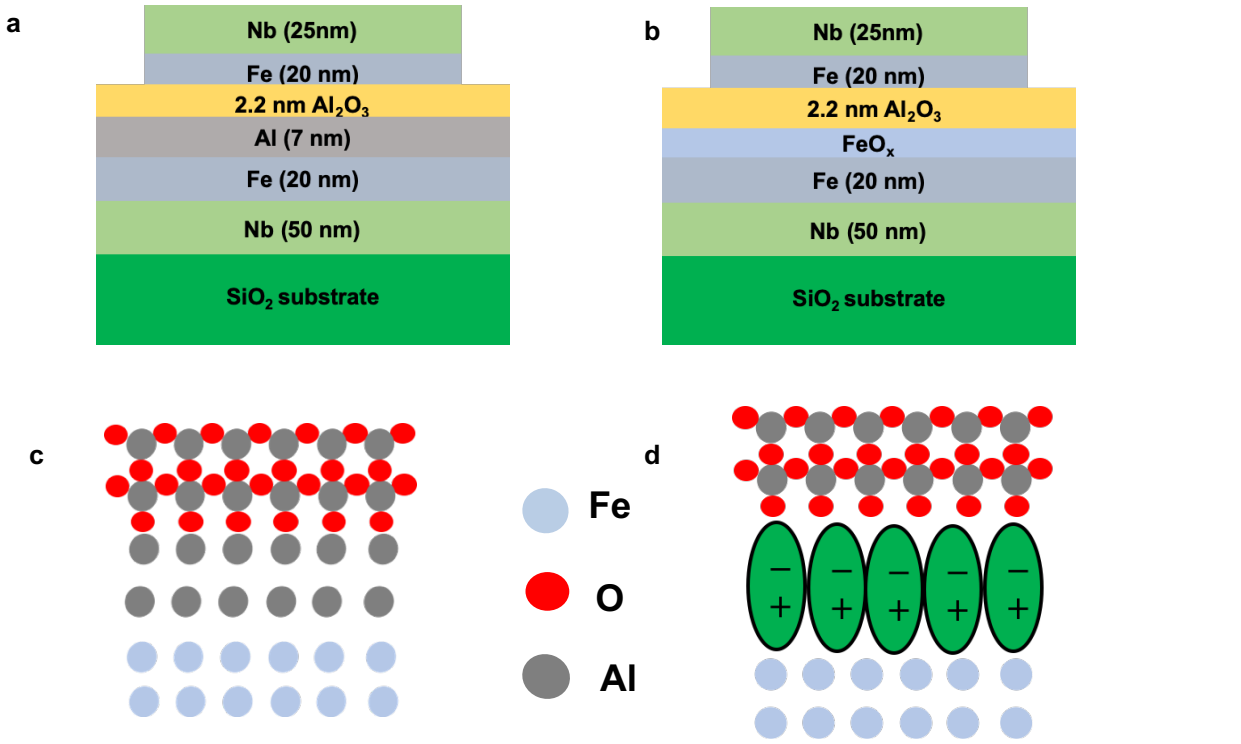

Figure 5.1 Schematic of the MIM capacitors with: a) a thick 7 nm Al wetting layer; and b) no Al wetting layer. The schematic description of the M-I interface for: c) ALD Al_2O_3/Al (7nm) with pure dielectric ALD Al_2O_3 and d) Al_2O_3/Fe with a ferroelectric FeOx interface in series with ALD Al_2O_3 dielectric layer.

5.2 Dielectric Properties by Tuning Al Wetting Layer Thickness

Figure 5.2(a) show a comparison of the specific capacitance ($C_0=C/A=\varepsilon_0\varepsilon_r/t$, where t is the thickness of dielectric) for the three sets of the ultrathin capacitors of Nb (25 *nm*)/Fe (20 *nm*)/ALD Al_2O_3 (2.2 *nm*)/Al (7*nm*, 1*nm* or 0 *nm*)/Fe (20 *nm*)/Nb (50 *nm*). Each set has three devices with junction areas of 200x200, 200x300 and 200x400 μm^2 respectively, for examination of the sample uniformity. The three samples would be otherwise identical except for different Al wetting layer thicknesses of 7 *nm* (black), 1 *nm* (red) and zero (blue). As shown in Figure 5.2(b), with a 7 *nm* thick Al wetting layer, the value of C_0 is around 0.032-0.04 F/m^2 on chip with uniformity of ~15%. This is an indication of negligible IL formation at the Al/ALD Al_2O_3 interface. However, with the reduction in Al wetting layer thickness to 1 *nm*, the value of C_0 decreases considerably to 0.021-0.016 F/m^2 on chip with variation ~23.8%. Interestingly, with the complete removal of the Al wetting layer, C_0 becomes negative in the range of -0.005 to -0.015 F/m^2. Figure 5.2(c) show ε_r derived from $\varepsilon_r=C_0t/\varepsilon_0$. The ultrathin capacitors with a 7.0 *nm* Al wetting layer show ε_r ~8.0 for 2.2 *nm* thick ALD Al_2O_3 dielectric layer that is close to that for the bulk crystalline Al_2O_3 with an EOT ~1.0 *nm*. This EOT value is comparable to the EOT for 4.5 *nm* high-K HfO_2 [73].

It should be noted that the observation of smaller and even negative ε_r on capacitors with 1 *nm* or none Al wetting layer cannot be attributed to the poorer quality of the ALD Al_2O_3 DE layer at thinner Al wetting layer based on our earlier investigation of the ALD Al_2O_3 tunnel barriers (thickness from 0.1 *nm*-1.0 *nm*) on the Fe electrodes including E_b ~ 1.3 eV and ALD Al_2O_3 coverage comparable to the counterparts with Al wetting layer. In other words, this suggest that

the leak-free ALD Al_2O_3 tunnel barriers can form on Fe electrode without the Al wetting layer. However, the slightly lower E_b ~ 1.3 eV, as compared to the optimal value of E_b~1.5-1.6 eV measured on ALD Al_2O_3 tunnel barriers on Al electrodes, suggests that a minor IL, most probably FeO_x due to the subtle effect of the surface structure of Fe on the hydroxylation during the first H_2O pulse, forms at the Fe/ALD Al_2O_3 interface [14, 15, 147]. While in many other devices, the native oxide IL is unfavourable, the ferroelectric FeO_x IL is formed at the Fe/ALD Al_2O_3 interface [14, 15, 147] provides an excellent opportunity to achieve ultrathin FE/DE bilayer capacitors connected in series of a total thickness smaller than 3-4 *nm*, allowing direct observation of the static negative capacitance [140, 142, 148]. This means the measured C_0 and ε_r on these ultrathin FE/DE bilayer capacitors must be considered as the combined effect of the constituent FE and DE capacitors.

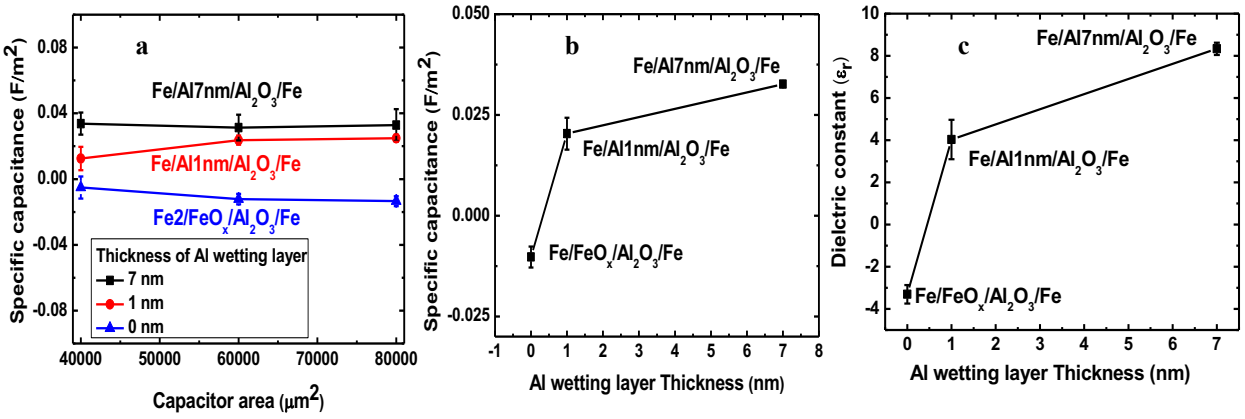

Figure 5.2 Variation of a) specific capacitance with three different junction areas 200x200, 200x300 and 200x400 μm2 b) specific capacitance with thick 7 nm Al wetting layer, thin 1 nm Al wetting layer and without Al wetting layer and c) dielectric constant (ε_r) for MIM capacitor for 20 cycles Al_2O_3 .

5.3 Mechanism for Observation of Negative Capacitance

Figure 5.3(a) illustrates the working principle of the ultrathin Fe/Al/ALD Al_2O_3/Fe pure DE capacitors under the application of an external electric field (E). The blue ovals represent electrical dipoles aligned in response to the external E field. Figure 5.3(b) shows the electrical dipoles in the Fe/FeO_x/ALD Al_2O_3/Fe FE/DE bilayer capacitors with coercive voltage (V_c) of few mV for polarization switching in FE material much smaller than total external applied external voltage (V_{tot}). At this ultrathin 2.2 *nm* thick ALD Al_2O_3 with ultrathin FE FeO_x, the presence of stable negative capacitance is possibly due to formation of regular, nanoscale stable domains with the same orientation of the electric polarization that makes the FE layers extremely polarizable as shown with the corresponding polarization (P_{FE}) under the application of E across the FE/DE stack. For ultrathin FE/DE capacitors the interfacial effects are more pronounced. Due to interfacial effect FE/DE stack capacitor fundamentally differ from the series combination of ferroelectric capacitance (C_{FE}) and dielectric capacitance ($C_{Al_2O_3}$) [149, 150]. Considering pure dielectric as in the case of Al/Al_2O_3/Al ultrathin capacitors, the stored charges in DE is $Q_{Al_2O_3}$. However, the FE layer shows polarization under externally applied field with $Q_{FE} = Q_P + Q_i$, where Q_P and Q_i corresponds to the polarized charges in FE material and induced or interfacial trapped charges respectively. For a simple approximation, the Fe/FeO_x/ALD Al_2O_3/Fe ultrathin capacitors can be considered as the two capacitors in series: DE ALD Al_2O_3 capacitor and FE FeO_x capacitor, which can be estimated using $\frac{1}{C_T} = \frac{1}{C_{Al_2O_3}} + \frac{1}{C_{FE}}$, where C_T is the total capacitance of FE/DE stack. With observe value of $C_{Al_2O_3} \sim 0.04$ F/m^2 and $C_T \sim -0.015$ F/m^2, the C_{FE} is estimated

to be~-0.010 F/m^2, which is one fourth C_{FE} but with opposite polarization. Thus, the thickness of FE (t_{FE}) is approximated from equation $t_{FE}=\varepsilon_0\varepsilon_r/C_0$ ~ 0.88-1.77 *nm* corresponding to $\varepsilon_{r,FE} \sim -1$ to -2. This indicates that the total thickness of FE/DE stack varies from 3-4 *nm*, which is ultrathin as compared to previous studies [140, 148]. However, at this ultrathin DE thickness of ~2.2 *nm* in presence of a FE layer in the FE/DE bilayer stack, there is the possibility of a leakage current due to the trapped charges at the FE/DE interface. Figure 5.3(c) shows the increase in the polarization of FE under the application of an external electric field or via external mechanical deformation in FE/DE bilayer capacitors. The induced charged at FE/DE interface Q_i add to Q_P that increases the total polarization charges ofQ_{FE}. The increase in the polarization of FE corresponds with the decrease in DE contribution resulting in stable negative capacitance. Figure 5.3(d) shows leakage current assisted polarization switching behavior in FE/DE capacitors with polarization switching effect, which is in agreement with the previous study on HZO/Al_2O_3 FE/DE structure [140, 148]. DE material thickness has the determinant impact on the FE polarization switching effect, at DE thickness > 4 *nm*, HZO/Al_2O_3 stack behaves like pure DE insulator with no polarization switching of HZO [140]. However, at ultrathin DE thickness < 4 *nm* HZO/Al_2O_3 stack exhibit FE effect with stable and switchable electrical polarization resulting negative capacitance [140, 142].

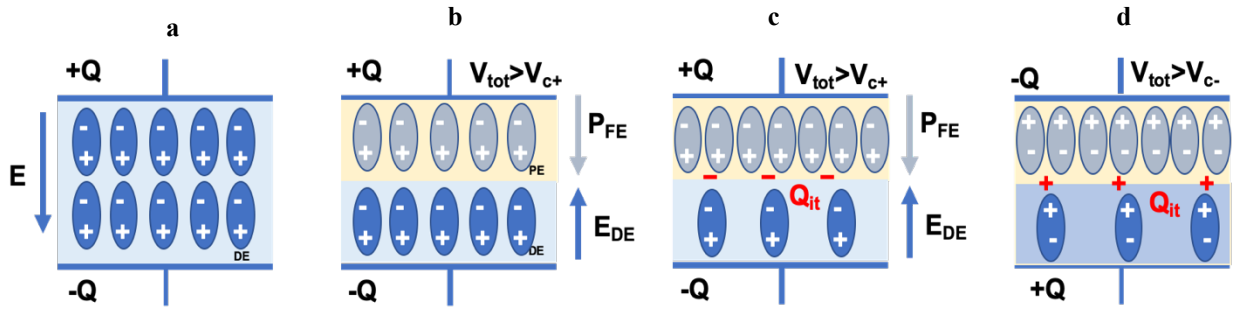

Figure 5.3 Working principle of a) Fe/Al/FeO_x/Al_2O_3/Fe dielectric (DE) capacitor under application of external electric field i.e. blue ovals represent electrical dipoles aligned under E field b) Fe/Al/FeO_x/Al_2O_3/Fe Ferroelectric/dielectric (FE/DE) bilayer capacitor with blue and light blue ovals represent electrical dipoles and polarization in aligned under E field at $V_{tot} > V_{c+}$ before switching ; c) Increase in FE capacitance due to external E field or via external deformation leading to increase in interfacial charges at FE/DE interface at $V_{tot} > V_{c+}$ after switching d) Leakage current assisted polarization switching with change in interfacial charges in FE/DE bilayer capacitors $V_{tot} > V_{c-}$ after switching.

5.4 Dynamic Response Under External Force

Since all ferroelectric materials are piezoelectric, the response of FE/DE stack with FE FeO_x would provide an interesting application for memory and sensors devices through the manipulation of electric dipoles [151]. Figure 5.4 shows the variation of specific capacitance with and without external deformation on the FE/DE stack. Before external deformation total capacitance is dominated by the series combination of FE and DE capacitance in FE/DE capacitors resulting negative capacitance (black) as shown in Figure 5.4(a). However, after the application of an external force in FE/DE capacitors, the contribution from DE remains the same but there is an increase in the FE capacitance due to the piezoelectric effect showing an increase in polarized charges at FE/DE interface. This results in the corresponding reduction in total negative

capacitance (red) for a series combination of FE/DE stack. The further increase in the external force makes the total capacitance to be small at positive value (blue). Quantitatively, this changes in capacitance under the external deformation is the manifestation of the change in polarization switching behavior in ultrathin FE/DE capacitors. Figure 5.4(b) shows the dynamic reproducible polarization switching on/off of negative capacitance in FE/DE ultrathin capacitors corresponding to before/after the external deformation by the application of external force. This indicates that the capacitance can be tuned with the external force, which would find potential application in non-volatile memory and piezoelectric force sensors application through the manipulation of the electric dipoles in FE/DE ultrathin capacitors.

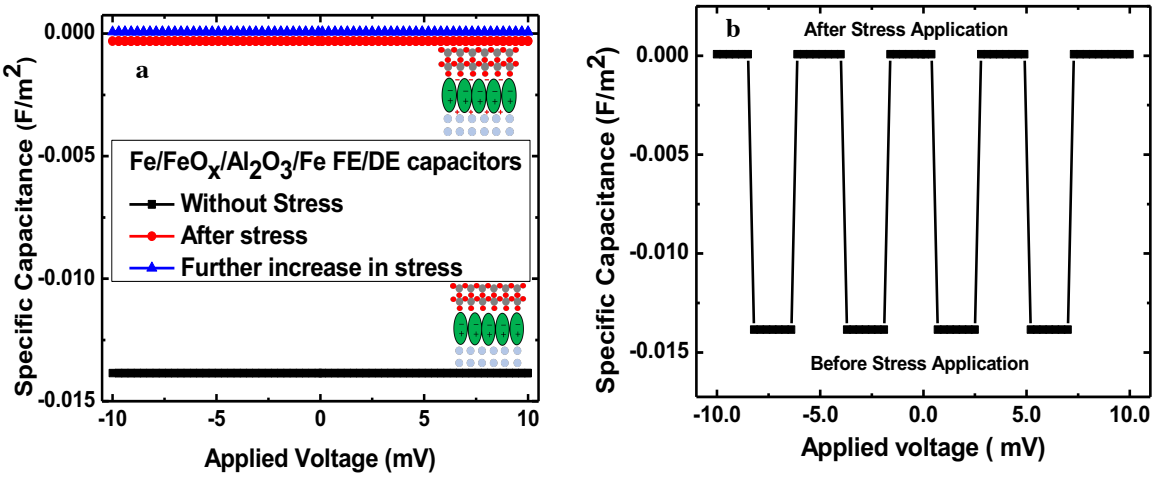

Figure 5.4 a) Comparison of C-V curve for MIM capacitor without Al wetting layer as measured and under the application of external force showing change in capacitance and b) dynamic response curve for MIM capacitor before and after application of external force.

5.5 Properties of FE/DE Stack

To validate the presence of the FeO_x IL in ultrathin FE/DE capacitors, Figure 5.5 shows the dependence of E_b on the Al wetting layer using ALD Al_2O_3/Al (7nm, 1nm or 0)/Fe (20 nm)/Nb (50 nm) half-cell structure studied using STS by Ryan *et al*. Our previous STS study suggest that compared to Al, Fe is a stronger oxygen getter, which means the oxidation of Fe forming FeO_x is more likely than AlO_x at a given ALD Al_2O_3 growth condition [147]. The Al wetting layer greater than 1 nm can result in negligible AlO_x and can prevent the oxidation of Fe with E_b ~1.55-1.66 eV for 5-cycles ALD Al_2O_3 on Fe [147] However, 1nm-thick Al wetting layer there is monotonic decrease in E_b to 1.40 eV and 1.30 eV when Al wetting layer is completely removed. This trend can be attributed to the formation of a native FeO_x oxide interface layer at the Fe/ALD Al_2O_3 interface when the Al wetting layer is very thin or absent [14, 147]. Specifically, the presence of FeO_x IL affects the E_b of ALD Al_2O_3 in a similar way to the native AlO_x case.[14] The dependence of E_b on Al wetting gives insight into the E_b for both pure Al/Al_2O_3/Al capacitor and FE/DE bilayer Fe/FeO_x/Al_2O_3/Fe structure. However, decreasing trend in E_b with Al wetting layer thickness confirms our assumption for the formation of IL FeO_x resulting FE/DE stack.

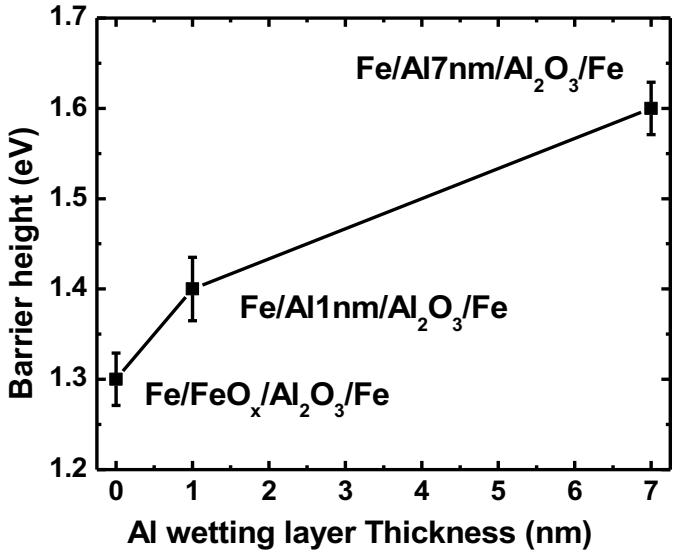

Figure 5.5 Barrier height comparison for MIM half-cell made for three different configurations with different thickness of Al wetting layer made using scanning tunnelling spectroscopy.

A series of I-V measurement were used to extract further information about properties of ultrathin FE/DE capacitors. Figure 5.6 provides two important pieces of information: 1) hysteretic I-V loop for ultrathin FE/DE capacitors show a strong evidence for the formation of FeO_x IL with ferroelectric polarization switching behavior at ultralow applied voltage of a few mV and 2) linear I-V for 2.2 *nm* DE devices showing quantum tunnelling behavior. This observation shows that a key tuning parameter in generating the FE/DE bilayer capacitors is the thickness of an Al wetting layer between the bottom Fe electrode and the ALD Al_2O_3 DE layer. This work demonstrates the feasibility of successful fabrication and characterization of $Fe/FeO_x/Al_2O_3/Fe$ FE/DE ultrathin capacitors using *in situ* ALD method. This observation of static negative capacitance with FE/DE ultrathin capacitors finds potential application for lowering switching energy of transistor and

power dissipation with the possibility for ultralow power devices [128-132], piezoelectric sensors and non-volatile memory applications [144-146].

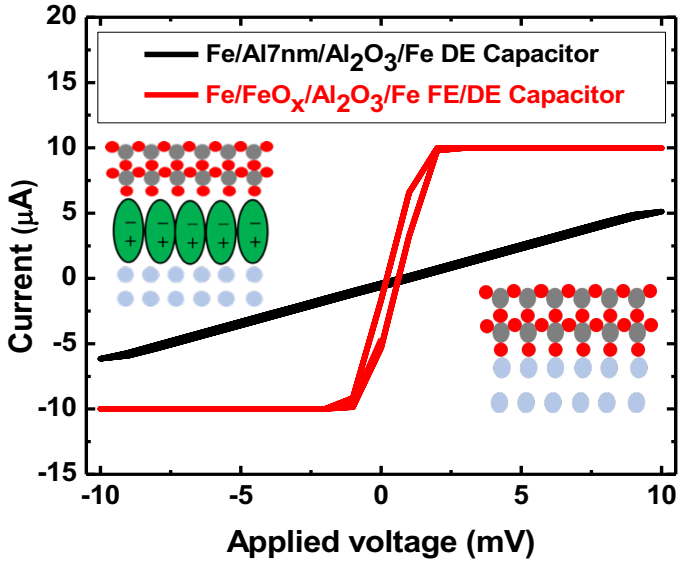

Figure 5.6 Comparison of I-V curve between MIM with 7 nm Al Fe/Al/Al_2O_3/Fe DE and without Al wetting layer Fe/FeO_x/Al_2O_3/Fe FE/DE.

5.6 Chapter 5 Conclusions

In summary, *in situ* ALD provides a unique approach to fabricate high quality ultrathin capacitors and has been applied for the first time in this work to generate FE/DE bilayer capacitors with a total FE/DE thickness < 3-4 *nm*. Specifically, the capacitors consist of a Nb (25 *nm*)/Fe (20 *nm*)/ALD Al_2O_3 (2.2 *nm*)/Al (7*nm*, 1*nm* or 0 *nm*)/Fe (20 *nm*)/Nb (50 *nm*) stack and the Al wetting layer was employed as the tuning mechanism to obtain either DE only capacitors at the Al thickness >1 *nm* and FE/DE bilayer capacitors at thinner or none Al wetting layers. The obtained

DE only capacitors exhibit high ε_r ~8.0, which represents the best so far achieved on ultrathin capacitors of DE thickness around 2 *nm*. This value is close to the Al_2O_3 bulk single crystal value of ε_r ~9.2. Interestingly, a sub-*nm* thick FeO_x FE layer can form on the surface of the Fe bottle electrode when the Al wetting layer is thinner or completely removed. This could be attributed to the minor interaction of the first ALD H_2O pulse with Fe surface through partial dissociations of the H_2O monolayer into atomic oxygen. The obtained FE/DE bilayer capacitors show a dynamic switching on/off of the negative capacitance that can be achieved under the application of an external force. This result not only provides a viable approach for generating ultrathin FE/DE bilayer capacitors but also offers a promising solution to low-power consumption microelectronics and piezoelectric sensors applications.

Chapter 6 High Tunnelling Magnetoresistance in Magnetic Tunnel Junctions with Sub-nm thick Al_2O_3 Tunnel Barriers Fabricated Using Atomic Layer Deposition

MTJs formed by sandwiching an ultrathin insulating barrier between two FM electrodes are the subject of an intensive research recently due to their potential applications in spintronics such as non-volatile MRAM and logic devices [33-35]. The figure-of-merit TMR of MTJs depends critically on the quality of the insulating TB and the M-I Interface becomes more challenging at sub-*nm* dielectric thickness range. Specifically, the spin tunnelling current decays exponentially with the TB thickness, which means a stronger coherent tunnelling is anticipated at a smaller TB thickness. It should be noted that the presence of defects in the TB can lead to decoherence of the spin tunnelling, not to mention an increased leakage current. Therefore, research and development of sub-*nm* thick TBs that are pinhole free and defect-free is important to achieving high-performance MTJs.

PVD, including magnetron sputtering and molecular beam epitaxy, has been widely adopted for MTJ fabrication with both amorphous AlO_x and epitaxial MgO TBs. The former can be obtained via thermal oxidation of ultrathin Al film on FM electrode in air or in oxygen [46, 47, 152] to allow

controlled oxygen diffusion into the Al to form AlO_x TBs. The best TMR~70 % at RT has been reported on MTJs with thermal AlO_x TBs. The advantage of the thermal AlO_x TBs is in the simplicity of the fabrication process and large-area uniformity due to the amorphous nature of the AlO_x. However, the thermal AlO_x TBs suffers several drawbacks including defects such as oxygen vacancies that are nonuniform through the TB thickness and can lead to soft dielectric breakdown along with high leakage current especially at sub-*nm* thicknesses [153-155]. The epitaxial MgO TBs, obtained through post annealing of MTJs at ~350-500℃, have advantages of enhanced coherent spin current tunnelling, which leads to enhanced TMR ~200-350 % at RT [4, 9, 156-159]. However, challenges remain in achieving high yield due to presence of defects including grain boundaries and oxygen vacancies in epitaxial MgO TBs, especially when the TB thickness is approaching 1 *nm* or smaller. Defects such as oxygen vacancies in both AlO_x and MgO TBs are common and difficult to avoid in oxides fabricated using PVD process. In addition, grain boundaries can easily form in epitaxial MgO TBs during recrystallization in the post annealing process and can serve as leakage channels in MTJs. To efficiently control the performance of MTJ devices the optimization of FM electrode for its composition, crystallinity and oxidation along with the quality of interface [45, 160-163] is crucial demanding the smooth and conformal TB with better FM-insulator interface [164, 165].

As discussed in Chapter 2, ALD provides a promising alternative for the fabrication of ultrathin leak-free and defect-free TBs. This can be attributed to the unique advantages the ALD techniques over the PVD approach [67, 68]. First of all, ALD is a chemical vapor deposition process that relies on well-defined chemical reactions, which occur only at the sample surface via a ligand

exchange between monolayers of the precursors. This minimizes the formation of defects such as oxygen vacancies in oxides. Secondly, ALD growth is self-limiting, enabling atomic control of the TB thickness [68]. Finally, ALD coating is conformal, [69, 70] which is important in obtaining pinhole-free ultrathin TBs over structured surfaces [166]. This has motivated researches recently in ALD growth of TBs of Al_2O_3, MgO and HfO_2 for MTJs [107, 167, 168]. However, it has been found that the thickness of the TBs obtained using *ex situ* ALD process is typically in the range of 2-5 *nm* to avoid leakage current. The TMR values reported on the MTJs with the ALD TBs are in the range of 1-20 % at RT, which is anticipated from the large thickness of these TBs [107, 109, 167-169]. The challenge in achieving thinner ALD TBs is primarily associated to the formation of a native oxide interface between FM electrode and the ALD TB due to exposure of the FM electrode to air or other gases in the *ex situ* ALD processes, which is more stronger oxygen getter compared to other metal electrode.

In this chapter, we explore the fabrication of ALD Al_2O_3 TBs using an *in situ* ALD process developed recently in our lab [14, 15, 147]. MTJs based on a simple Fe/ALD Al_2O_3/Fe structure was employed as a proof of concept in this study and the ALD Al_2O_3 TB thickness was selected to be 0.55 *nm* and 1.1 *nm*. In order to probe the nucleation effect of the ALD Al_2O_3 TBs, two sets of devices were compared: one with and the other without a 1 *nm* thick Al wetting layer on the bottom Fe electrode using both *in situ* STS and *ex situ* transport measurement. Remarkably, TMR of 77% was demonstrated on Fe/ALD Al_2O_3/Fe MTJs with an ALD Al_2O_3 TB of 0.55 *nm* in thickness. In the following, we will report our experimental results to successfully demonstrate

fabrication of Fe/ALD Al_2O_3/Fe MTJs with 0.55 *nm* ALD Al_2O_3 TBs for potential application in future MRAM devices [9, 46, 152, 156, 157].

6.1 Optimization of Multilayer Thin Films Structure

Figure 6.1(a) show the M-H loops measured on several samples including Fe (50 *nm*), Fe (50 *nm*)/Al (7 *nm*), Nb (50 *nm*)/Fe (50 *nm*) and Nb (50 *nm*) /Fe (50 *nm*)/Al (7 *nm*) fabricated using *in situ* DC sputtering. An overall improvement in saturated magnetization of the multi-layered samples as compared to the single-layered Fe ones is most likely due to the prevention of Fe from oxidation to form non-magnetic FeO_x by the capping layers of Nb or/and Al. Based on the literature, negligible intermetallic formation between Nb/Fe or Fe/Al structure is anticipated [170, 171]. Figure 6.1(b) show the M-H loops of two each of 50 *nm* (black and red) and 5 *nm* (purple and blue) thick Fe films and the overlap of the M-H loops for the samples of the same thickness illustrates reliable reproducibility from run to run. Based on the M-H loops, the coercive field of about 52 Oersted and 20 Oersted, respectively, can be estimated for the 50 *nm* and 5 *nm* thick Fe films. Thus, thicker Fe film serves as the fixed layer while the thinner one, the free layer in the MTJs of this work.

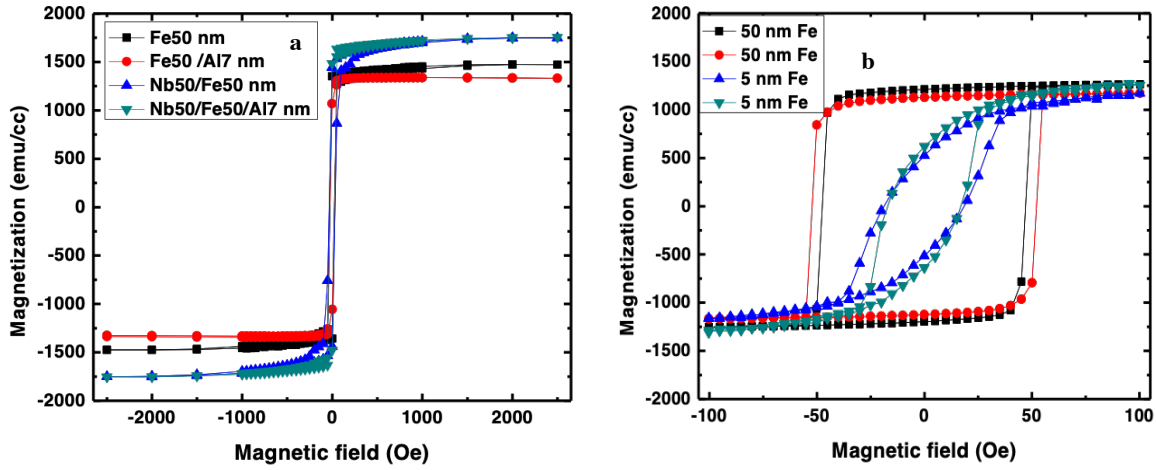

Figure 6.1 Magnetization vs magnetic field (M-H) loop for multi-layered structure with a) Fe (50 nm), Fe (50 nm)/Al (7 nm), Nb (50 nm)/Fe (50 nm) and Nb (50 nm) /Fe (50 nm)/Al (7 nm) b) M-H loop for Fe (50 nm) and Fe (5 nm) showing the coercive field dependent on the Fe film thickness.

Figure 6.2 exhibits representative AFM images taken on three thin film samples: Fe (50 *nm*), Nb (50 *nm*)/Fe (50 *nm*), and Nb (50 *nm*)/Fe (50 *nm*)/Al (7 *nm*). Overall, all three samples have very smooth surface that are featureless over the AFM scan area of 5x5 μm^2. In fact, the similar AFM scans were performed on different locations of these samples to ensure uniformity. The surface roughness (R_a) calculated based on the AFM images are 0.90±0.05 *nm*, 0.85±0.05 *nm* and 0.82±0.05 *nm*, respectively, on the Fe (50 *nm*), Nb (50 *nm*)/Fe (50 *nm*), and Nb (50 *nm*)/Fe (50 *nm*)/Al (7 *nm*) samples. The low R_a values on each of the three layers of the bottom electrode for the MTJs has confirmed an ideal smooth surface of the metal electrode for growth of the ALD Al_2O_3 TBs.

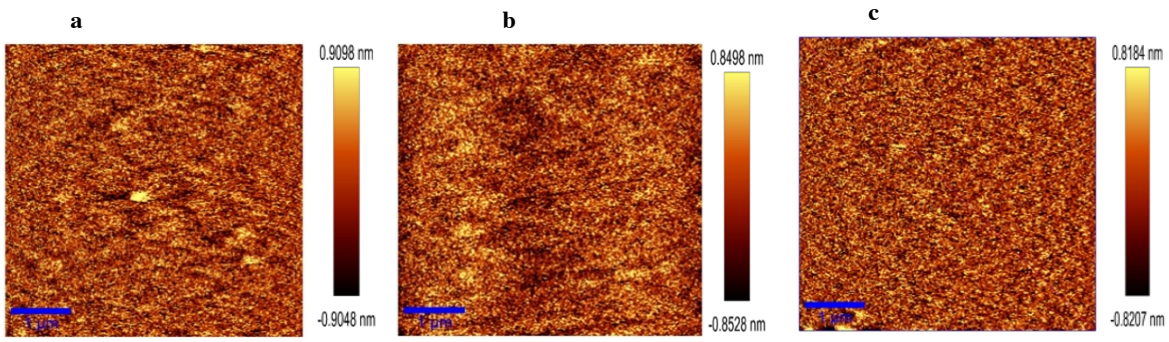

Figure 6.2 AFM images of a) Fe (50 nm), b) Nb (50 nm)/Fe (50 nm), and c) Nb (50 nm)/Fe (50 nm)/Al (7 nm) thin films deposited on SiO2. The scale bar is 1.0 μm.

6.2 MTJs Device Structures

Figure 6.3 shows schematically the two device structures of the MTJs investigated in this work: one with (Figure 6.3(a)), and the other, without (Figure 6.3(b)) a 1 *nm* thick Al wetting layer on top of the bottom Fe electrode. The Al wetting layer has been found to allow better nucleation of the ALD Al_2O_3 TBs with a negligible defective metal-insulator interface [147]. Considering ALD is a chemical process, the improved nucleation of the ALD Al_2O_3 TBs on the metal surface can lead to improved TB quality, especially the defect concentration that affects the ALD Al_2O_3 TB's height, and dielectric breakdown [14, 15]. However, the presence of a non-ferromagnetic layer of Al between the two ferromagnetic Fe electrodes is undesirable since it reduces the coherent spin tunnelling through the MTJ. Therefore, the Al wetting layer thickness was controlled to be around 1 *nm* for a comparison of the MTJ performance of with and without such a wetting layer.

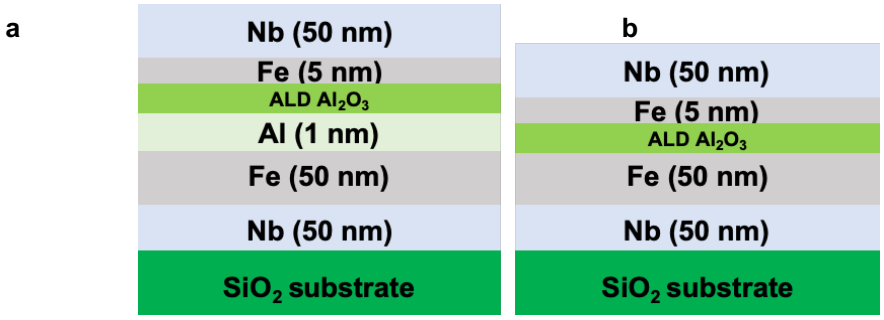

Figure 6.3 Schematic for the device structure for MTJs fabrication a) with 1 nm Al wetting layer and b) without Al wetting layer.

6.3 Characterization of MTJ Devices

Figure 6.4 compares a representative STS *dI/dV* spectra taken on 5 cycles (or 0.55 *nm* thick) ALD Al_2O_3 TBs with (Figure 6.4(a)) and without (Figure 6.4(b)) the 1 *nm* thick Al wetting layer on Fe bottom electrode, or the half cells of the two kinds of MTJs by Ryan *et al* as shown in Figure 6.3. The *dI/dV* spectra on the two devices show qualitatively similar characteristics of a dielectric TB, indicating that the ALD Al_2O_3 TBs can form on both surfaces of the Al and Fe. However, quantitative differences are clearly visible especially on values of the E_b's. Specifically, the $E_b \sim 1.40\ eV$ observed on the ALD Al_2O_3 TB with the Al wetting layer in Figure 6.4(a) is higher than the $E_b \sim 1.33\ eV$ directly on Fe (Figure 6.4(b)), indicating a higher defect concentration in the latter [14, 15, 147]. This may be attributed to the formation of an IL of FeO_x between the Fe and ALD Al_2O_3 TBs due to the less dense Fe atoms on the surface of the Fe as compared to the Al atom density on the Al surface [147]. The larger inter-atom distance on the Fe surface as compared to the Al surface would lead to more difficult hydroxylation of the Fe surface during the first H_2O

pulse of the ALD Al_2O_3 growth. When a partial decomposition of the H_2O to oxygen and hydrogen occurs, instead of to hydroxyl groups (OH^{-1}) on the metal surface, formation of defective FeO_x IL may form. The ultrathin ALD Al_2O_3 TBs grown on the defective native oxide IL would be defective, which explains the reduced E_b of the ALD Al_2O_3 TB on Fe as compared to that on Al. Nevertheless, the $E_b \sim 1.33\ eV$ on the ALD Al_2O_3 TBs of 0.55 *nm* in thickness on Fe is only 5% lower than that on Al. This means the effect of the FeO_x IL is insignificant. In addition, the $E_b \sim 1.33\ eV$ of the 0.55 *nm* thick ALD Al_2O_3 TB on Fe is significantly better than the low E_b ~ 0.3- 0.6 eV for thermal TB based devices [152, 154, 172]. This suggests that the defect concentration in ALD Al_2O_3 TBs is much reduced as compared to the thermal AlO_x TB case. The argument is further supported by the significantly lower leakage current and harder dielectric breakdown observed in the former in contrast to the latter [14, 15, 147].

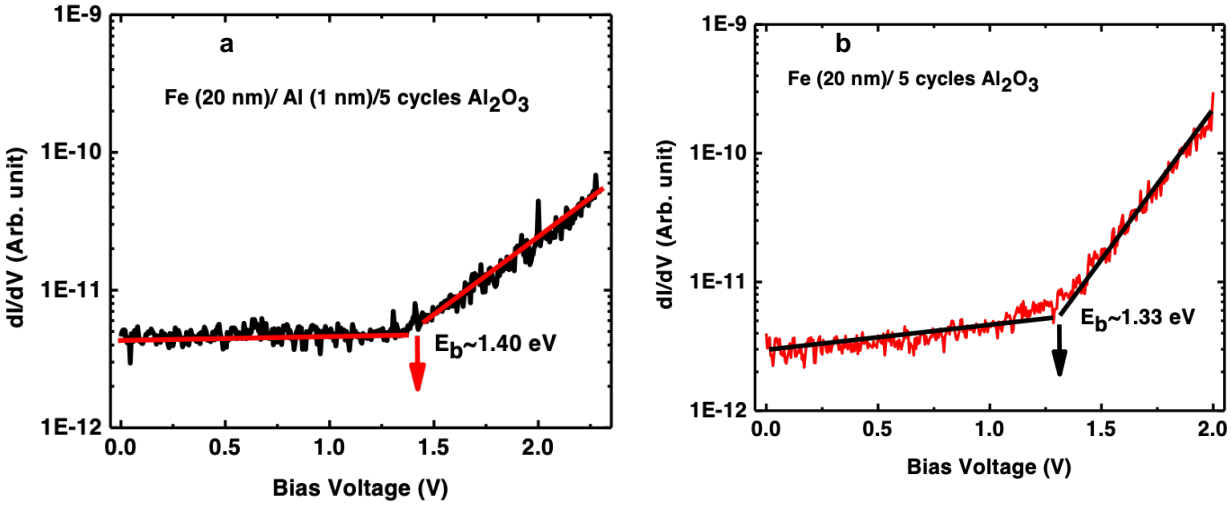

Figure 6.4 Scanning tunnelling spectroscopy to study *dI/dV* spectra for 5C-ALD Al_2O_3 a) with 1 nm Al wetting layer and b) without Al wetting layer.

Figure 6.5 shows the RA vs. H hysteresis loops measured at 100 K and 300 K on the two representative Nb/Fe (50 *nm*)/ALD Al_2O_3 /Fe (5 *nm*)/Nb MTJs with an 1 *nm* thick Al wetting layer (Figures 6.5(a)-(b)) and without (Figures 6.5(c)-(d)), respectively, at 300 K (RT) and 100 K. The observed hysteretic behavior on both samples is anticipated for MTJs due to the switching of the magnetic moments in the free Fe layer (top Fe electrode) between parallel to anti-parallel orientations with respect to that in the pinned Fe layer (bottom Fe electrode) as the applied H field exceeds the coercive field of the free layer. The TMR values can be calculated from the R-H loops are 4.25 % and 4.26 % at 300 K and 100 K, as in Figures 6.5(a)-(b) respectively, for the MTJ with the 1 *nm* thick Al wetting layer. These low TMR values indicate that the presence of the non-ferromagnetic Al wetting layer, even at the 1 *nm* thickness, between the two Fe electrodes is undesirable. Since it behaves like a barrier that could significantly reduce the coherent spin tunnelling. When the Al wetting layer is removed, significantly higher TMR ~77 % at 300 K and

~90 % at 100 K, respectively, are obtained on the counterpart MTJ without Al wetting layer as shown in Figures 6.5(c)-(d). The current state-of-the art MTJs with optimized FM electrode $Co_{60}Fe_{20}B_{20}$, pinning layer IrMn, optimized AlO_x TBs formed by oxidizing 1 *nm* Al in plasma of Ar/O_2 and magnetic thermal annealing at 265℃ for 1 hour to achieve better FM-I interface demonstrates the maximum TMR ~70 % at RT [46, 47, 152, 155]. An improved TMR~81.3% at RT (and ~95 % at 100 K) was reported by further optimization of the AlO_x TBs using inductively coupled plasma oxidation on $Co_{40}Fe_{40}B_{20}$ electrodes [173]. Therefore, the TMR values obtained in the MTJs with ALD Al_2O_3 TBs of 0.55 *nm* in thickness are comparable to the best so far achieved in MTJs made with PVD approaches. The trend of increasing TMR values with decreasing operation temperatures is anticipated from reduced scattering effect by phonons and magnons at lower temperatures [174, 175]. In fact, the 17% increase in the TMR value at 100 K as from that at 300 K in the MTJs with the 0.55 *nm* ALD Al_2O_3 TB is comparable to that previously reported on MTJs [173].

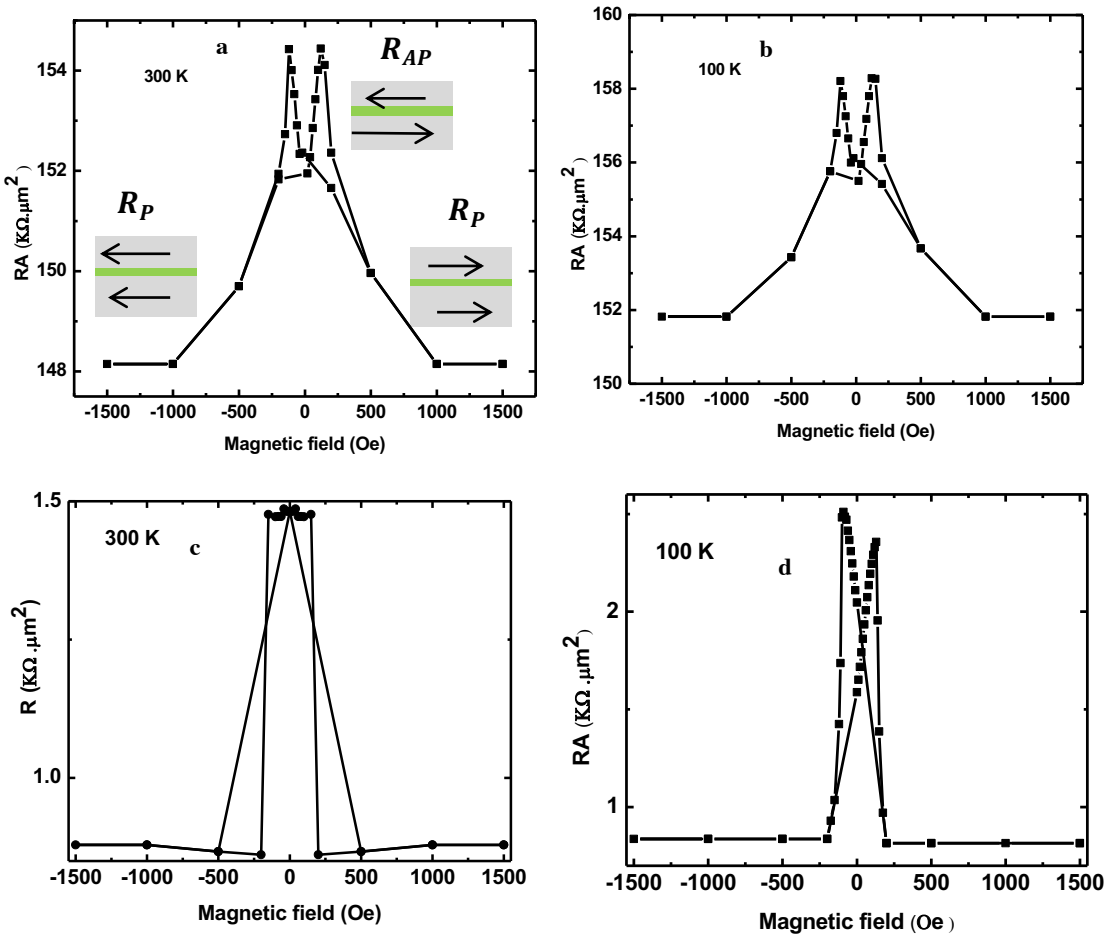

Figure 6.5 Temperature dependence hysteresis loops of RA vs magnetic field for Nb (50 nm)/Fe (50 nm)/Al (1 nm)/ ALD Al_2O_3 / Fe (5 nm)/Nb (50 nm) MTJs structure with Al wetting layer at (a) at 300 K and (b) 100 K respectively and Nb (50 nm)/Fe (50 nm)/ALD Al_2O_3 /Fe (5 nm)/Nb (50 nm) MTJs structure at (c) at 300 K and (d) 100 K without Al wetting layer respectively.

The current state-of-art MTJ fabrication uses optimized FM electrode, antiferromagnetic pinning layer, and magnetic thermal annealing and the best figure-of-merit TMR is in the range of 10-70 % for MTJs with AlO_x TBs [33-35, 46, 47, 152, 173] and 200-350 % for MTJs having epitaxial MgO TBs [4, 9, 156-159]. However, further reduction of these TBs to sub-*nm* thickness range

remains challenging due to defects, such as grain boundaries and oxygen vacancies, within the dielectric TBs, resulting in increased leakage current and incoherent tunnelling in both AlO_x or MgO based MTJs [31, 56-62, 153-155]. This is in agreement with the observed reduced E_b in range of 0.3- 0.6 eV for thermal TB based devices [152, 154, 172]. In our previous study, STS analysis reveal the importance of controlling native oxide IL, which can leads to the formation of defective ALD TBs of reduced and thickness-dependent E_b along with the soft dielectric breakdown [14, 15].

While this work represents the first success in fabrication of MTJs with sub-*nm* think ALD Al_2O_3 TBs, many efforts have been put in the synthesis of ALD TBs for MTJs in the past [107, 109, 167-169]. The reported thickness of the ALD TBs is typically in the range 2-5 *nm* due to significant increase in leakage at smaller TB thicknesses [109, 167-169]. One of the primary reasons leading to the difficulties in achieving thinner, leak-free ALD TBs in the prior effort is that these ALD TBs were fabricated using *ex situ* processes. Thus, exposure of metal surfaces to an ambient condition before ALD TB growth implies that a native oxide IL forms before nucleation of the ALD TB [109, 116-118, 167-169]. The IL has a significant impact on the quality of the ALD TBs growth on top of it because it is typically defective with oxygen vacancies and pinholes leading to the defective growth continue to ALD TBs. This explains the significant increase in leakage with *ex situ* ALD TBs at thickness below 2-5 *nm* [153-155]. However, the control over the formation of a native oxide IL, which can even form in an *in situ* ALD process have been optimized in our previous work [14, 15]. The defective ALD TBs obtained in *ex situ* ALD processes is illustrated

in the low E_b together with soft dielectric breakdown. In the *in situ* ALD processes, the IL can be reduced to negligible level ~ 0.1-0.2 *A°* [16], which not only enables sub-*nm* think pin-hole free ALD TBs to be achieved, but also reduces the defect concentration in ALD Al_2O_3 TBs as illustrated in the E_b of 1.33-1.40 eV that is significantly higher than the previously reported E_b~0.3-0.6 eV for AlO_x TBs [152, 154, 172]. This work therefore illustrates the critical importance of controlling the FM/ALD TB interface and the potential of the *in situ* ALD process for fabrication of ultrathin, high quality TBs for MTJs [33-35, 46, 47, 152, 173].

6.4 Improving MTJs Performances

It remains to be seen that higher TMR values could be obtained on MTJs with ultrathin ALD TBs after optimization of the MTJ fabrication conditions, especially in control the interface between the metal electrodes and ALD TBs. This section discusses about the future direction to improve the performance of MTJs. One option includes the use of FM material like CoFeB which has high spin polarization as compared to Fe electrode and boron acts as an oxygen diffusion barrier forming boron oxides at interface, which prevents oxidation of FM electrode and results better interface [55, 158, 159]. Figure 6.7 shows saturated magnetization M-H loop of FM CoFeB showing much larger difference in coercive field of 50 *nm* and 5 *nm* CoFeB film making it suitable choice of FM material for MTJ fabrication.

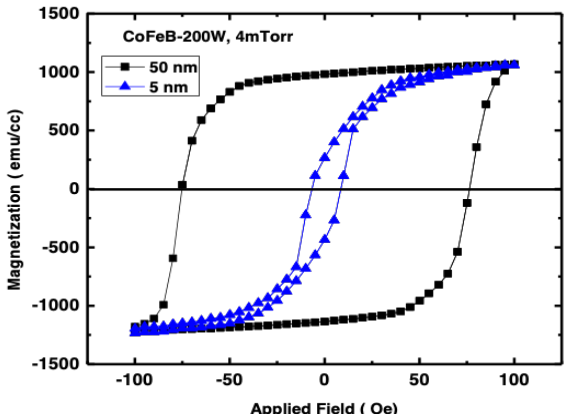

Figure 6.6 Hysteresis loop for CoFeB ferromagnetic material with 50 and 5 nm thickness characterized using vibrating sample magnetometer showing feasibility for fabrication of spin valve MTJs structure.

Another option includes the use of antiferromagnetic pinning layer for the fabrication of exchanged bias MTJ, which shows more effective switching and increase the figure-of-merit TMR. Figure 6.8(a) show the characterization of FM electrodes and the anti-ferromagnetic IrMn electrode using VSM, which shows expected M-H loops for both Fe 50 *nm* and IrMn 50 *nm* thin films. Figure 6.8(b) compares the M-H loop for Fe films with different thickness of IrMn pinning layer, which clearly indicates that the pinning is efficient for FM thickness < 10 *nm*for the fabrication of exchanged bias MTJ structure.

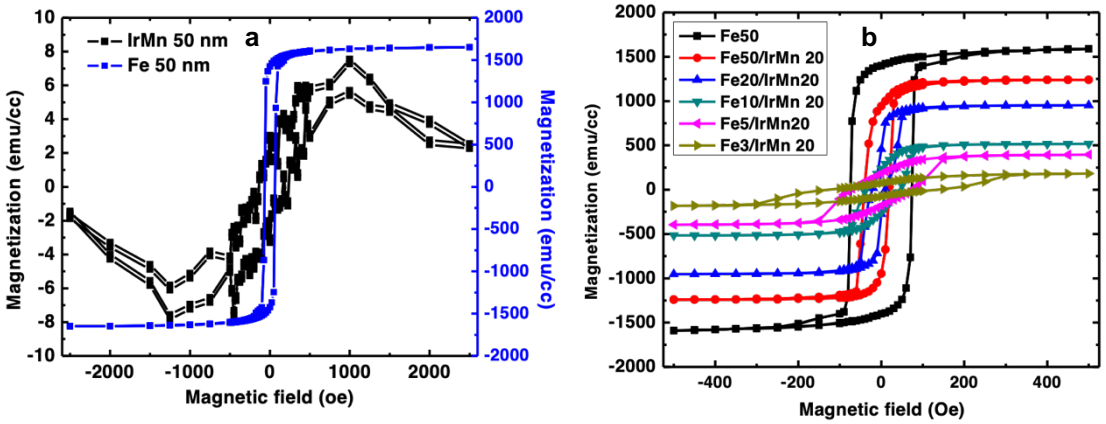

Figure 6.7 Hysteresis loop comparison for a) Fe (50 nm) and IrMn (50 nm) layers; b) Fe(50-3 nm)-IrMn (20 nm) bilayer structure with different thickness of FM material for fabrication of exchanged bias MTJs respectively.

Figure 6.8(a) compares the magnetization of Fe (3 or 5 *nm*)/IrMn (20 *nm*) bilayer structure before and after magnetic thermal annealing (MTA). The MTA condition was optimized after several tests run with annealing temperature in range between 160-175°C with H ~1000 Oe for 30 min and cooled to RT under the external H. The M-H loop comparison shows the effect of exchange bias mechanism after annealing with Fe 5 *nm*. However, Fe 3 *nm* do not show much exchange bias mechanism possibly due to thin magnetic film. Figure 6.9(b) shows a multilayer structure with Fe 5 *nm* consisting of Nb(10 *nm*)/IrMn(20 *nm*)/Fe(5 *nm*)/Al(1 *nm*)/Fe(5 *nm*)/Nb(10 *nm*), which shows an exchange bias mechanism after MTA at above specified condition. The fabrication of MTJs using ultrathin ALD Al_2O_3 is encouraging, and higher TMR values could be obtained by using optimized FM electrode like $Co_{60}Fe_{20}B_{20}$, pinning layer like IrMn and magnetic thermal annealing to improve the interface between the FM electrodes and ALD TB.

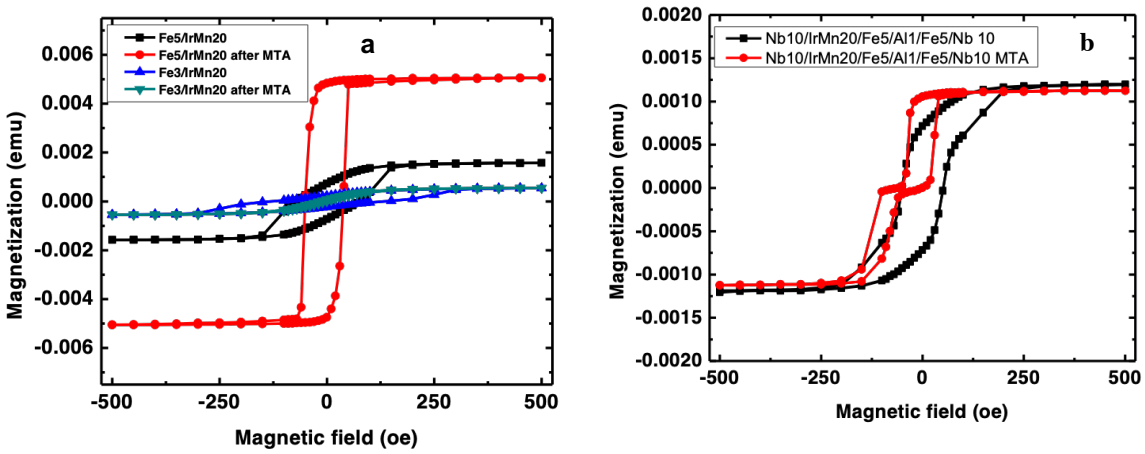

Figure 6.8 Hysteresis loop comparison for a) Fe(5nm) /IrMn (20 nm) and Fe (3 nm)/IrMn (20 nm) for bilayer structure before and after magnetic thermal annealing ; and b) Nb(10 nm)/IrMn (20 nm)/Fe(5 nm) /Al (1 nm)/Fe (5 nm)/ Nb (10 nm) before and after magnetic thermal annealing for fabrication of exchanged bias MTJs respectively.

6.5 Chapter 6 Conclusion

In summary, pinhole-free and defect-free ultrathin dielectric TBs is a key to obtaining high TMR and efficient switching in magnetic tunnel junctions (MTJs). Among others, ALD provides a unique approach for the fabrication of ultrathin TBs with several advantages including an atomic-scale control on the TB thickness, conformal coating, and low defect density. Motivated by this, this work explores fabrication and characterization of spin-valve Fe/ALD-Al_2O_3/Fe MTJs with ALD Al_2O_3 TB thickness of 0.55 *nm* using *in situ* ALD. Remarkably, high TMR values of ~77% and ~ 90% have been obtained respectively at RT and at 100 K, which are comparable to the best reported values on MTJs having thermal AlO_x TBs with optimized device structures. *In situ* scanning tunnelling spectroscopy characterization of the ALD Al_2O_3 TBs has revealed a higher E_b of 1.33 *eV*, in contrast to E_b~0.3-0.6 eV for their AlO_x TB counterparts, indicative of significantly

lower defect concentration in the former. This first success of the MTJs with sub-*nm* thick ALD Al_2O_3 TBs demonstrates the feasibility of *in situ* ALD for fabrication of pinhole-free and low-defect ultrathin TBs. Eventually this breakthrough will lead to practical applications and the performance could be further improved through device optimization.

Chapter 7 Conclusion and Future Perspective

Following the empirical Moore's law during the past few decades, the research and development with reduced dimension of devices has been the main motivation for high-performance MIM architecture. The primary challenges include the difficulties in controlling the defects and pinholes in ultrathin insulator when it's thickness approach ultrathin ~1-2 *nm* leading to an increase in *J*. Although MBE method allow the atomic layer-by-layer heteroepitaxy of different materials in the stack, the TB fabricated with PVD method is an issue. The presence of oxygen vacancies in PVD grown TBs, such as AlO_x or MgO TBs is illustrated with an increase in *J* at small TB thickness <1 *nm*, and much reduced TB height of a few sub-eV from the bulk value of a few eV detrimental to quantum coherent tunnelling that affects directly the TMR and coherence. Another challenge is the M-I interface plays a critical role in controlling the quality of the ultrathin dielectric including the barrier height, dielectric constant, electric breakdown, and uniformity. A critical step towards addressing this challenge is to establish research capability that allows for fabrication of dielectric materials and characterization of relevant properties with ultrathin, uniform, and pinhole/defect-free insulating TB on metal substrates. This would require removing the naturally formed native oxides on the surface of most metals and metallic compounds such as Al, Fe, Co, and Nb.

This dissertation has addressed the imperative and urgent ALD method to explore new approach that can grow atomically thin insulating materials with atomic resolution control, excellent coverage conformal and low defect density on functional electrodes using unique in-house

integrated *in situ* deposition (sputtering/ALD) method for fabrication of MIM architecture. The high ε_r ~8.9 within 3% of the bulk value ~9.2 and low J ~10^{-9} A/cm^2 have been demonstrated for the first time on the ALD Al_2O_3 films in thickness range ~3.3-4.4 *nm* with an effective oxide thickness ~1.4-1.9 *nm* comparable to High-K HfO_2 of 3-4 *nm*. The ALD Al_2O_3 seed layer approach was used to engineering incompatible M-I interface for obtaining high quality dielectric required for applications in MIM tunnel junctions and CMOS. This illustrates the critical importance of the control over M-I interface to obtain dense hydroxylation and reduce incubation period for improving the dielectric properties of ultrathin ALD MgO films. In addition, tuning thickness of Al wetting layer in capacitors helped in the realize FE/DE bilayer capacitors with a total FE/DE total thickness < 3-4 *nm* that show a dynamic switching on/off of the negative capacitance under the application of an external force. This not only provides a viable approach for generating ultrathin FE/DE bilayer capacitors but also offers a promising solution to low-power consumption microelectronics and piezoelectric sensors applications. The MTJs with 0.55 *nm* thick ALD Al_2O_3 TBs represents the first success with sub-*nm* thickness TBs with observe TMR ~77% at 300 K. This work revealed the significance of controlling M-I interface at an atomic scale, and paves the way for the fabrication of high quality dielectric for future microelectronics and memory application. We demonstrated that low cost, versatile and industrial compatible ALD techniques with the pinhole and defect free ultrathin conformal dielectric material provides an alternative approach for conformal and precise sub-angstrom thickness control method potential for application in ultrathin gate dielectric, spintronics and neuromorphic memory devices.

There are many research directions that can be explored for making application of ultrathin defects free dielectric especially MTJs for their application in NV-MRAM devices. The preliminary results show that the MTJ devices with optimized structure can enhance its TMR and is more efficient with exchanged bias CoFeB based FM with MgO tunnel barrier for epitaxial growth. Alternatively would be to use perpendicular magnetic materials for efficiently switching the parallel and anti-parallel orientation with spin-polarized current that reduces the power consumption with NV-MRAM applications.

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List of Publications:

1. High Tunnelling Magnetoresistance in Magnetic Tunnel Junctions with Sub-nm thick Al_2O_3 Tunnel Barriers Fabricated Using Atomic Layer Deposition **Jagaran Acharya**, Ryan Goul and Judy Wu ((Just submitted manuscript))
2. Switching On/Off of Negative Capacitance in Ultrathin Ferroelectric/Dielectric Capacitors **Jagaran Acharya**, Ryan Goul and Judy Wu (Manuscript under consideration)
3. Effect of Al_2O_3 Seed-Layer on the Dielectric and Electrical Properties of Ultrathin MgO Films Fabricated using *In Situ* Atomic Layer **Jagaran Acharya**, Ryan Goul, Devon Romine, Ridwan Sakidja, and Judy Wu ACS Applied Materials & Interfaces 11 (33) 2019
4. Electron tunnelling properties of Al_2O_3 tunnel barrier made using atomic layer deposition in multilayer devices Ryan Goul, Jamie Wilt, **Jagaran Acharya**, Bo Liu, Dan Ewing, Matthew Casper, Alex Stramel, Alan Elliot, Judy Z Wu AIP Advances 9 (2), 025018 (2019)
5. Probing Dielectric Properties of Ultrathin $Al/Al_2O_3/Al$ Trilayers Fabricated Using in Situ Sputtering and Atomic Layer Deposition ACS Applied Materials & Interfaces **Jagaran Acharya**, Jamie Wilt, Bo Liu, and Judy Wu, ACS Applied Materials & Interfaces 10 (3), 3112-3120 (2018)
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7. Disordered Bilayered $V_2O_5 \cdot nH_2O$ Shells Deposited on Vertically Aligned Carbon Nanofiber Arrays as Stable High-Capacity Sodium Ion Battery Cathodes E Brown, **Jagaran Acharya**, A Elangovan, GP Pandey, J Wu, J Li Energy Technology 6 (12), 2438-2449 (2018)
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