The DØ Central Track Trigger

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***Abstract*—An overview of the system architecture and algorithms used for the DØ Central Track Trigger (CTT) in the Run 2 of the Fermilab Tevatron Proton-Antiproton Collider is presented. This system uses information from the newly commissioned Central Fiber Tracker and Preshower Detectors to generate Level 1 trigger decisions. It also generates lists of seed tracks and preshower clusters that are sent to the Level 1 Muon Trigger, L2 Silicon Track Trigger, and Central and Forward Preshower Level 2 preprocessors. The system consists of modular boards which utilize field-programmable gate arrays (FPGAs) to implement trigger algorithms. The system delivers trigger decisions every 132 ns, based on input data flowing at a maximum sustained rate of 475 gigabits per second. The first results of trigger efficiency studies are presented.**

***Index Terms*—Data acquisition, field programmable gate arrays (FPGAs), parallel processing, particle tracking, scintillation detectors, triggering.**

I. Introduction

THE DØ detector is located at the Tevatron accelerator at Fermi National Accelerator Laboratory, Batavia, IL, [1], [2] The Tevatron accelerates protons and antiprotons to energies of about 1 TeV. Particle bunches are collided head-on in the center of the detector. Interactions between protons and antiprotons, or events, result in the production of elementary particles such as electrons, muons, quarks, and gluons materialized as jets, photons, and neutrinos (inferred by missing transverse energy of an event). Currently, the Tevatron bunch crossing period is 396 ns, however, the CTT hardware is designed to support bunch crossing periods of 396 and 132 ns.

The data bandwidth produced by all of DØ readout electronics far exceeds what can be saved for offline storage and analysis. For this reason, a trigger system is needed to quickly analyze detector data and select only the interesting physics events. DØ utilizes three levels of triggers, with each successive level incorporating more rigorous filter algorithms [3], [4]. Level 1 (L1) consists of custom hardware/firmware-based triggers that search for patterns consistent with electrons, muons, and jets. Level 2 (L2) relies on conventional CPUs and digital signal processors to combine L1 objects and additional information of muons, electrons, and jets. Level 3 (L3) is a computer farm that uses software algorithms for particle identification after simple event reconstruction. The maximum allowable trigger rates for events passing L1, L2, and L3 are about 10, 1.5, and 50 Hz, respectively.

One of the main components of the DØ trigger is the central track trigger (CTT) [5], [6], [19]. The CTT reconstructs trajectories of charged particles using fast discriminator data provided by several scintillator-based detectors. Data processed by the CTT are used to make L1 trigger decisions, otherwise known as trigger terms. While the CTT is optimized for making fast L1 trigger decisions, the electronics also store more detailed event data (e.g., sorted lists of tracks and preshower clusters) for later L2/L3 readout, or for use as seeds in other DØ trigger systems.

II. Charged Particle Tracking in DØ

The CTT system uses data from three detectors, shown in Fig. 1. The central fiber tracker (CFT), the central preshower (CPS), and the forward preshower (FPS) share common online electronics and provide full coverage of the interaction region at the center of the detector [7]–[9].

The CFT consists of 80 000 1-mm scintillating fibers mounted on eight carbon-composite cylinders at radii ranging from 20 to 55 cm. Approximately half of the CFT fibers are positioned axially (parallel to the beam line), while the rest are helically arranged at a small stereo angle. The CFT cylinders are positioned inside of a super conducting solenoid magnet that produces a 2 Tesla magnetic field. The trajectory of a charged particle is bent in the transverse (perpendicular to beam axis) plane of the detector with a curvature inversely

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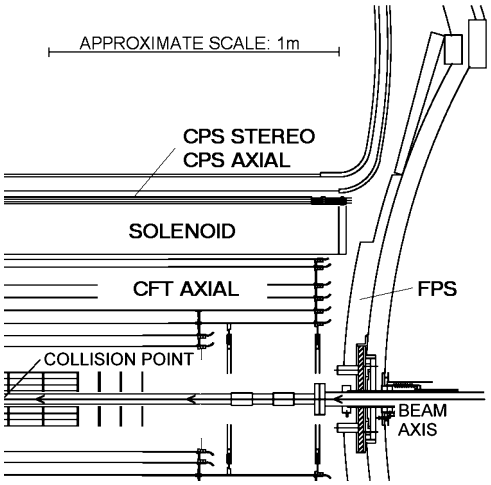

Fig. 1. Axial view of one quarter of the CFT, CPS, and FPS detectors.

proportional to the transverse momentum $\mathrm{p_T}$ of the particle. The CFT provides coverage down to about 22° from the beam axis.

The CPS is constructed of three cylindrical layers immediately outside the solenoid (radius 70 cm). One of these layers is axial and the other two are stereo layers. The CPS provides additional means of identifying electrons and photons with coverage down to about 23° from the beam axis.

Unlike the CPS and CFT detectors, the FPS detectors are oriented in the transverse plane, and are positioned near both end caps. The FPS is comprised of four stereo layers with a lead radiator in the middle. It provides additional electron and photon identification in the forward region; coverage is from 25° down to 9° from the beam axis.

The active medium of the CFT, CPS, and FPS detectors is plastic scintillator which transforms a small fraction of the energy deposited by a traversing charged particle into visible light. Approximately 100 000 optical waveguides deliver this light to visible light photon counters (VLPCs) [10], [11]. The VLPCs are light-sensitive solid-state photomultipliers that convert the light into electrical signals. When cooled to ∼9 K, the VLPCs exhibit a quantum efficiency of about 80% and a gain in the range of 17 000 to 65 000. A typical signal from a charged particle crossing a CFT fiber thus consists of about 400 000 electrons. These minute charge pulses are discriminated by the analog front-end (AFE) boards [12] located on the VLPC cryostat. The AFE boards also store the charge pulse in an analog pipeline for later digitization and readout [13].

III. Overall System Design

The input to the CTT system consists of the discriminator bits generated on the AFE boards every 132 ns. These discriminator bits are sent from the AFE boards over point-to-point low-voltage differential signal (LVDS) links to chains of digital front-end (DFE) boards, shown in Fig. 2. All of the DFE boards in the CTT system are built using a common 6 U × 320 mm motherboard that supports as many as two daughterboards. Currently, there are two different daughterboard layouts which have different sizes and numbers of

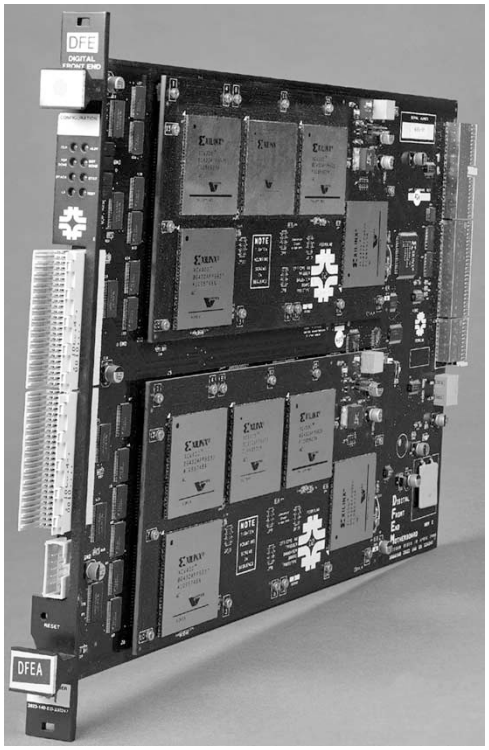

Fig. 2. A DFE motherboard with two singlewide daughterboards.

field programmable gate arrays (FPGAs). A transition board allows a DFE motherboard to drive LVDS, fiber optic, and coaxial copper links. CTT-specific protocols [6] define the data format for communication between all DFE boards and consumers. This hardware modularity, when coupled with the flexibility of FPGAs, enables the CTT designers to hide the application-specific functionality in firmware. Thus, the number of unique DFE boards in the system is minimized. This offers many benefits such as faster hardware development time, simplification of the control and monitoring software, and a reduction of spare board inventories.

The CTT system is comprised of three subsystems: CFT/CPS Axial, CPS Stereo, and FPS. Of these, CFT/CPS Axial and FPS subsystems make L1 trigger decisions and send trigger terms to the DØ trigger framework. All three subsystems participate in L2/L3 readout by sending track and cluster lists to various preprocessor and readout crates with a dead time not exceeding 5%. In the following sections we will focus primarily on the CFT/CPS Axial subsystem.

IV. CTT Subsystems

A. CFT/CPS Axial

The CFT/CPS Axial subsystem (Fig. 3) is designed to provide triggers for charged particles with $\mathrm{p_T} > 1.5$ GeV/c at the highest possible efficiency. In addition to finding tracks the CFT/CPS Axial subsystem must also find preshower clusters, match tracks to clusters, and report the overall occupancy of the CFT axial layers. Significant resources are allocated for triggering on isolated tracks, which are single high $\mathrm{p_T}$ tracks in sectors with low occupancy. The CFT/CPS Axial system also supplies the L1 Muon and L2 Silicon Track Trigger (L2STT)

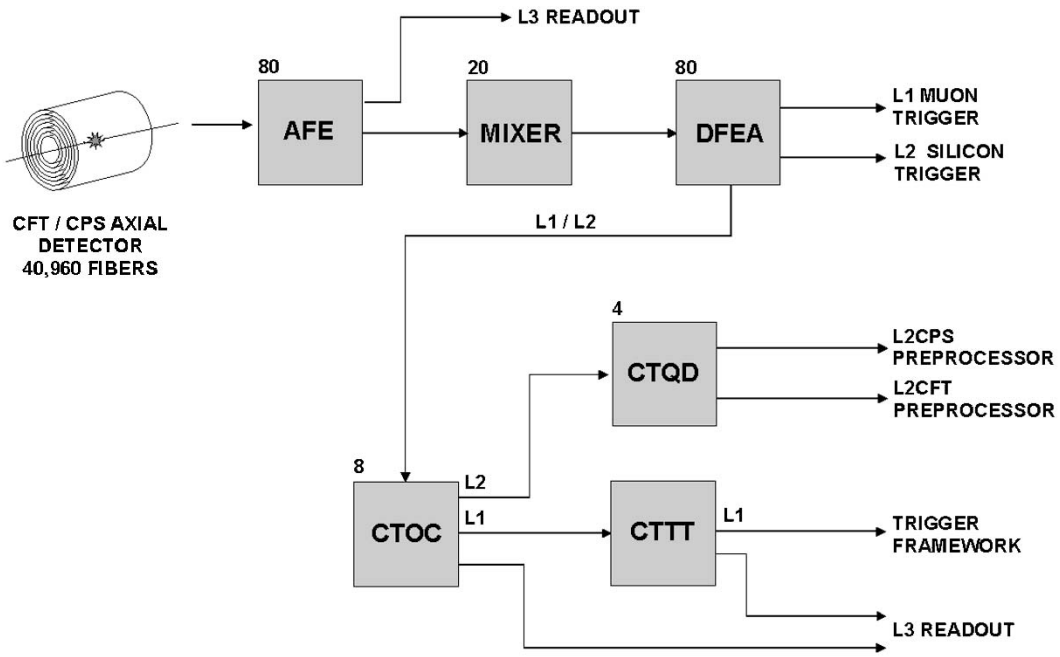

Fig. 3. The CFT/CPS axial components of the CTT system.

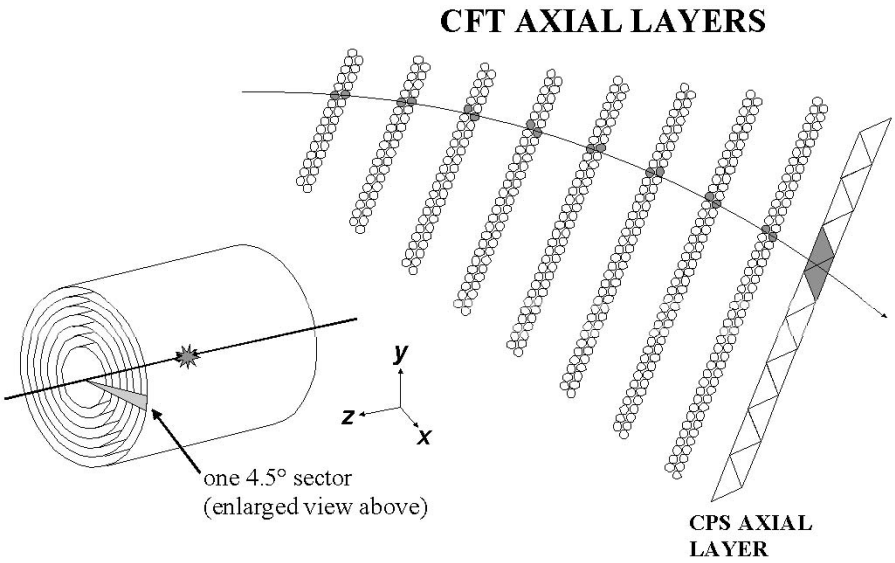

Fig. 4. Transverse schematic view of a single 4.5° sector. A hypothetical track is overlaid on the eight CFT axial "doublet" layers and CPS axial layer. Track equations require a fiber hit on all eight CFT axial layers.

systems with lists of seed tracks, and sends track and cluster information to the L2CFT and L2CPS preprocessors.

The CFT/CPS axial detector layers contain 40 960 fibers arranged in cylinders centered on the beam axis. The VLPC output signals from these fibers are discriminated by 80 512-channel AFE boards and sent out on 320 1-Gigabit per second LVDS links. Every 132 ns the AFE boards transmit a complete image of the CFT/CPS axial detector.

For mechanical reasons, the CFT and CPS axial fibers are grouped by cylinder layer before routing to the AFE boards. However, the track finder algorithms require the fiber information to be arranged in 4.5° sectors in the transverse plane (Fig. 4). Furthermore, each track finder daughterboard must receive information from each of its neighboring sectors in order to find tracks which cross-sector boundaries. A set of 20 mixer boards [14], [15] handles this data reorganization and duplication. After data duplication, the mixer output data rate is a constant 475 gigabits per second. Total latency through the mixer system is 200 ns.

TABLE I
TRACK EQUATION DISTRIBUTION IN TRACK FINDER FPGAS

p_T Bin	p_T Range (GeV/c)	Track Equations	FPGA Resources (system gates)
Maximum	>10	3000	200k
High	5 to 10	3000	200k
Medium	3 to 5	4000	300k
Low	1.5 to 3	10000	500k

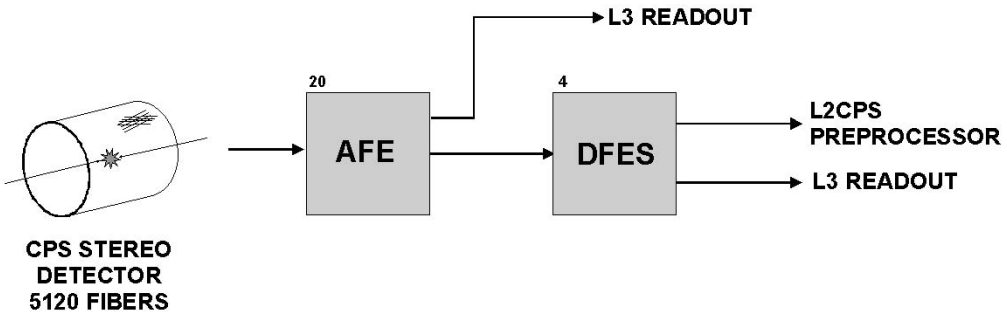

Fig. 5. CPS Stereo subsystem hardware.

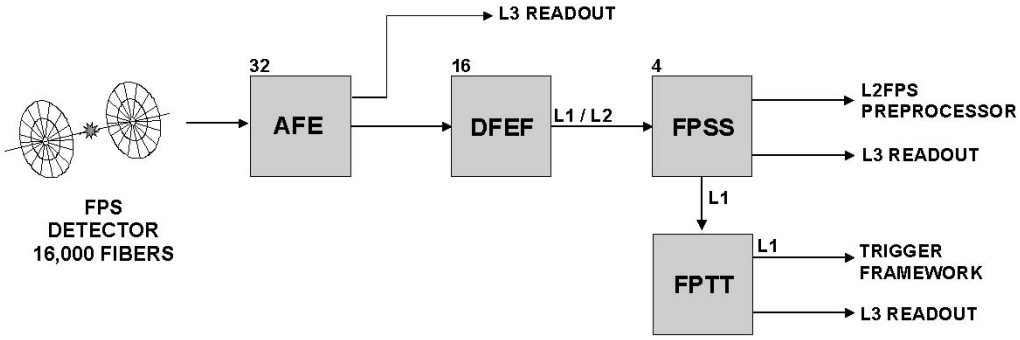

Fig. 6. FPS subsystem hardware.

From the mixer system, the properly organized discriminator bits are sent to the first tier of digital front end boards. This first tier consists of 40 motherboards, with each motherboard having two singlewide daughterboards (DFEAs). Each DFEA daughterboard unpacks the CFT data and compares the fiber hits against approximately 20 000 predefined track equations. In order to minimize latency, this operation is performed in parallel using combinatorial logic in FPGAs. Device resources are balanced by grouping track equations into four $\mathrm{p_T}$ bins, with each $\mathrm{p_T}$ bin corresponding to a single FPGA, as shown in Table I.

Each track finder FPGA outputs the six highest $\mathrm{p_T}$ tracks it finds; these tracks are passed to a fifth FPGA for additional processing which includes sorting, matching tracks and CPS clusters, counting tracks, calculating sector occupancy and total $\mathrm{p_T}$ [16]. Tracks from each sector are sent over gigabit coaxial cables to the L1 Muon trigger, where the tracks are matched to hits in the Muon detector. (L1 Muon requires these seed tracks within 1 μs after beam crossing.) Counts of tracks and occupancy data are passed downstream to the octant boards over LVDS links.

The next tier of DFE boards (CTOC) collects and sorts data within an octant (10 sectors). In L1 mode, these boards receive track counts and sector occupancy data from the DFEAs. The CTOC boards must sum up the number of tracks, determine which sector had the most fibers hit, and check for isolated tracks. This information is passed on downstream to a single DFE board (CTTT) where the individual trigger term bits are generated and sent to the DØ trigger framework within 2.5 μs of the beam crossing. The CTTT can provide up to 96 trigger terms of which 55 are currently defined. Examples of CTTT trigger terms are: at least one or at least two tracks above a $\mathrm{p_T}$ threshold of 1.5, 3, 5, or 10 GeV/c or at least one isolated track above 5 or 10 GeV/c; and at least one track with a confirmation in the preshower for triggering on electrons.

The DØ trigger framework considers trigger term bits from many different subsystems (i.e., CTT, L1 muon, etc.) and makes a global L1 decision. When this occurs a L1_ACCEPT control bit is sent to all of the readout electronics. Upon receiving an L1_ACCEPT the AFE boards jump back a fixed number of events in their analog buffers and digitize the fiber data with 8-bit resolution. When the L1_ACCEPT control bit embedded in the data stream reaches the DFEA boards, these then send a sorted list of found tracks and CPS clusters to the CTOC boards. The lists are sorted by the CTOC and CTQD boards and passed downstream to preprocessor crates for more detailed analysis. These track lists, remapped onto the geometry of the DØ silicon tracker, are also used as seeds for the L2STT. Additionally, the CTOC and CTTT boards send copies of their input data to a L3 readout crate for monitoring and debugging.

B. CPS Stereo

The CPS Stereo subsystem (Fig. 5) is used to provide additional track information in the axial plane of the detector.

Unlike the other CTT subsystems, CPS Stereo does not generate L1 trigger terms. Rather, the DFES boards store discriminator bits and begin processing only after a L1 trigger decision has been made by the DØ trigger framework.

Event buffers in the DFES FPGAs store discriminator bits sent from the AFE boards. Upon receipt of the L1_ACCEPT control bit the DFES boards extract the discriminator bits and search for clusters of hits in the stereo layers [17]. Sorted lists of CPS clusters are sent on the L2CPS preprocessor for additional

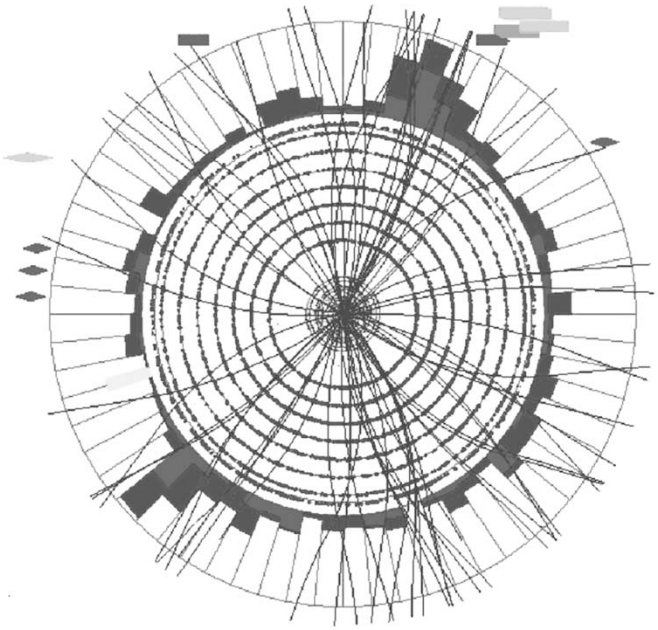

Fig. 7. Transverse view of the central DØ detector showing reconstructed tracks triggered by the CTT. This composite view also displays energy deposited in the central calorimeter, shown as towers in the outer ring.

analysis. The DFES boards also send a copy of the discriminator bits to the L3 readout system.

C. FPS

The FPS subsystem (Fig. 6) produces its own set of L1 trigger terms, which are passed to the DØ trigger framework [18]. The overall structure of the FPS subsystem is similar to the CFT/CPS Axial subsystem in that FPS has three tiers of DFE boards: a finder (DFEF); a concentrator (FPSS); and trigger term generator (FPTT).

The DFEF boards receive discriminator bits from the AFE boards and search for clusters of hits in the FPS fiber layers. A list of clusters is stored in the DFEF for later L2 readout while counts of clusters are passed downstream to the FPSS boards. The FPSS boards sum these cluster counts and pass this information to the FPTT, where the L1 trigger terms are produced. These trigger terms must reach the trigger framework within 2.5 μs after beam crossing.

When the DØ trigger framework issues a L1_ACCEPT the FPS subsystem switches into readout mode. The AFE boards begin digitizing and reading out fiber data, while the DFEF boards extract cluster lists from their buffers. These lists of clusters are concatenated and sorted by the FPSS boards before being sent to the L2FPS preprocessor. The FPSS and FPTT boards send their L1 input data to the L3 readout system.

V. CTT Performance

Fig. 7 shows an example event in which the CTT triggers on high $\mathrm{p_T}$ tracks associated with electromagnetic clusters.

One way to quantify the CTT performance is to compare CTT trigger terms against data reconstructed offline. An early example of an efficiency study is shown here. Fig. 8 plots the efficiency of the TTK(1, 10) trigger term, which is set for one or more tracks above a $\mathrm{p_T}$ threshold 10 GeV/c. First, several hundred thousand events (unbiased with respect to charged tracking triggers) are selected. These events are required to have good quality tracks reconstructed by the offline system from the digitized fiber charge information. Events with at least one track above 10 GeV/c are selected. For these events the efficiency of the trigger term is computed as the fraction of events that have the online TTK(1, 10) bit set.

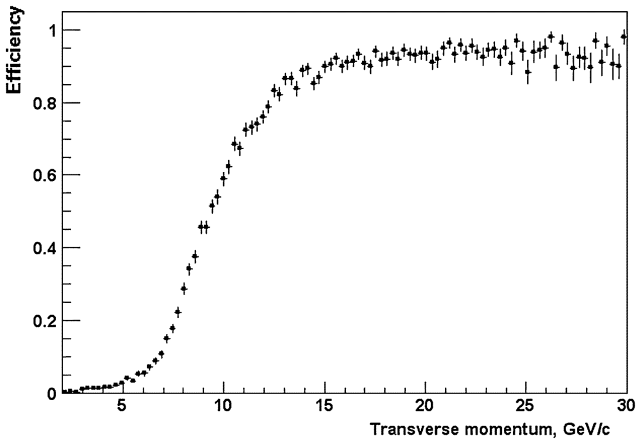

Fig. 8. Efficiency of CTT triggering on at least one track with $\mathrm{p_T} > 10$ GeV as a function of offline track $\mathrm{p_T}$. Efficiency at the plateau continues to improve as the track equations are fine tuned to better match the detector geometry.

VI. Conclusion

The first trigger terms from the CFT/CPS Axial chain were commissioned in February 2003, and the system has been in stable operation since. Offline studies of these trigger terms demonstrate that the CTT system is efficient in finding and triggering on charged particle tracks. Firmware exploiting more complex signatures (tracks with matching preshower signals, local isolation and local and global detector occupancy) is being deployed and studied. The input chain for the DØ L2STT system is being commissioned. All hardware for the CPS Stereo and FPS subsystems is in place and firmware is currently being developed.

In order to further improve background rejection and $\mathrm{p_T}$ resolution an upgrade for the DFEA track finder daughterboards is being studied. These next generation DFEA daughterboards will use several multimillion gate Virtex II FPGAs [20] and we expect first prototypes later this year.

The CTT in its current configuration will allow the DØ Collaboration to take full advantage of the unique physics opportunities of Run II.

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